6.8. Chapter Summary

This chapter deals with operation of the QUCS software, which is at the l
implementation of the model that has been created.

The essential elements of the circuit simulation with QUCS are shown. M
representations of the physical operation are developed and it is demons
these equations can be modified. Parameter modification is also demon
the overarching design process for adding new component models to th
shown.

The iterative flow path for designing the new floating gate device is shown
Also shown are the schematic representations for simulation.

This chapter also contains details of the use of equation defined device
the compact models are based, and specifically, the way they apply to
floating gate device model. The formats for the EDD equations repre
floating gate device were then developed. This was done specifically for th
EKV v2.6 Long Channel transistor model as shown in Fig.6.6.1. This mo
effectively connected to an additional set of EEDs that represent the m
required in order to allow the modified EKV model to operate as a fl
device.

Finally, a single schematic representation has been developed and is
Fig.6.7.6.

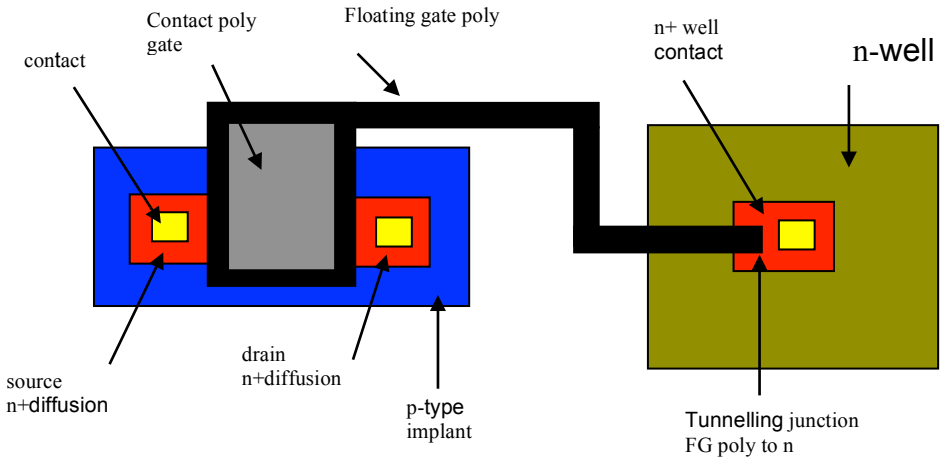
Chapter 7.

Simulation of Floating Gate models in MOS operating regions.

7.1. Physical Structure

The physics justifying the structure and parameters associated with the model were taken from references [14,24,25,27,29,32]. A typical example of a Floating Gate device was shown in Fig.3.1.1. and is repeated in Fig.7.1.1. other examples can be seen in Appendix (5). For the device shown the tunnel charging element is shown as a separate section of the device with the floating gate polysilicon being common to both elements. A fundamental element of the floating gate model created is the EKV v2.6 MOSFET. The EKV v2.6 MOSFET model is a physics based model that relies on the processing limitations and tolerances of the fabrication parameters. A charge based model for the calculation of the transcapacitances is used [10], which ensures charge conservation during transit analysis. For the EKV model using submicron technology this uses an oxide thickness <10nm that is close to conventional processing limits. Some of the design equations have already been shown in Ch.6. and a more comprehensive version can be obtained from ref.[10,24].

(a)



(b)

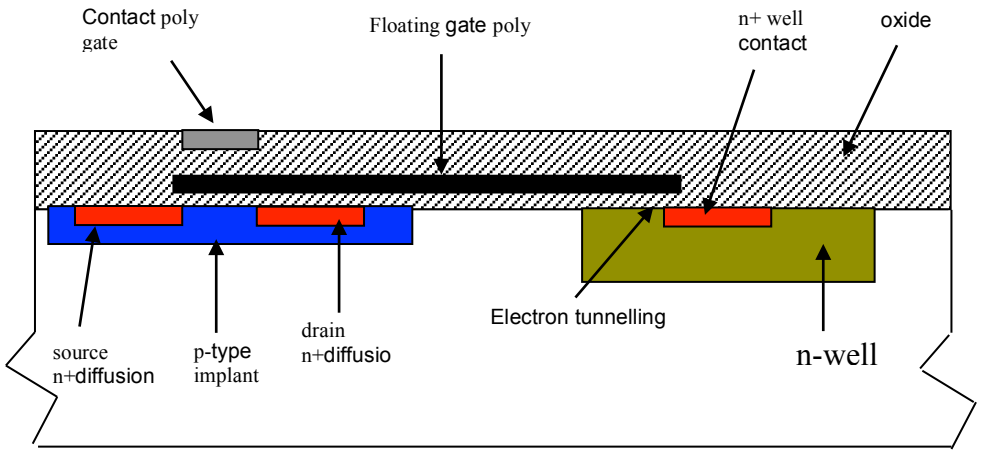


Fig.7.1.1. General structure of a Floatung Gate Device (a) plan (b) sectional

7.2. QUCS 7-port simulation model for floating gate device.

Shown in Fig.7.2.1. is the schematic representation of the floating gate model that has been developed for the QUCS simulation package. Central to the model is the EKV transistor model EKVLC1 and shown are some of the models associated parameters. The parameters shown happen to be the default values but may be adjusted to suit design and processing variations. The EKV parameters are accessed

by double clicking on the transistor's symbolic representation within QUCS. The charging tunnelling current is controlled by the EDD "D1". The other components associated with the model, $C_{cont.}$, and C_{fg} are calculated upon the basis of device design, and K is a constant that modifies these capacitances due to the physical structure. $R_{cont.}$, and R_{fg} are selected on the basis of a time constant that won't interfere throughout the simulation period, but allows an electrical connection to the floating gate so that analysis can be carried out.

The EDD D1 is added so that the floating gate can be programmed via the tunnelling terminal T. When a voltage is applied to the tunnelling terminal T, no charge will flow into the floating gate while $V_3 \geq V_2$ otherwise charge flowing onto floating gate is 9.35e8*exp(-368.04/($V_3 - V_2$ +1E-20)).

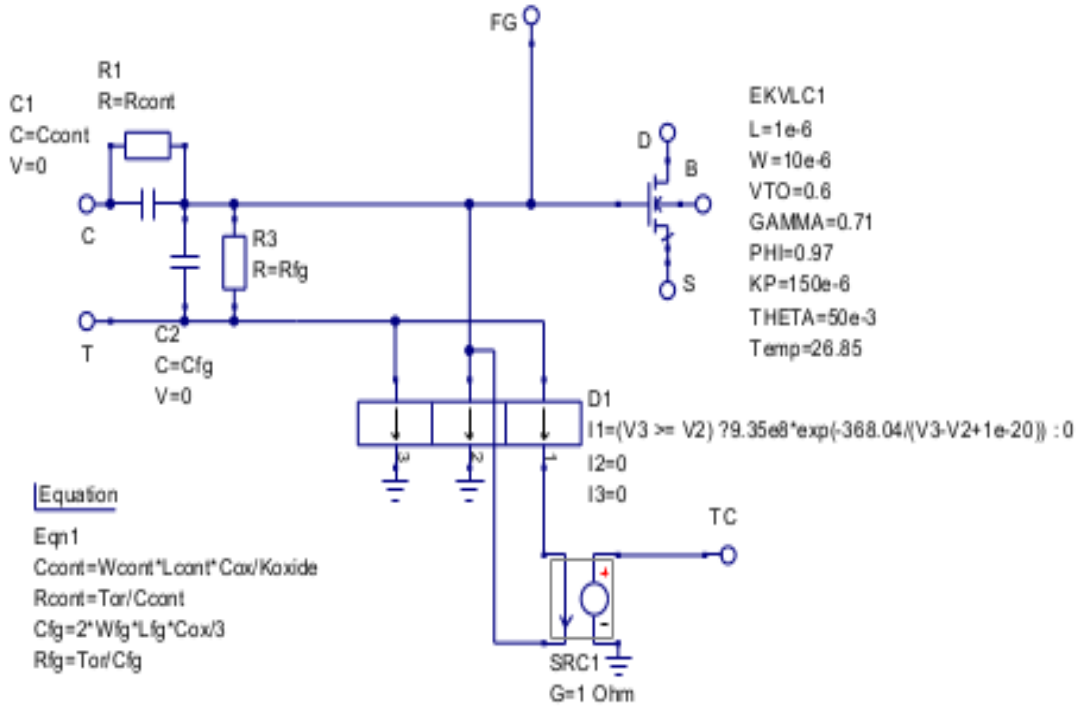


Fig.7.2.1. QUCS model for Floating Gate

7.3. Simulation circuit for charge transfer.

Fig.7.3.1. shows the symbol FG1 that was created to represent the circuit shown in Fig.7.2.1.

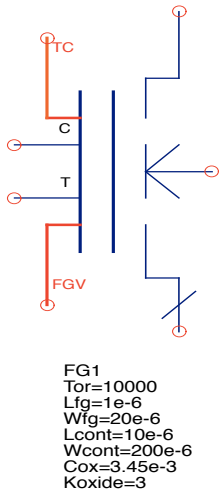


Fig.7.3.1. QUCS symbol created for sub circuit shown in Fig.7.2.1.

The symbol was then used as a subcircuit within the circuit configuration shown in Fig.7.3.2. that was used for charge transfer on to the floating gate. Parameters are passed to the subcircuit, and the time constant, Tor, has been set to 10000s. This allows access to the floating node whilst having a minimal effect on the model performance.

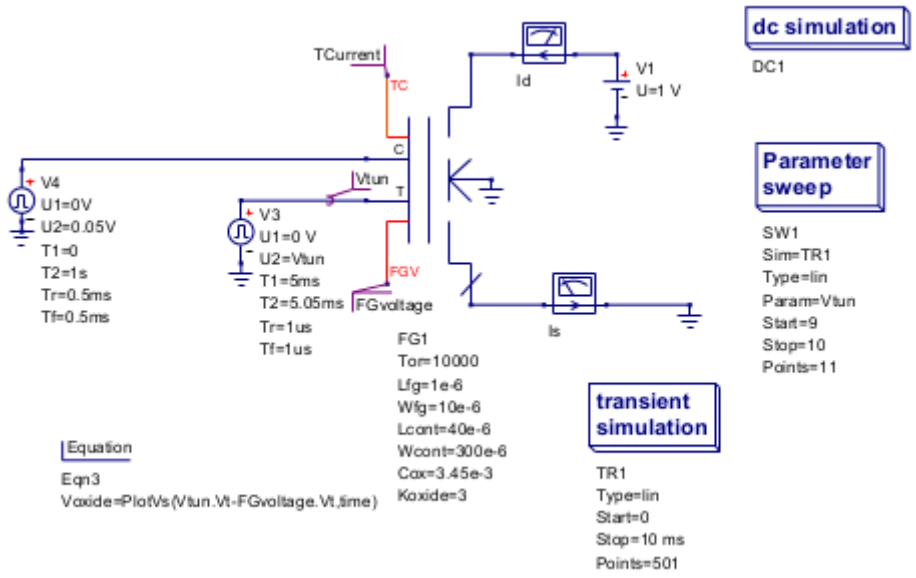


Fig.7.3.2. QUCS model for charge transfer

7.4. Charge Partitioning

For the EKV model used there is a parameter named Xpart, which sets up the proportion of the channel charge between the drain and source. Early editions of QUCS used a 50/50 split purely as a convenient split. The later versions of QUCS have modified the division of charge so that more accurate levels of division can be used. Typically for digital systems a split 0/100 is used. For this work it is set to a default value of 0.4, which indicates a 40/60 split between drain and source, Appendix 3, but may easily be modified when setting transistor parameters.

7.5. Sweep responses for Floating Gate voltage v Drain Source current for voltage directly applied to Floating Gate

Fig. 7.5.1 (a) and (b) shows a simulation circuit and sweep response for the designed floating gate device with a voltage being directly applied to the floating gate so emulating various quantities of charge being present on the floating gate.

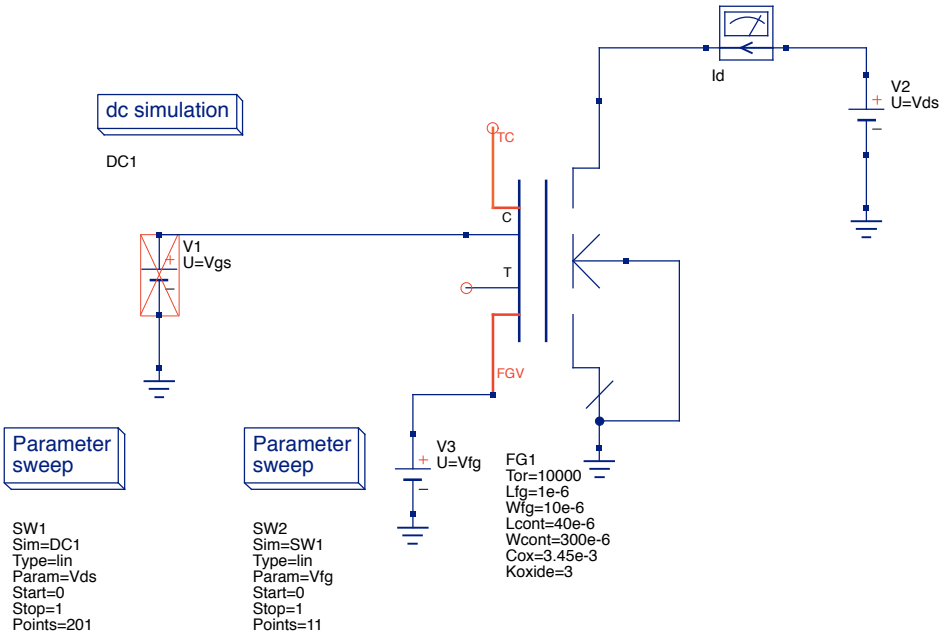


Fig.7.5.1.(a). Simulation circuit for external voltage applied to floating gate

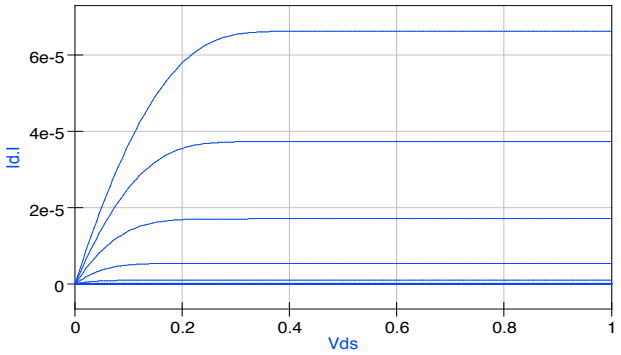


Fig.7.5.1.(b) Sweep simulation response for Fig.7.5.1.(a)

The simulation shown in Fig.7.5.1. is defined by the sweep parameters SW1 and SW2 equations and using the floating gate transistor FG1, with parameters as shown. This could then be used with reference to the full analysis shown in Chapter 8.

7.6. Simulation circuit for Pulsed response

Fig. 7.6.1. shows the schematic simulation circuit for programming the floating gate device. Pulsed tunnel voltages are applied between 9 – 10V in steps of 0.1V. The Control Voltage is set at a subthreshold value of 0.05V. The tunnel pulses are applied from 5 – 6ms. After the tunnel pulse is removed the resultant increase of the floating gate voltage can be seen.

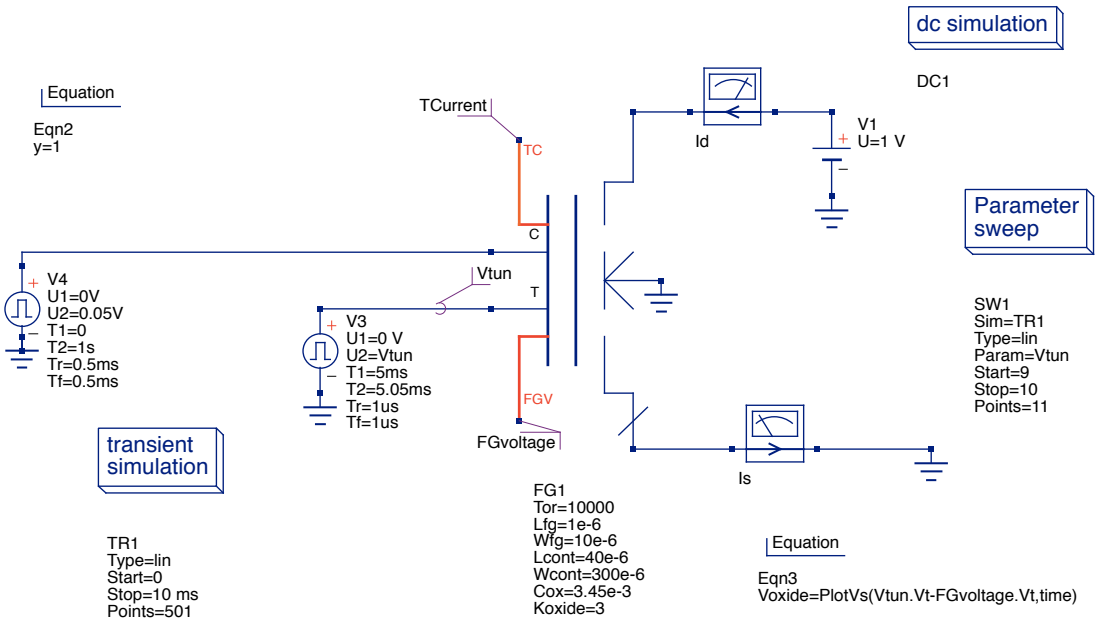


Fig.7.6.1. Schematic for simulation of charging of floating gate for pulsed voltages applied to tunnelling terminal.

The results of the simulation are shown in Fig.7.6.2.(a) and (b).

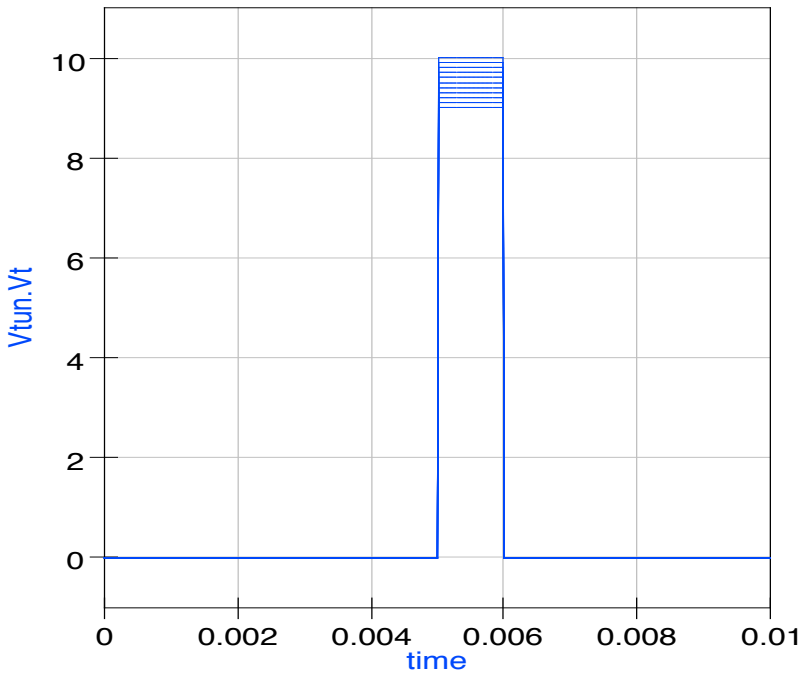


Fig.7.6.2.(a) Pulsed tunnel voltage

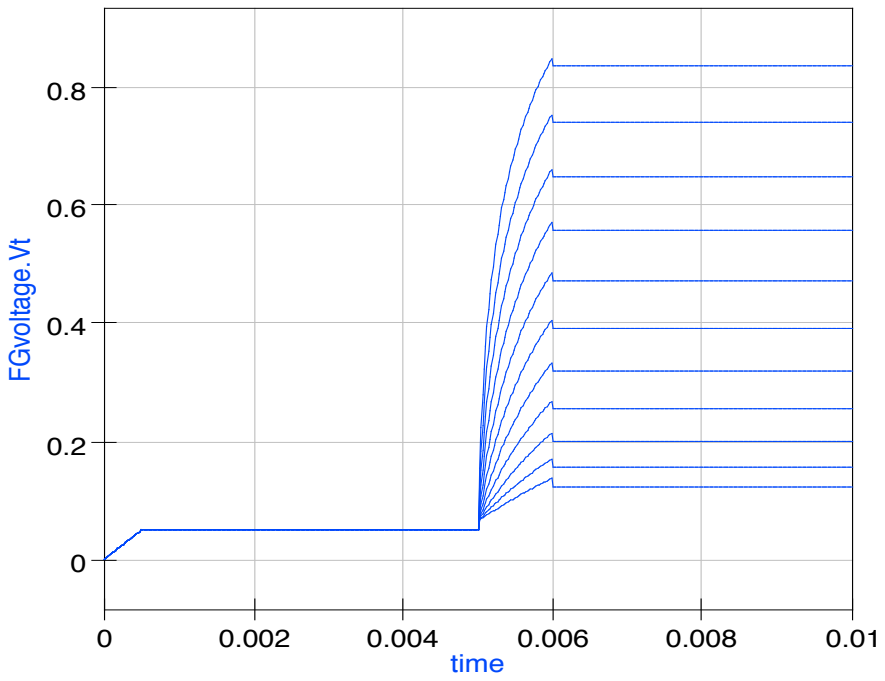


Fig.7.6.2.b. Floating gate voltage before, during and after application of tunnel voltage pulse.

Fig.7.6.2.a. shows the magnitude of the simulation voltages for the series of pulses that are applied to the tunnelling terminal for 50ms, from 9 – 10V in steps of 0.1V. Whilst Fig.7.6.2.b. shows the value of the floating gate voltage during the eleven simulations, and most importantly the retained floating gate voltage.

Initially contact and tunnelling voltages = 0V

After 0.05ms the contact voltage has risen to 0.05V and this is reflected in the rise of the floating gate voltage.

From 5 – 6ms a tunnelling voltage is applied. During this time charge carriers are injected onto the floating gate

After 6ms the tunnelling voltage is removed. There is a slight drop in the floating gate voltage due the effect of the contact voltage. However it is clear that the charge carriers injected onto the floating gate are now trapped and that the floating gate voltage has been increased.

The simulation process is then repeated for tunnelling voltages increments of 0.1V between 9 – 10V.

7.7 Chapter Summary

This chapter deals with the approach to the characterisation of the floating gate device. The device structure is again shown in Fig.1.1.a & b. (as in Fig.3.1.1.a & b.). This is then detailed as the EKV v2.6. schematic with the necessary modifications that are required to create a floating gate device. This includes the R-C networks associated with the Contact terminal and the Tunnelling terminal. Also shown is the EDD that enabled the floating gate to charge under the correct tunnel voltages. In Fig.7.3.2. the simulation circuit shows the test pulses that were applied to the tunnelling terminal and the contact voltage that takes the form of an extended pulse of a duration beyond the simulation time.

Charge partitioning was also considered so that both analogue and digital applications could be considered for design.

Fig.7.6.2.a. & b. show the simulation responses for a range of pulses from 9 – 10V with the Contact voltage set to 0.05V for a drain-source voltage of 1V. The results clearly show the increase of floating gate voltage during and after programming.

Chapter 8.

Simulation, Settings and Results of Simulation

8.1. Test circuit used for simulation

The simulation circuit was based on the Floating Gate transistor model created and is shown in Fig.8.1.1.

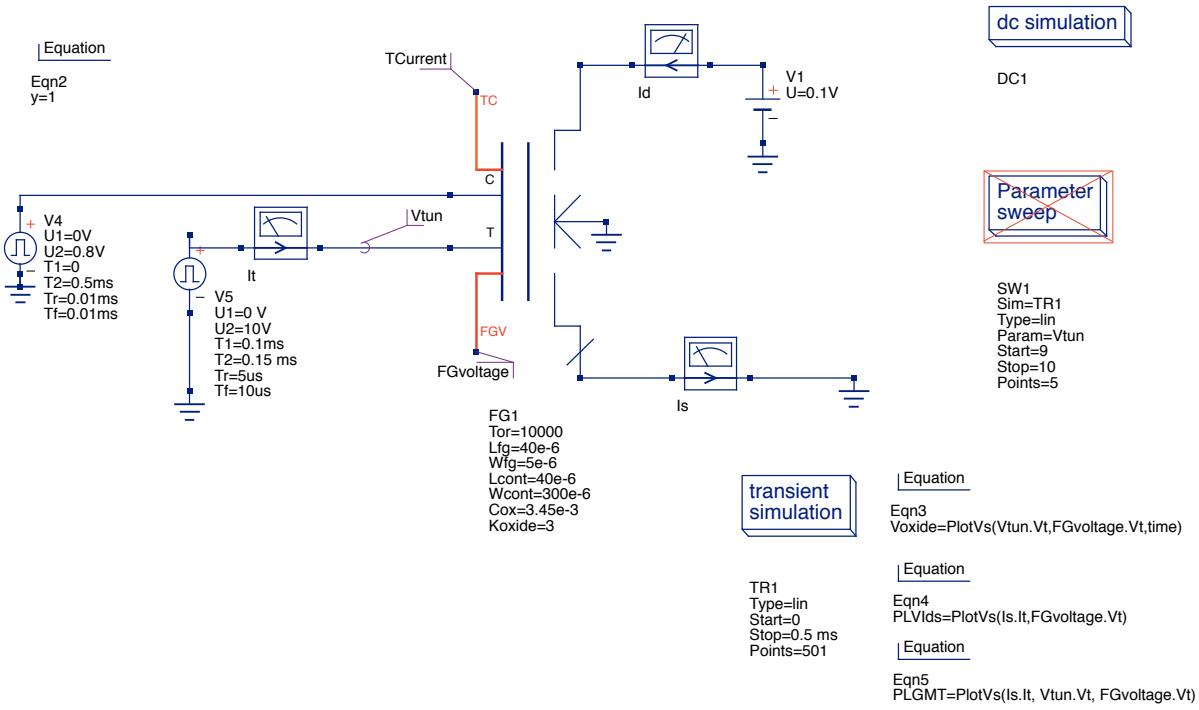


Fig.8.1.1. Schematic for Floating Gate transistor, FG1, charging.

For the schematic transient simulations were carried out over 250ms. Drain-source voltage was set by V_1 and effectively the gate-source (contact) voltage was set by V_4. The value of V_{gs} was given a rise time of 0.01ms and effectively remained at the U_2 level throughout the simulation. The tunnelling voltage was set by V_5, this was a voltage pulse starting at (V_5) U_1 and rising to (V_5) U_2, with a rise time Tr and a fall time Tf.

The schematic equations represent the values that are to be plotted after the simulation is completed.

The QUCS schematic circuit that was used to carry out the simulations of the floating gate device is shown in Fig.8.1.1. and covered the following regions:-

(i) above threshold and above saturation

(ii) above threshold and below saturation

(iii) below threshold and above saturation

(iv) below threshold and below saturation.

Results obtained were then tabulated and graphs for the modification of the floating gate voltage and variation in source drain current were plotted at the beginning and end of the tunnelling pulse, and after the pulse was removed.

With regards to the subcircuit model for FG1 it is important to note that parameters can be passed from the schematic to the subcircuit model where they can be used in calculations, i.e. T_{or}, L_{fg}, W_{fg}, L_{cont}, W_{cont}, C_{ox}, and K_{oxide} values can be used.

The floating gate transistor FG1 was created to be part of the QUCS library and can be called upon to be placed on a schematic. Details of the subcircuit that represents the floating gate devices can be accessed by highlighting it and clicking the pop-down icon. The subcircuit is shown in Fig.8.1.2.

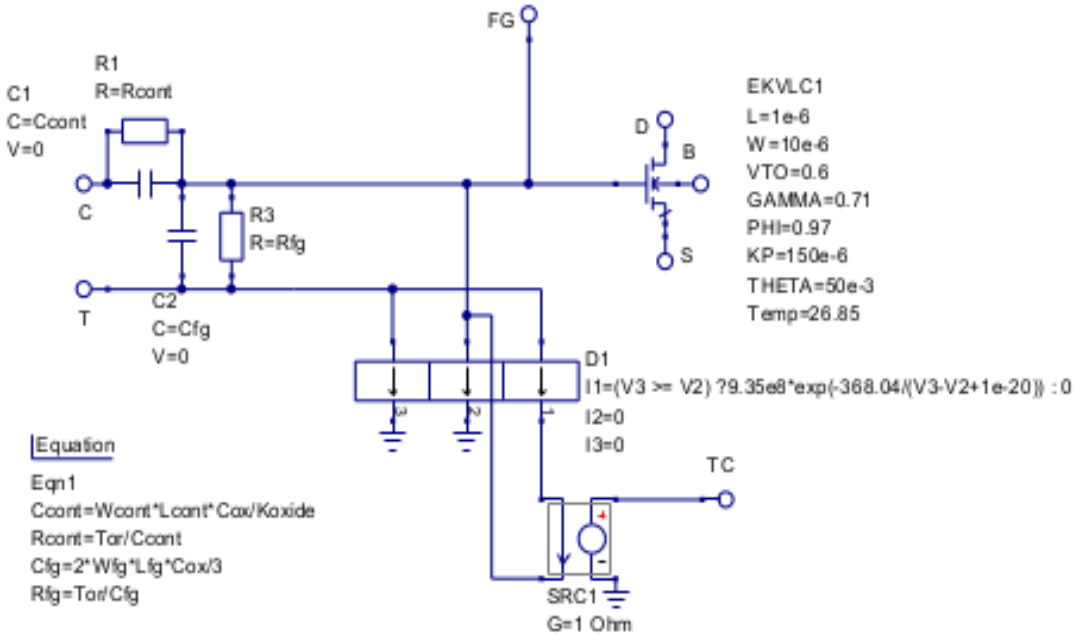


Fig.8.1.2. Schematic subcircuit for Floating Gate transistor, FG1.

Value for L_{fg}, W_{fg}, L_{cont} and W_{cont}, can be set from the parameter values in the schematic. The EDD, D1, defines the tunnelling operation for the floating gate transistor. The transistor EKVLC1 is basically the EKVv2.6 Long Channel device and uses the default parameters apart from the ones shown changed in this subcircuit. In turn the subcircuit model of this device can be accessed to show its EDD equivalent that has already been referred to in Fig. 6.7.1.

In Fig.8.1.3. and Fig.8.1.4. show the responses to a single simulation run for the schematic shown in Fig.8.1.1.

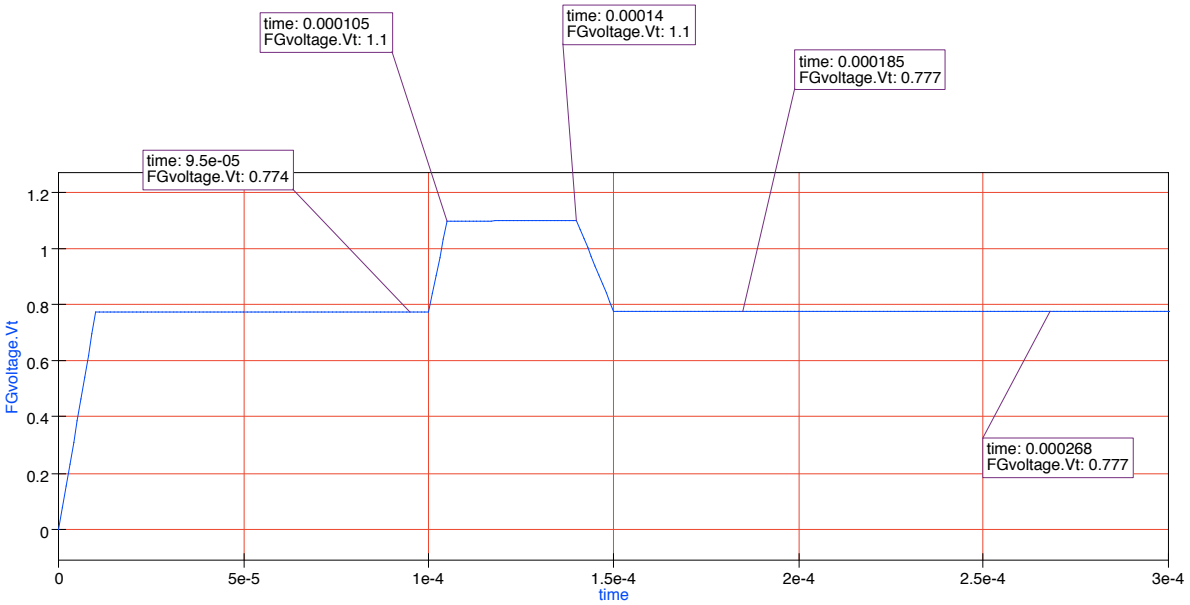


Fig.8.1.3. Floating Gate voltage during simulation.

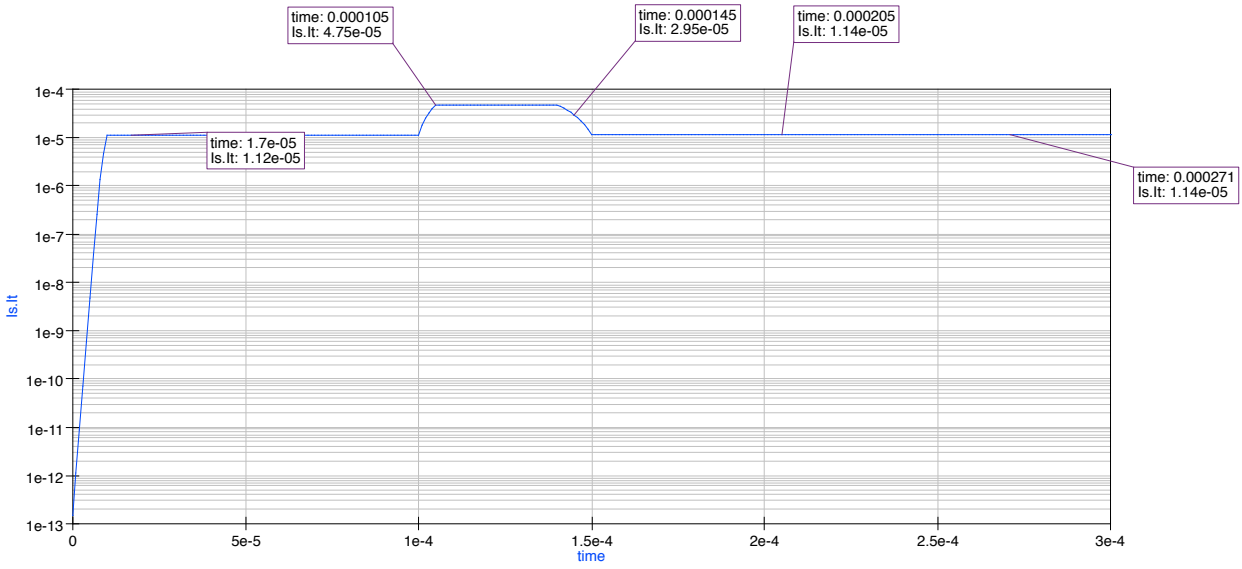


Fig.8.1.4. Source current during simulation

Fig.8.1.1. formed the basis of the measurement to demonstrate the operation of the FG device. The dimensions are as shown and the drain-source, and contact voltages are set for the four different regions. The tunnelling voltage is then varied according to the Parameter Sweep and various measurements are taken as indicated by Fig.8.1.3. and Fig.8.1.4.

8.2. Simulation Results.

The actual simulation schematic was as shown in Fig.8.1.1. Four series of simulations were carried out defined by the combinations of biasing voltages indicated in section 8.1. for Contact voltage and Drain-Source voltage. Full details of the simulation results can be seen in Appendix 6. Measured results are:- **Tunnel Voltage, Floating Gate Voltage at start of pulse, Floating Gate Voltage after pulse rise, Floating Gate Voltage before pulse fall, Floating Gate Voltage after pulse fall, Floating Gate Voltage after Contact Voltage removed, Source Current before pulse, Source Current after initial pulse rise, Source Current at end of pulse before fall, Source Current after pulse removed, Source Current after Contact Voltage removed, Tunnel Current at start of pulse, Tunnel Current at the end of pulse.**

These simulation results give an excellent picture of charge movement for the tunnelling process and show the degree of programming that has taken place.

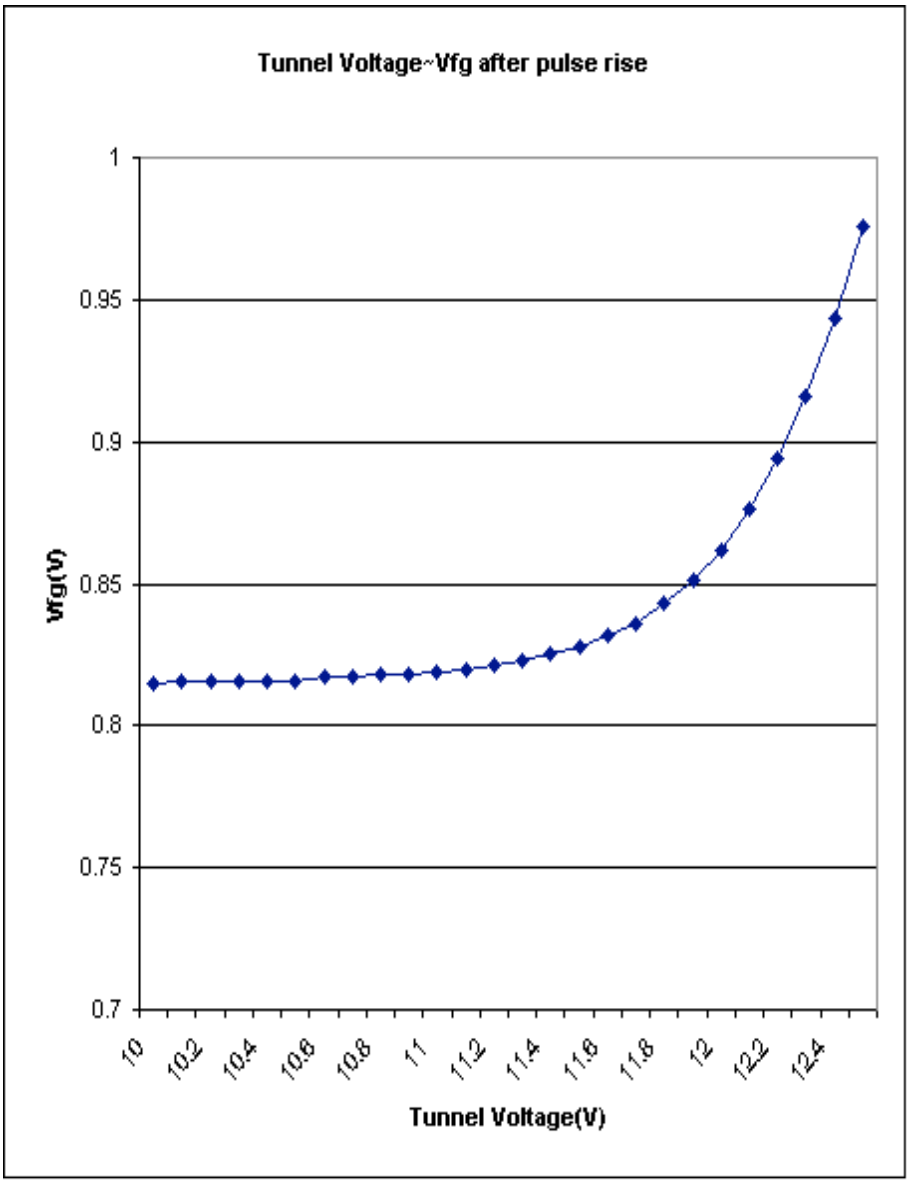
Graphical representation of these results are shown in section 8.3. and summaries are shown after each series of graphical results.

8.3. QUCS Simulation data for floating gate MOS device based on EKV v 2.6

8.3.1.1. Series 1

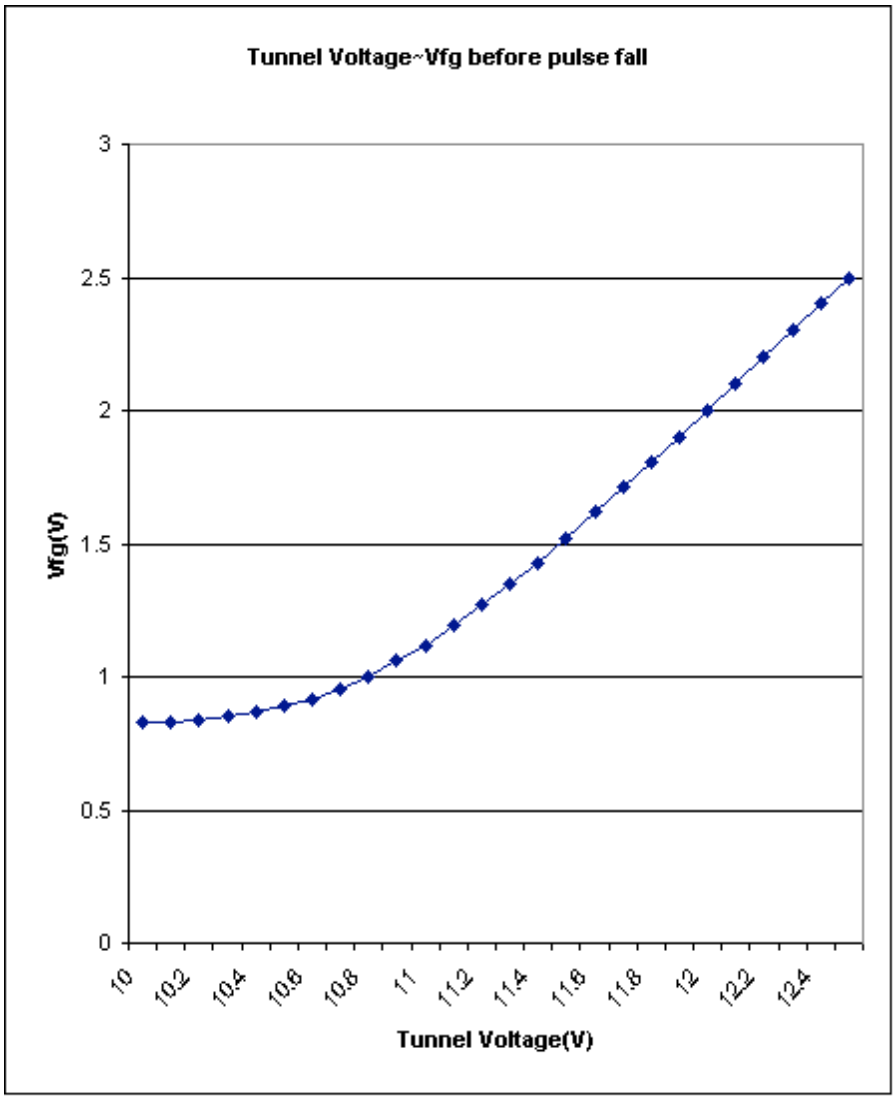
Fig.8.3.1.1. .V_c = 0.8V, V_{ds} = 2V T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 10 – 12.5V in steps of 0.1V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

Tunnel Voltage (volts)	Vfg after pulse rise (volts)
10	0.815
10.1	0.816
10.2	0.816
10.3	0.816
10.4	0.816
10.5	0.816
10.6	0.817
10.7	0.817
10.8	0.818
10.9	0.818
11	0.819
11.1	0.82
11.2	0.821
11.3	0.823
11.4	0.825
11.5	0.828
11.6	0.832
11.7	0.836
11.8	0.843
11.9	0.851
12	0.862
12.1	0.876
12.2	0.894
12.3	0.916
12.4	0.943
12.5	0.976



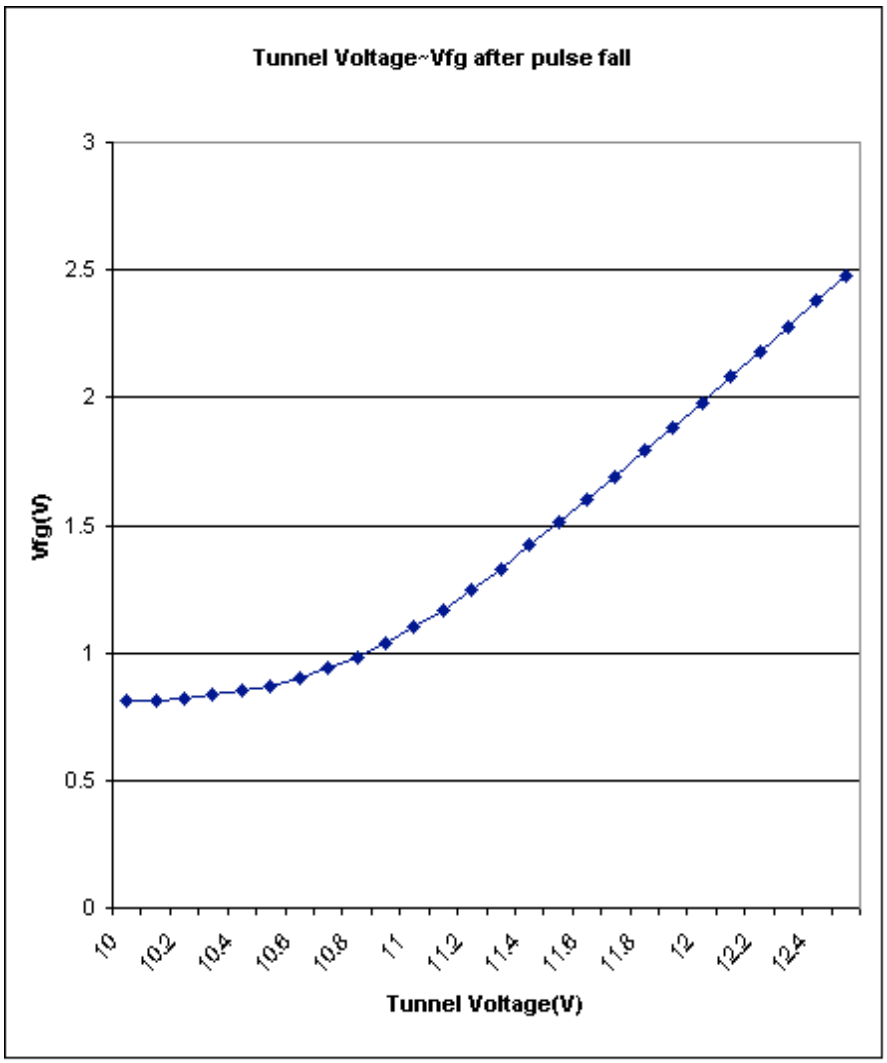
QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 1
Fig.8.3.1.2. V_c = 0.8V, V_{ds} = 2V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 10 – 12.5V in steps of 0.1V.
Total pulse duration = 50µs, T_r = 5µs and T_f = 5µs

Tunnel Voltage (volts)	Vfg before pulse fall (volts)
10	0.826
10.1	0.831
10.2	0.84
10.3	0.851
10.4	0.867
10.5	0.889
10.6	0.918
10.7	0.955
10.8	1
10.9	1.06
11	1.12
11.1	1.19
11.2	1.27
11.3	1.35
11.4	1.43
11.5	1.52
11.6	1.62
11.7	1.71
11.8	1.81
11.9	1.9
12	2
12.1	2.1
12.2	2.2
12.3	2.3
12.4	2.4
12.5	2.5



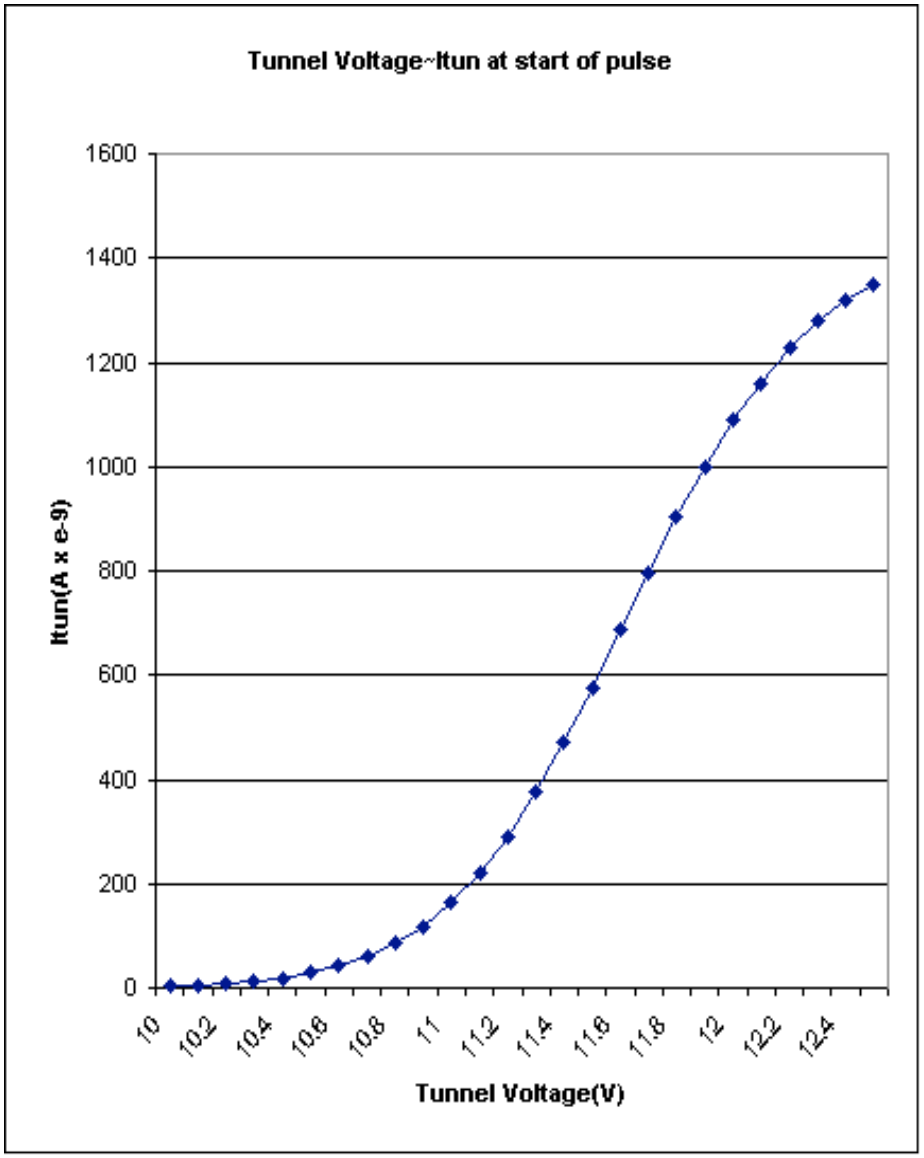
QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 1
Fig.8.3.1.3. V_c = 0.8V, V_{ds} = V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 10 – 12.5V in steps of 0.1V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

Tunnel Voltage (volts)	Vfg after pulse fall (volts)
10	0.809
10.1	0.815
10.2	0.823
10.3	0.834
10.4	0.85
10.5	0.872
10.6	0.901
10.7	0.938
10.8	0.983
10.9	1.04
11	1.1
11.1	1.17
11.2	1.25
11.3	1.33
11.4	1.42
11.5	1.51
11.6	1.6
11.7	1.69
11.8	1.79
11.9	1.88
12	1.98
12.1	2.08
12.2	2.18
12.3	2.28
12.4	2.38
12.5	2.48



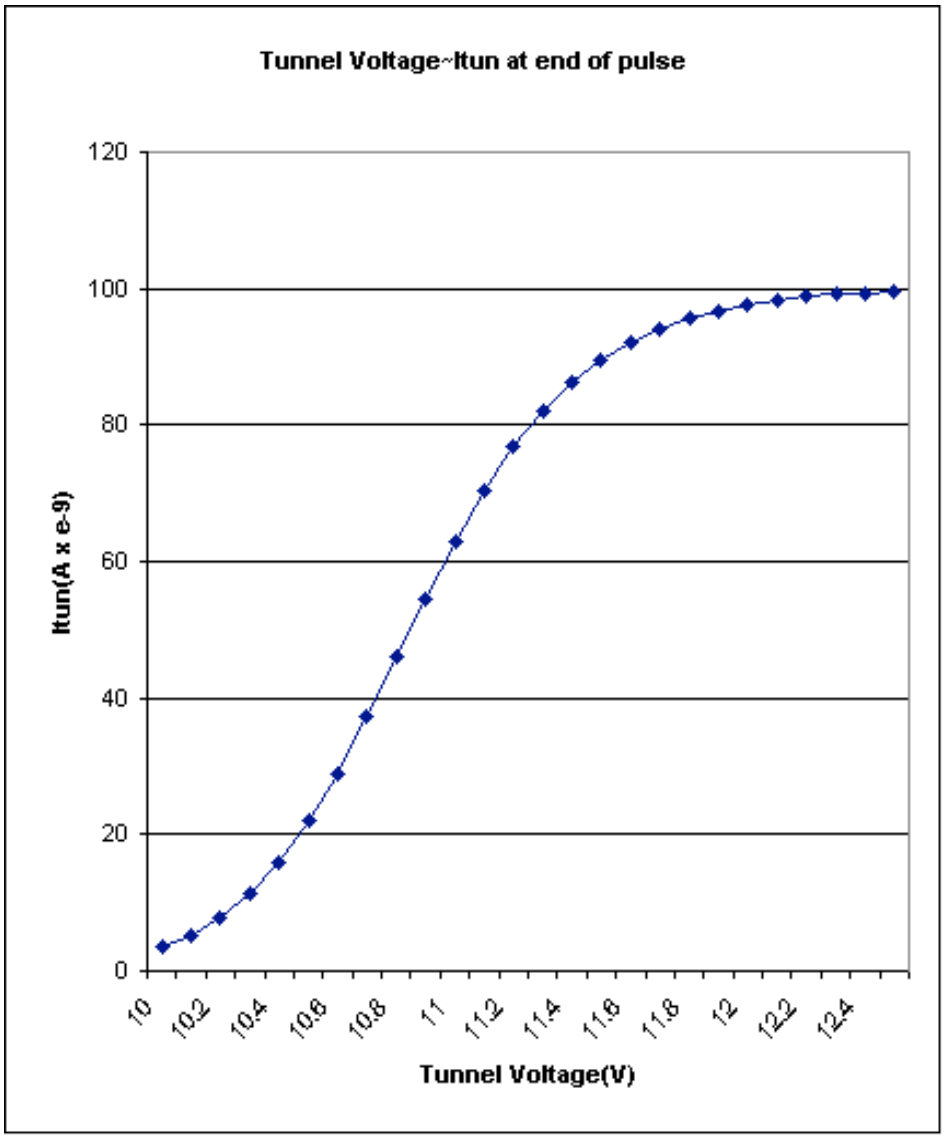
QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 1
Fig.8.3.1.4. V_c = 0.8V, V_{ds} = 2V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 10 – 12.5V in steps of 0.1V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

Tunnel Voltage (volts)	Itun at start of pulse during pulse x e-9(A)
10	3.68
10.1	5.65
10.2	8.59
10.3	12.9
10.4	19.3
10.5	28.4
10.6	41.4
10.7	59.6
10.8	84.6
10.9	117
11	163
11.1	220
11.2	291
11.3	375
11.4	471
11.5	577
11.6	686
11.7	797
11.8	903
11.9	1000
12	1090
12.1	1160
12.2	1230
12.3	1280
12.4	1320
12.5	1350



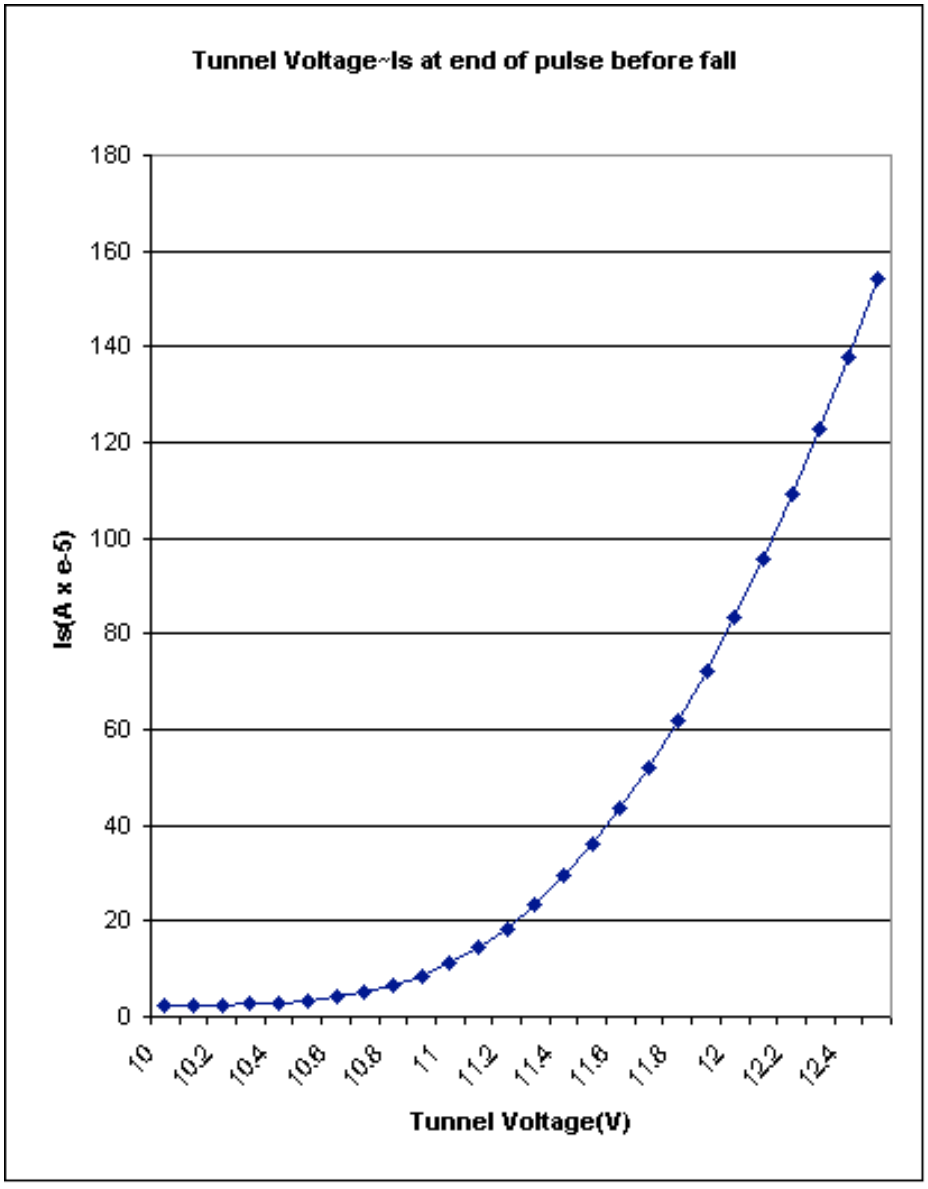
QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 1
Fig.8.3.1.5. V_c = 0.8V, V_{ds} = 2V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 10 – 12.5V in steps of 0.1V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

Tunnel Voltage (volts)	Itun during pulse end of pulse x e-9(A)
10	3.53
10.1	5.31
10.2	7.85
10.3	11.3
10.4	16
10.5	21.9
10.6	29
10.7	37.2
10.8	45.9
10.9	54.6
11	62.9
11.1	70.4
11.2	76.8
11.3	82.1
11.4	86.3
11.5	89.6
11.6	92.2
11.7	94.1
11.8	95.6
11.9	96.8
12	97.6
12.1	98.3
12.2	98.8
12.3	99.1
12.4	99.4
12.5	99.6



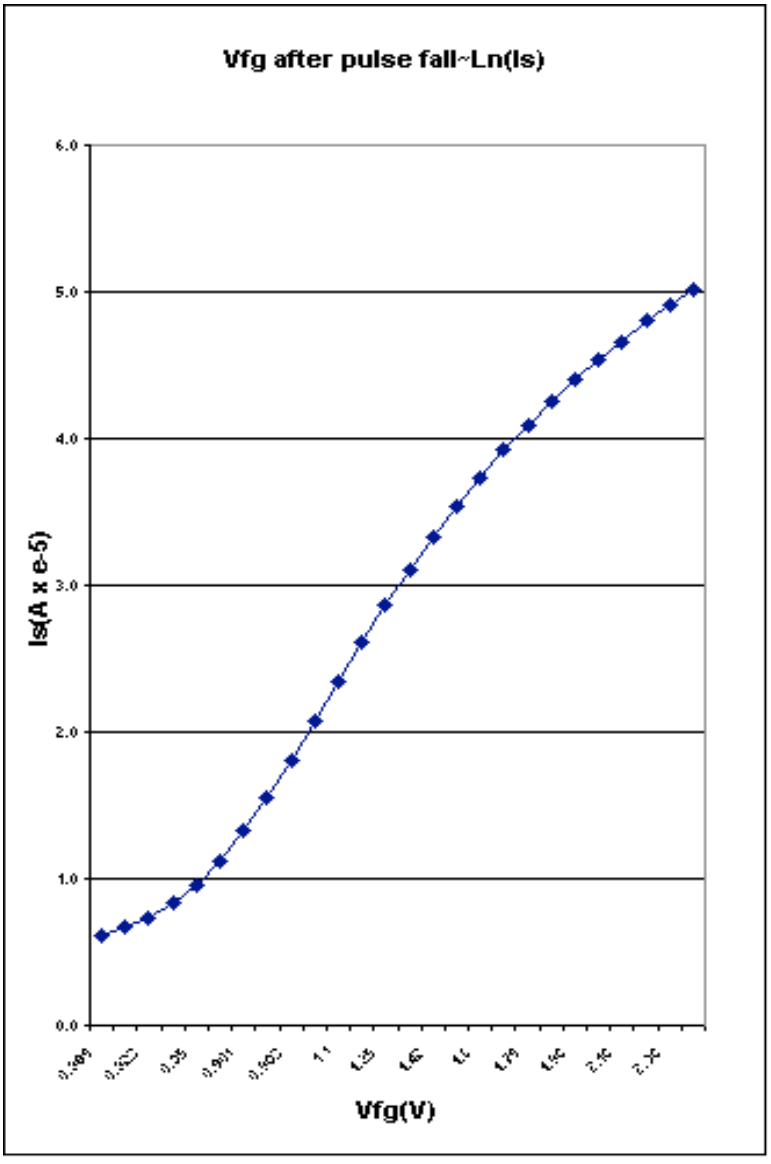
QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 1
Fig.8.3.1.6. V_c = 0.8V, V_{ds} = 2V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 10 – 12.5V in steps of 0.1V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

Tunnel Voltage (volts)	Is at end of pulse before fall x e-5(A)
10	2.14
10.1	2.25
10.2	2.4
10.3	2.63
10.4	2.97
10.5	3.47
10.6	4.19
10.7	5.22
10.8	6.65
10.9	8.6
11	11.2
11.1	14.4
11.2	18.5
11.3	23.4
11.4	29.3
11.5	36
11.6	43.6
11.7	52.2
11.8	61.7
11.9	72.2
12	83.5
12.1	95.7
12.2	109
12.3	123
12.4	138
12.5	154



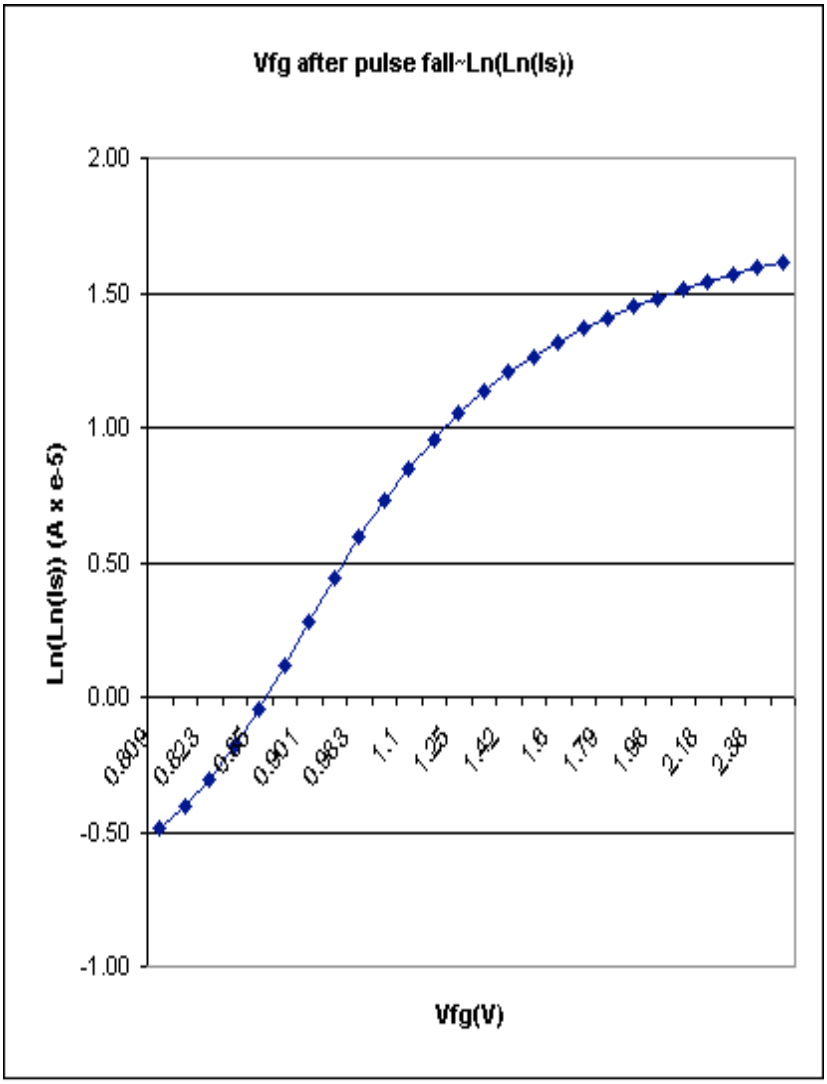
QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 1
Fig.8.3.1.7. V_c = 0.8V, V_{ds} = 2V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 10 – 12.5V in steps of 0.1V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

Vfg after pulse fall (volts)	Is after pusle removed x e-5(A)	Ln(Is) x e-5(A)	Ln(Ln(Is)) x e-5(A)
0.809	1.85	0.6152	-0.4858
0.815	1.95	0.6678	-0.4037
0.823	2.09	0.7372	-0.3049
0.834	2.3	0.8329	-0.1828
0.85	2.61	0.9594	-0.0415
0.872	3.07	1.1217	0.1148
0.901	3.75	1.3218	0.2790
0.938	4.72	1.5518	0.4394
0.983	6.08	1.8050	0.5906
1.04	7.94	2.0719	0.7285
1.1	10.4	2.3418	0.8509
1.17	13.6	2.6101	0.9594
1.25	17.5	2.8622	1.0516
1.33	22.3	3.1046	1.1329
1.42	28	3.3322	1.2036
1.51	34.6	3.5439	1.2652
1.6	42	3.7377	1.3185
1.69	50.5	3.9220	1.3666
1.79	59.8	4.0910	1.4088
1.88	70	4.2485	1.4466
1.98	81.2	4.3969	1.4809
2.08	93.3	4.5358	1.5120
2.18	106	4.6634	1.5398
2.28	123	4.8122	1.5712
2.38	135	4.9053	1.5903
2.48	150	5.0106	1.6116



QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 1
Fig.8.3.1.8. V_c = 0.8V, V_{ds} = 2V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 10 – 12.5V in steps of 0.1V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

Vfg after pulse fall (volts)	Is after pusle removed A x e-5	Ln(Is) A x e-5	Ln(Ln(Is)) A x e-5
0.809	1.85	0.6152	-0.4858
0.815	1.95	0.6678	-0.4037
0.823	2.09	0.7372	-0.3049
0.834	2.3	0.8329	-0.1828
0.85	2.61	0.9594	-0.0415
0.872	3.07	1.1217	0.1148
0.901	3.75	1.3218	0.2790
0.938	4.72	1.5518	0.4394
0.983	6.08	1.8050	0.5906
1.04	7.94	2.0719	0.7285
1.1	10.4	2.3418	0.8509
1.17	13.6	2.6101	0.9594
1.25	17.5	2.8622	1.0516
1.33	22.3	3.1046	1.1329
1.42	28	3.3322	1.2036
1.51	34.6	3.5439	1.2652
1.6	42	3.7377	1.3185
1.69	50.5	3.9220	1.3666
1.79	59.8	4.0910	1.4088
1.88	70	4.2485	1.4466
1.98	81.2	4.3969	1.4809
2.08	93.3	4.5358	1.5120
2.18	106	4.6634	1.5398
2.28	123	4.8122	1.5712
2.38	135	4.9053	1.5903
2.48	150	5.0106	1.6116



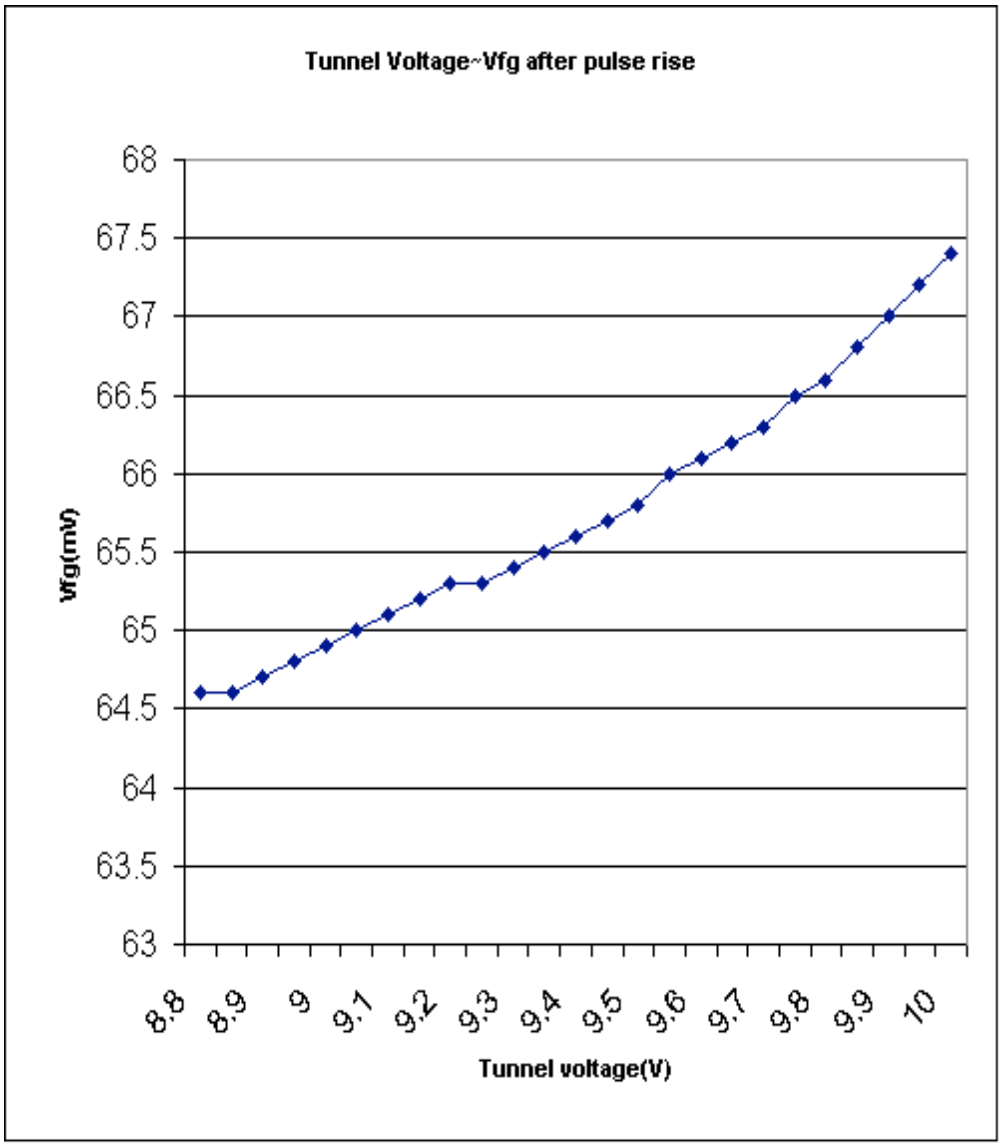
8.3.1.2. Summary of Series (1)

Results for Series (1): Vgs above threshold and Vds above saturation with Fowler-Nordheim voltage set between 10 – 12.5V in order to effect tunnelling. Initially the floating gate voltages until Fowler-Nordheim becomes more active at approximately 11.5V. During the 0.5ms duration of the tunnel pulse the floating gate voltage increases as anticipated. For the test circuit the contact voltage was already set above the threshold and was sufficient for saturation. From the simulation the results obtained it can be seen that even with the contact voltage set to 0V after a tunnelling pulse of 11V for 0.5ms then the floating gate could start to create a inversion layer and enter into the linear region. Also noted was that with a tunnelling pulse for 0.5ms at approximately 12V the floating gate device was entering into saturation.

8.3.2.1. Series (2)

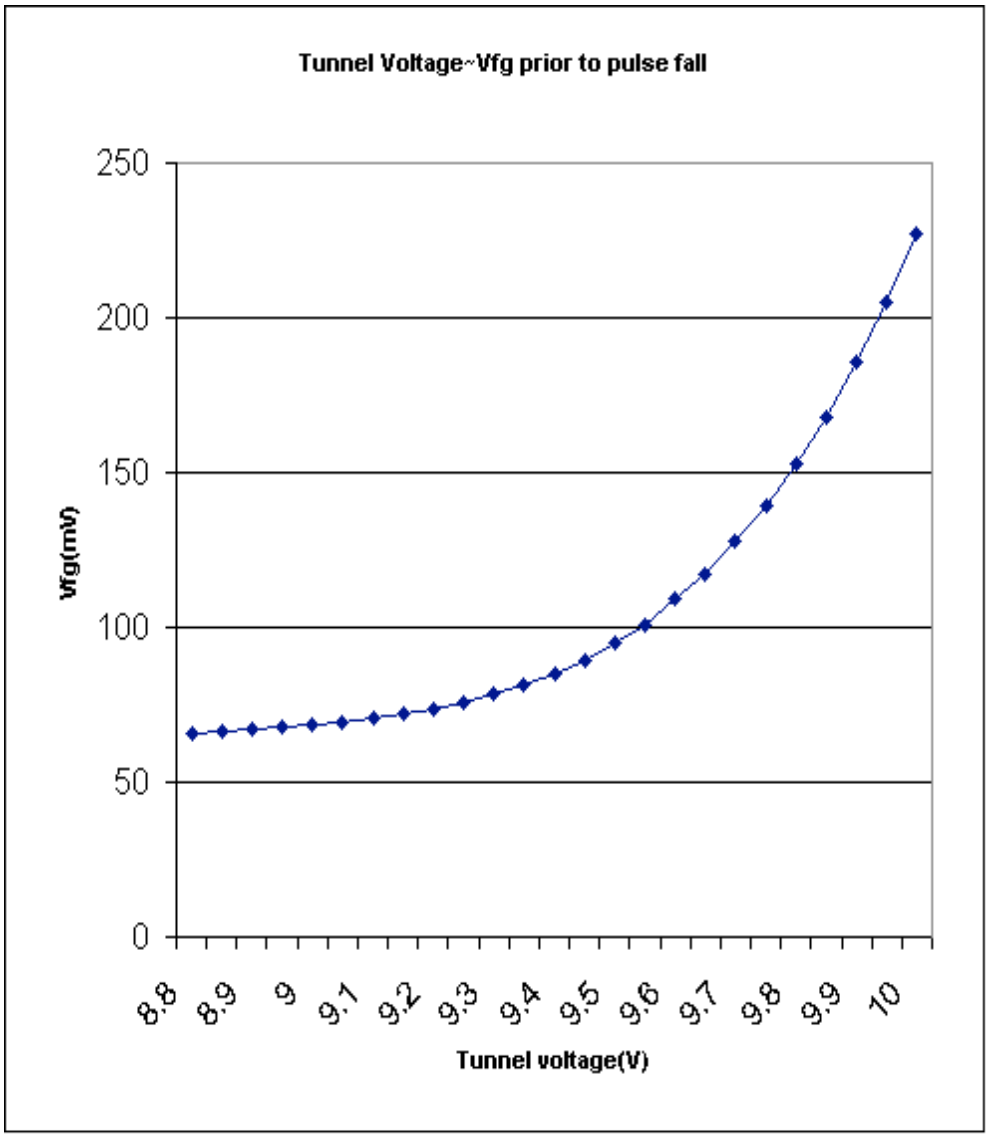
QUCS Simulation data for floating gate MOS device based on EKV v2.6
Series 2
Fig.8.3.2.1. V_c = 0.05V, V_{ds} = 0.1V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 8.8 – 10V in steps of 0.05V.
Total pulse duration = 50µs, T_r = 5µs and T_f = 5µs

Tunnel Voltage (Volts)	Vfg after pulse rise (mV)
8.8	64.6
8.85	64.6
8.9	64.7
8.95	64.8
9	64.9
9.05	65
9.1	65.1
9.15	65.2
9.2	65.3
9.25	65.3
9.3	65.4
9.35	65.5
9.4	65.6
9.45	65.7
9.5	65.8
9.55	66
9.6	66.1
9.65	66.2
9.7	66.3
9.75	66.5
9.8	66.6
9.85	66.8
9.9	67
9.95	67.2
10	67.4



QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Fig.8.3.2.2. V_c = 0.05V, V_{ds} = 0.1V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 8.8 – 10V in steps of 0.05V.
Total pulse duration = 50µs, T_r = 5µs and T_f = 5µs

Tunnel Voltage (volts)	Vfg before pulse fall
(Volts)	(mV)
8.8	65.9
8.85	66.4
8.9	66.9
8.95	67.6
9	68.4
9.05	69.3
9.1	70.5
9.15	72
9.2	73.7
9.25	75.8
9.3	78.4
9.35	81.5
9.4	85.2
9.45	89.6
9.5	94.9
9.55	101
9.6	109
9.65	117
9.7	128
9.75	139
9.8	153
9.85	168
9.9	186
9.95	205
10	227

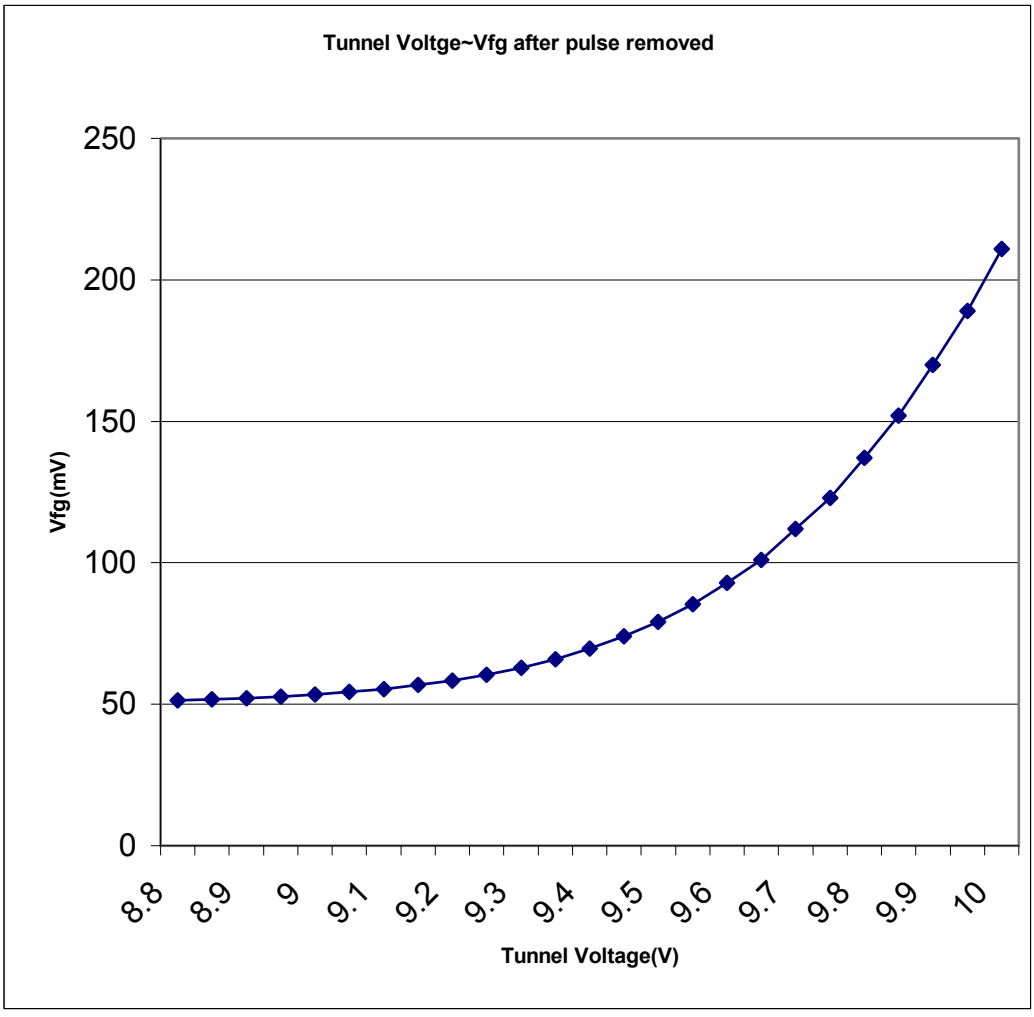


QUCS Simulation data for floating gate MOS device based on EKV v 2.6

Series 2

Fig.8.3.2.3. V_c = 0.05V, V_{ds} = 0.1V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 8.8 – 10V in steps of 0.05V.
Total pulse duration = 50µs, T_r = 5µs and T_f = 5µs

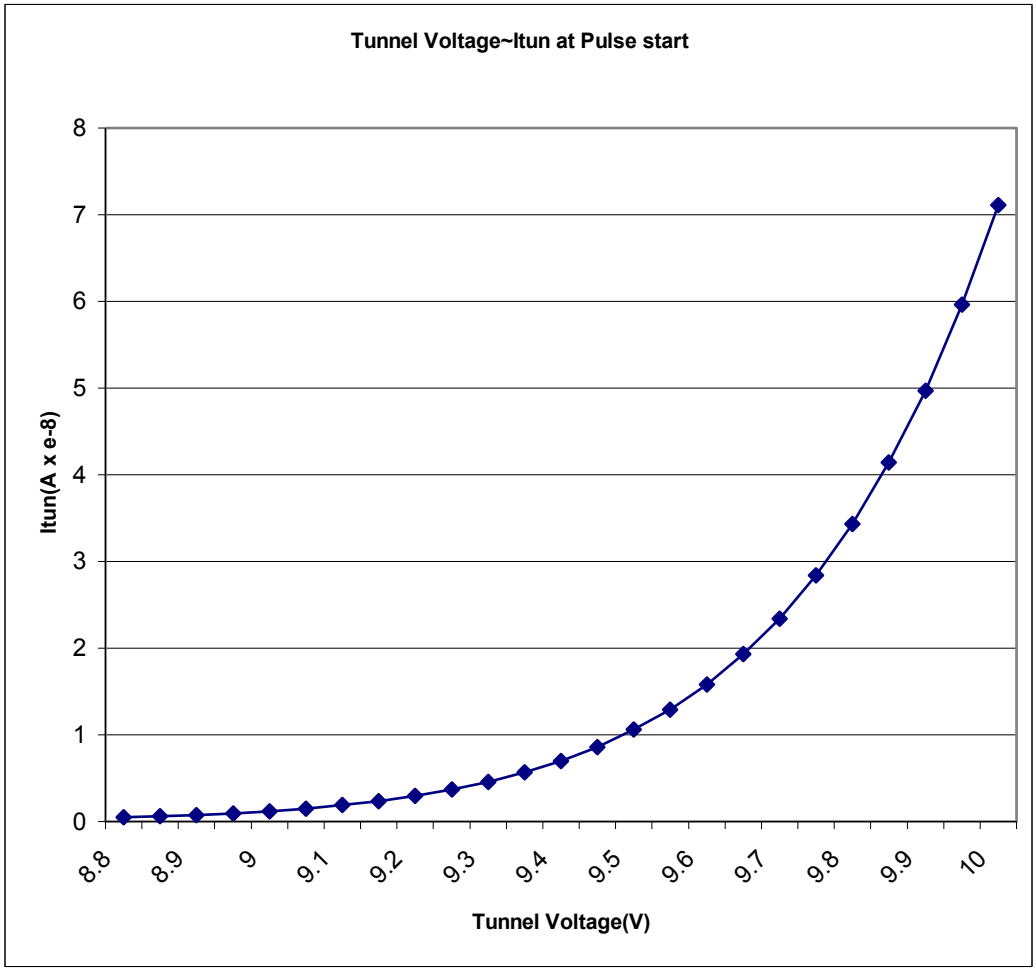
Tunnel Voltage (Volts)	Vfg after pulse fall (mV)
8.8	51.3
8.85	51.7
8.9	52.1
8.95	52.7
9	53.4
9.05	54.3
9.1	55.4
9.15	56.8
9.2	58.4
9.25	60.5
9.3	62.9
9.35	65.9
9.4	69.6
9.45	74
9.5	79.2
9.55	85.4
9.6	92.89
9.65	101
9.7	112
9.75	123
9.8	137
9.85	152
9.9	170
9.95	189
10	211



QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 2
Fig.8.3.2.4. V_c = 0.05V, V_{ds} = 0.1V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 8.8 – 10V in steps of 0.05V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

start

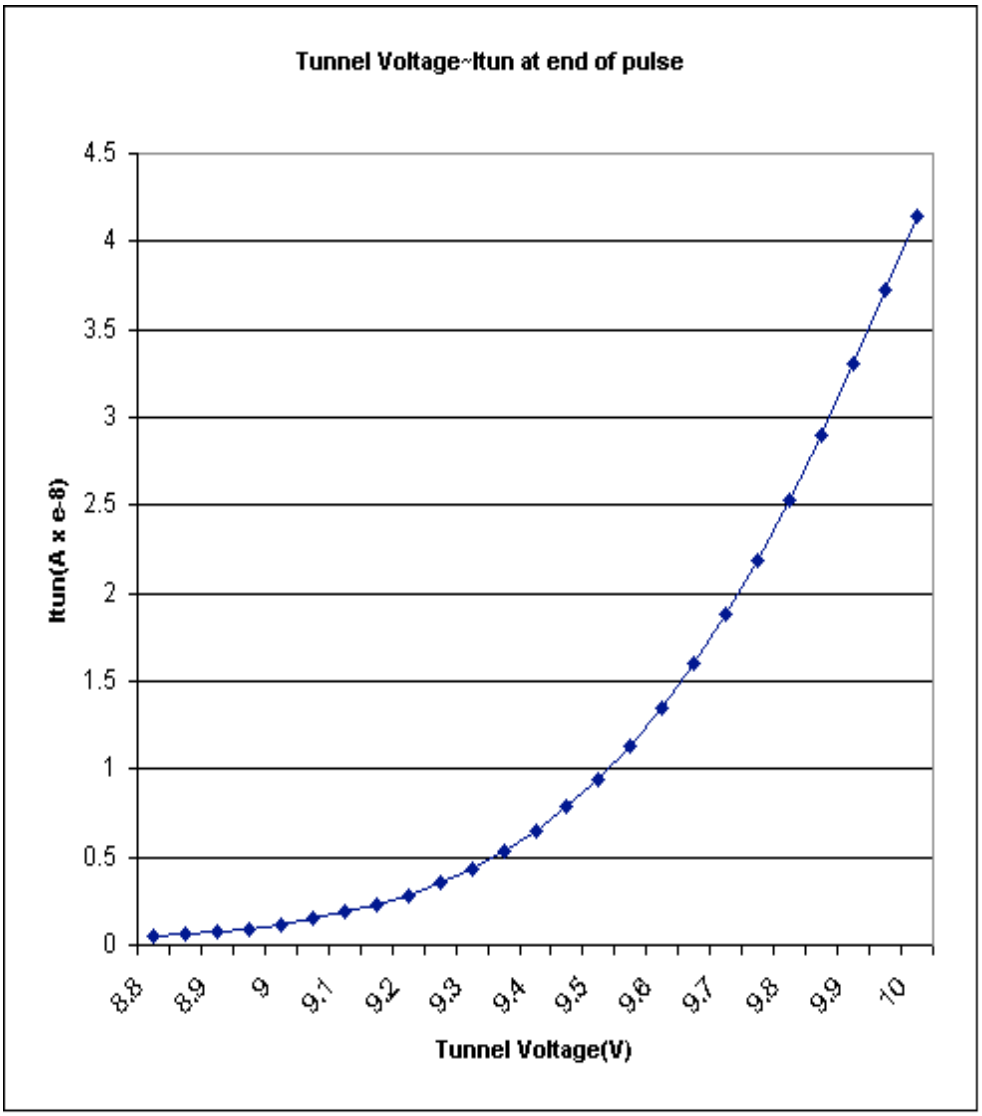
Tunnel Voltage (Volts)	Itun during pulse xe-8(A)
8.8	0.047
8.85	0.0597
8.9	0.0757
8.95	0.0956
9	0.12
9.05	0.151
9.1	0.19
9.15	0.237
9.2	0.296
9.25	0.368
9.3	0.457
9.35	0.565
9.4	0.698
9.45	0.859
9.5	1.06
9.55	1.29
9.6	1.58
9.65	1.93
9.7	2.34
9.75	2.84
9.8	3.43
9.85	4.14
9.9	4.97
9.95	5.96
10	7.11



QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 2
Fig.8.3.2.5. V_c = 0.05V, V_{ds} = 0.1V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 8.8 – 10V in steps of 0.05V.
Total pulse duration = 50µs, T_r = 5µs and T_f = 5µs

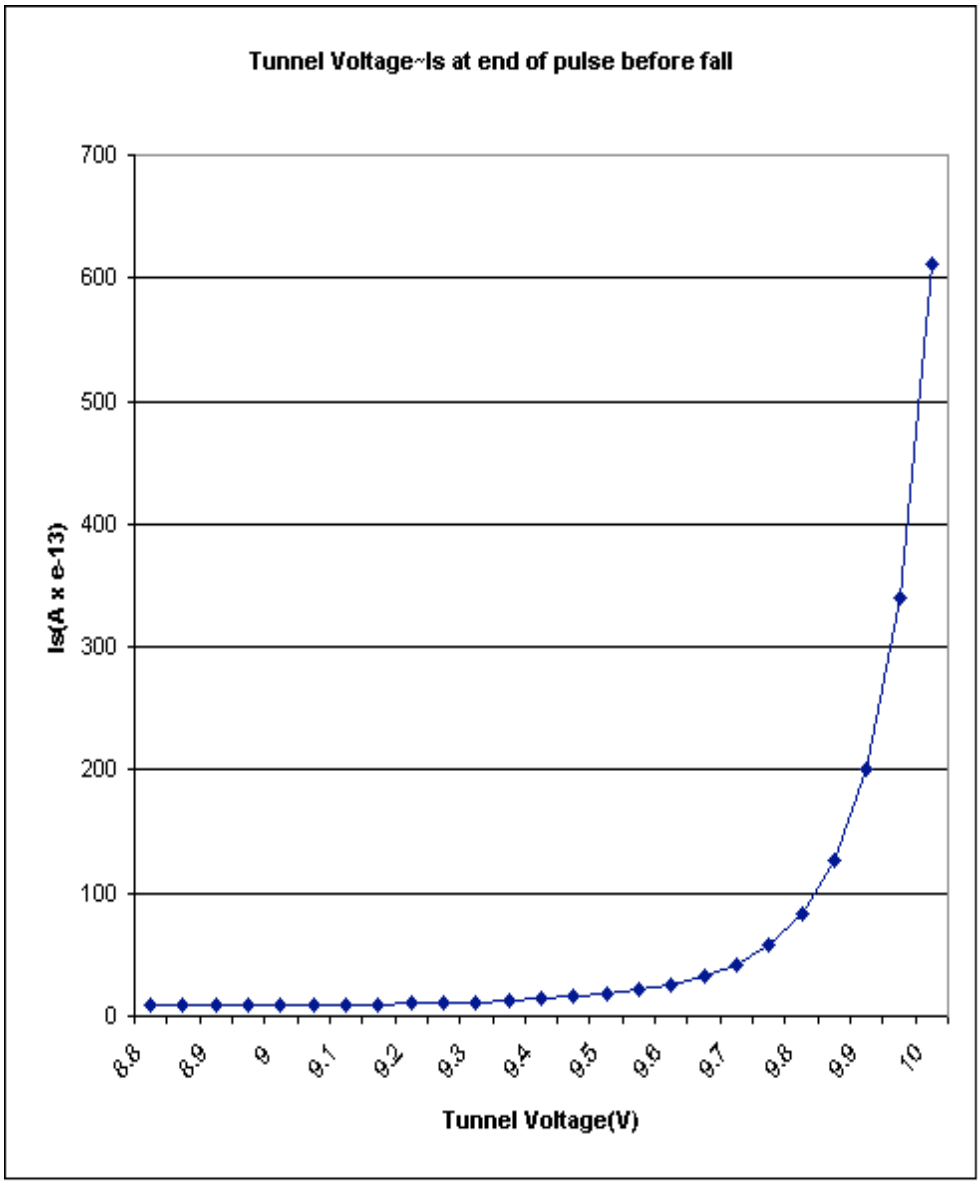
end

Tunnel Voltage (Volts)	Itun during pulse xe-8(A)
8.8	0.0467
8.85	0.0593
8.9	0.075
8.95	0.0945
9	0.119
9.05	0.149
9.1	0.186
9.15	0.231
9.2	0.286
9.25	0.353
9.3	0.434
9.35	0.531
9.4	0.647
9.45	0.785
9.5	0.946
9.55	1.13
9.6	1.35
9.65	1.6
9.7	1.88
9.75	2.19
9.8	2.53
9.85	2.9
9.9	3.3
9.95	3.72
10	4.15



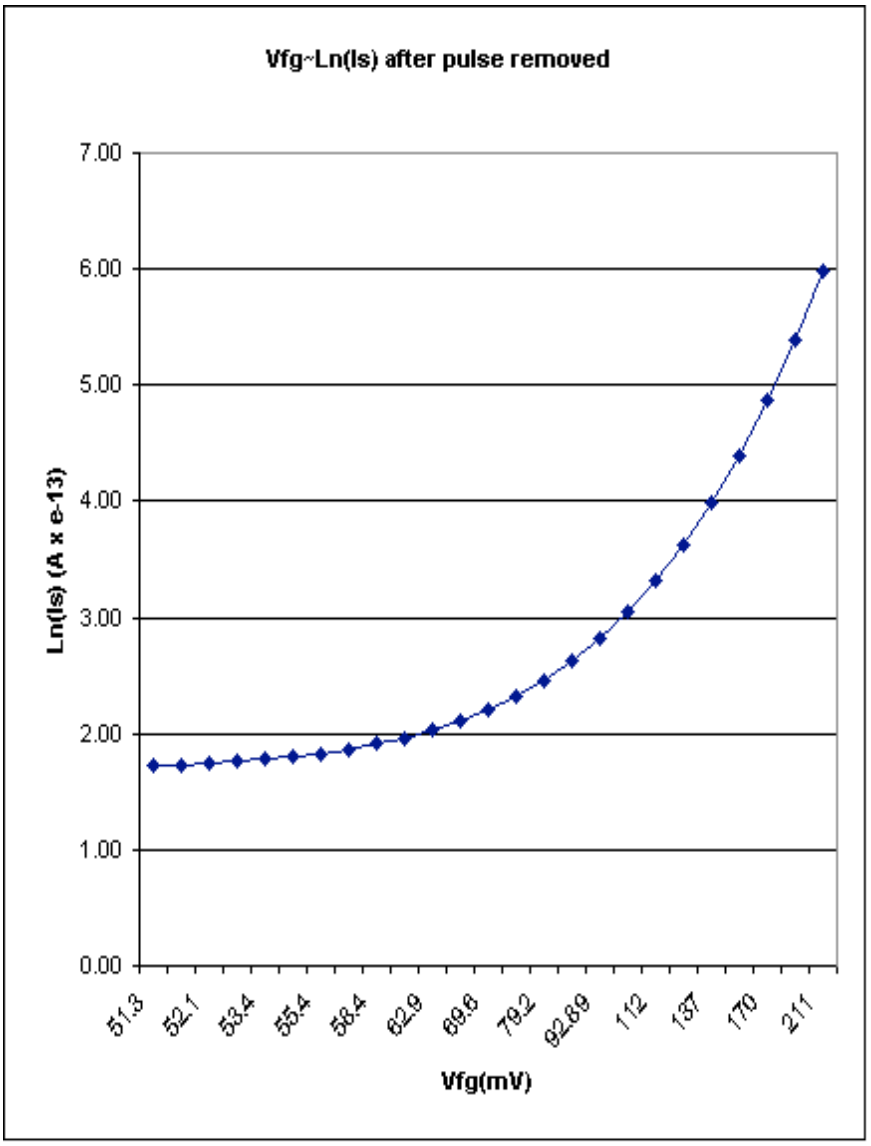
QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 2
Fig.8.3.2.6. V_c = 0.05V, V_{ds} = 0.1V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 8.8 – 10V in steps of 0.05V.
Total pulse duration = 50µs, T_r = 5µs and T_f = 5µs

Tunnel Voltage (Volts)	Is at end of pulse before fall xe-13(A)
8.8	8.234
8.85	8.33
8.9	8.45
8.95	8.6
9	8.78
9.05	9.01
9.1	9.29
9.15	9.65
9.2	10.1
9.25	10.7
9.3	11.4
9.35	12.5
9.4	13.7
9.45	15.4
9.5	17.7
9.55	20.9
9.6	25.5
9.65	32.2
9.7	42.2
9.75	57.8
9.8	83
9.85	126
9.9	201
9.95	340
10	611



QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 2
Fig.8.3.2.7. V_c = 0.05V, V_{ds} = 0.1V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 8.8 – 10V in steps of 0.05V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

Vfg after pulse fall (mV)	Is after pusle removed xe-13(A)	Ln(Is) xe-13(A)
51.3	5.59	1.721
51.7	5.65	1.732
52.1	5.72	1.744
52.7	5.8	1.758
53.4	5.91	1.777
54.3	6.06	1.802
55.4	6.23	1.829
56.8	6.46	1.866
58.4	6.75	1.910
60.5	7.12	1.963
62.9	7.6	2.028
65.9	8.23	2.108
69.6	9.06	2.204
74	10.2	2.322
79.2	11.7	2.460
85.4	13.8	2.625
92.89	16.8	2.821
101	21.1	3.049
112	27.6	3.318
123	37.7	3.630
137	54	3.989
152	81.5	4.401
170	130	4.868
189	220	5.394
211	394	5.976



8.3.2.2. Summary of Series (2)

Results for Series (2): For the plot of tunnel voltage against floating gate voltage there is a small positive rise indicating that the system is below Fowler-Nordheim tunnelling. However as larger voltage pulses are applied some tunnelling takes place and there is charge accumulation on the floating gate. After the pulse is removed the floating gate remains high and for a 10V pulse was set at just over 200mV.

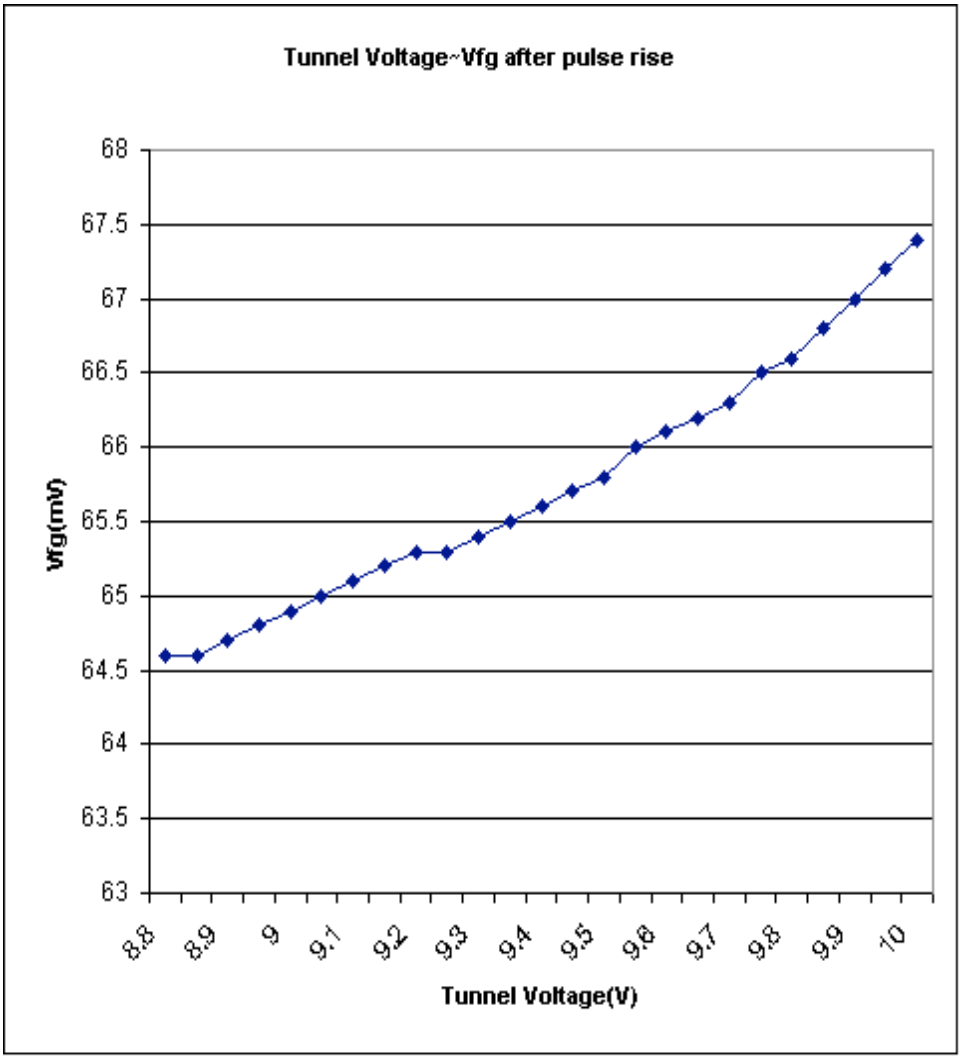
For the tunnelling current, this is low at low voltage but gradually takes effect. At higher pulse voltage values this increase takes place more rapidly, almost implying a square law relationship. This continues throughout the duration of the pulse although at a lesser level at the end of the pulse.

The drain-source current is extremely small as would be expected (10^{-13}A), although there is a rapid increase around 9.95V when the Fowler-Nordheim mechanism is starting to operate. This is probably due to a sudden transient change in the field, when the floating gate voltage reaches 150mV.

8.3.3.1. Series (3)

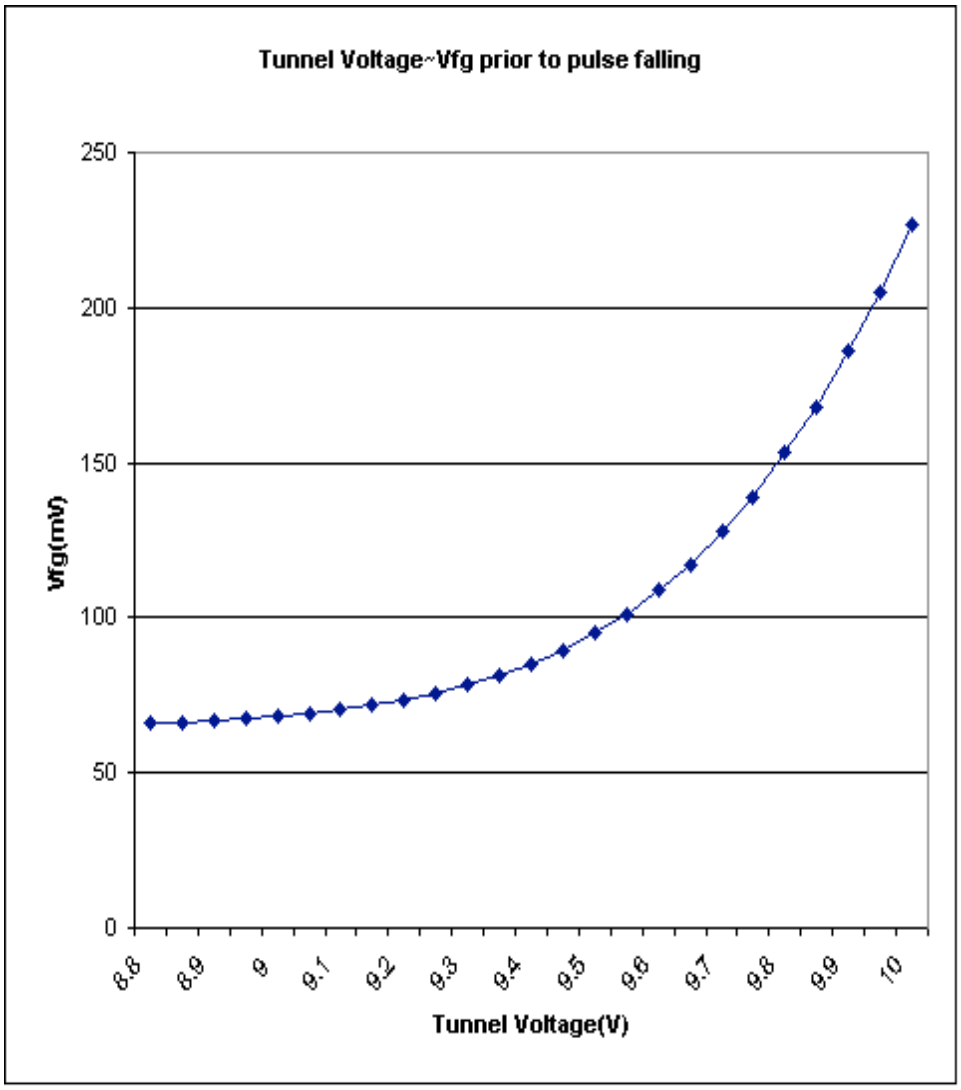
QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 3
Fig.8.3.3.1. V_c = 0.05V, V_{ds} = 2V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 8.8 – 10V in steps of 0.05V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

Tunnel Voltage (Volts)	Vfg after pulse rise (mV)
8.8	64.6
8.85	64.6
8.9	64.7
8.95	64.8
9	64.9
9.05	65
9.1	65.1
9.15	65.2
9.2	65.3
9.25	65.3
9.3	65.4
9.35	65.5
9.4	65.6
9.45	65.7
9.5	65.8
9.55	66
9.6	66.1
9.65	66.2
9.7	66.3
9.75	66.5
9.8	66.6
9.85	66.8
9.9	67
9.95	67.2
10	67.4



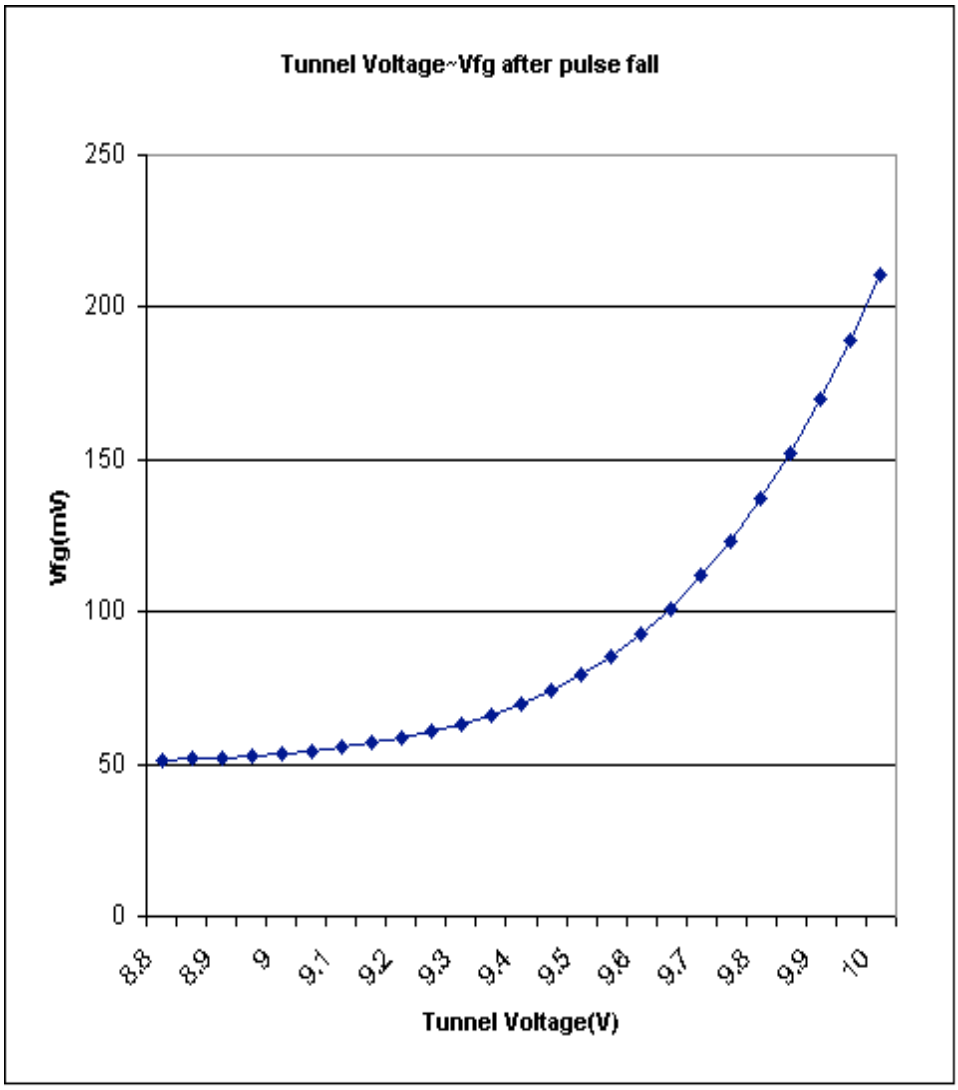
QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 3
Fig.8.3.3.2. V_c = 0.05V, V_{ds} = 2V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 8.8 – 10V in steps of 0.05V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

Tunnel Voltage (Volts)	Vfg before pulse fall (mV)
8.8	65.9
8.85	66.4
8.9	66.9
8.95	67.6
9	68.4
9.05	69.3
9.1	70.5
9.15	72
9.2	73.7
9.25	75.8
9.3	78.4
9.35	81.5
9.4	85.2
9.45	89.6
9.5	94.9
9.55	101
9.6	109
9.65	117
9.7	128
9.75	139
9.8	153
9.85	168
9.9	186
9.95	205
10	227



QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 3
Fig.8.3.3.3. V_c = 0.5V, V_{ds} = 2V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 8.8 – 10V in steps of 0.05V.
Total pulse duration = 50µs, T_r = 5µs and T_f = 5µs

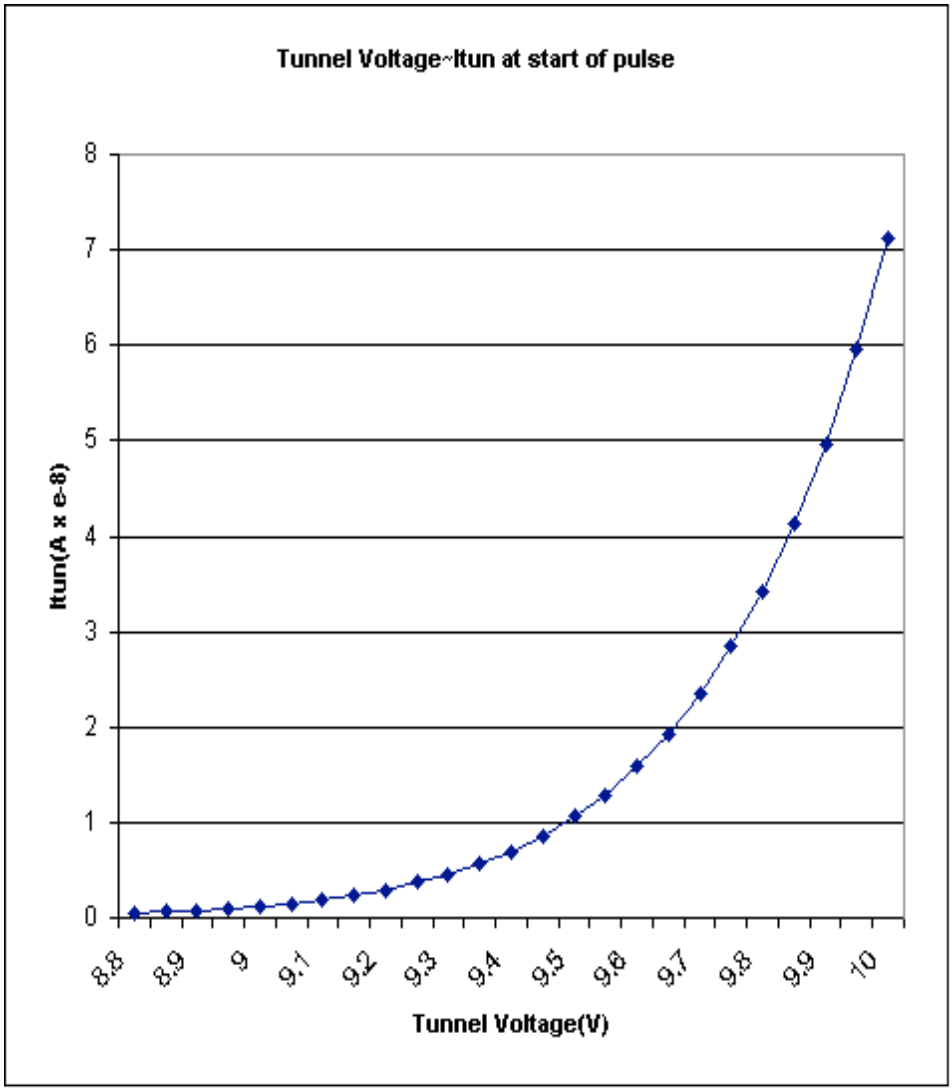
Tunnel Voltage (Volts)	Vfg after pulse fall (mV)
8.8	51.3
8.85	51.7
8.9	52.1
8.95	52.7
9	53.4
9.05	54.3
9.1	55.4
9.15	56.8
9.2	58.4
9.25	60.5
9.3	62.9
9.35	65.9
9.4	69.6
9.45	74
9.5	79.2
9.55	85.4
9.6	92.8
9.65	101
9.7	112
9.75	123
9.8	137
9.85	152
9.9	170
9.95	189
10	211



QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 3
Fig.8.3.3.4. V_c = 0.5V, V_{ds} = 2V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 8.8 – 10V in steps of 0.05V.
Total pulse duration = 50µs, T_r = 5µs and T_f = 5µs

start of pulse

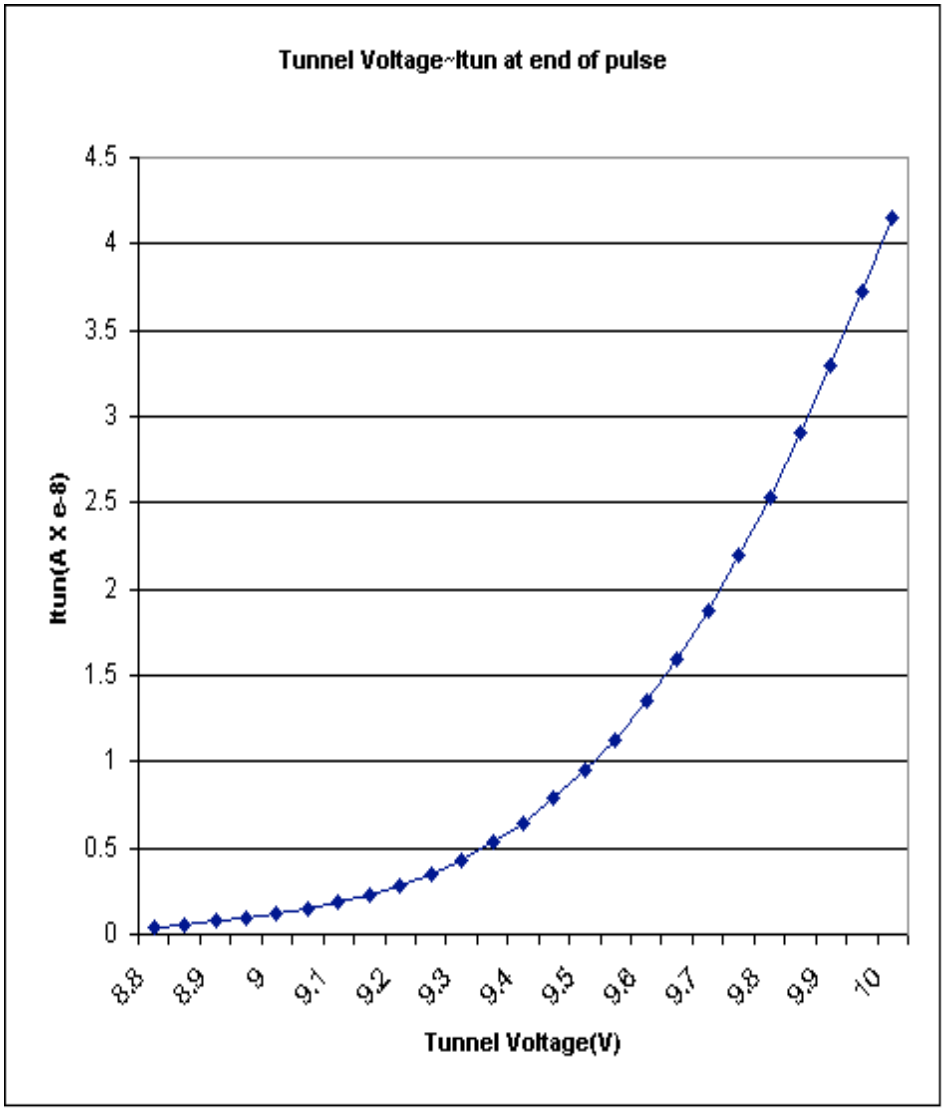
Tunnel Voltage (Volts)	Itun during pulse x e-8(A)
8.8	0.047
8.85	0.0597
8.9	0.0757
8.95	0.0956
9	0.12
9.05	0.151
9.1	0.19
9.15	0.237
9.2	0.296
9.25	0.368
9.3	0.457
9.35	0.565
9.4	0.698
9.45	0.859
9.5	1.06
9.55	1.29
9.6	1.58
9.65	1.93
9.7	2.34
9.75	2.84
9.8	3.43
9.85	4.14
9.9	4.97
9.95	5.96
10	7.11



QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 3
Fig.8.3.3.5. V_c = 0.5V, V_{ds} = 2V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 8.8 – 10V in steps of 0.05V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

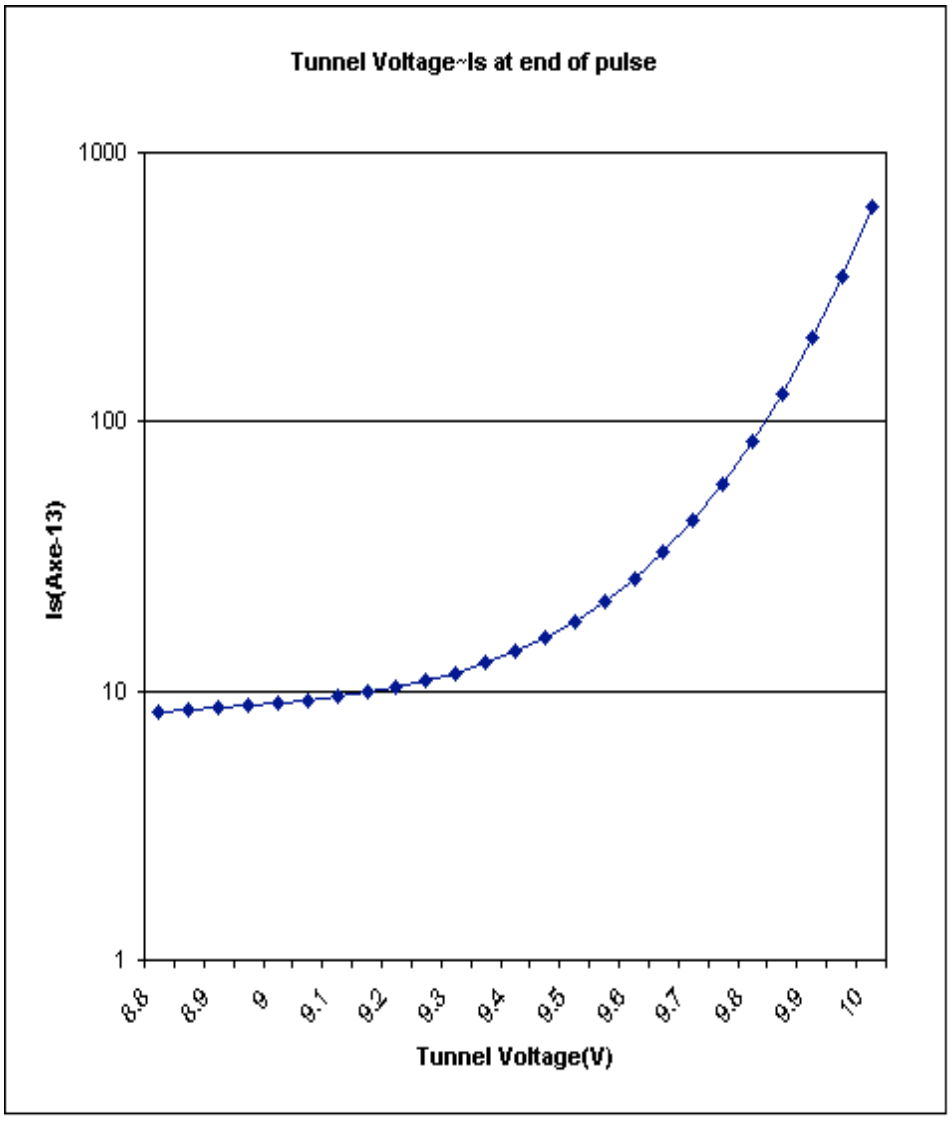
end of pulse

Tunnel Voltage (Volts)	Itun during pulse x e-8(A)
8.8	0.0467
8.85	0.0593
8.9	0.075
8.95	0.0945
9	0.119
9.05	0.149
9.1	0.186
9.15	0.231
9.2	0.286
9.25	0.353
9.3	0.434
9.35	0.531
9.4	0.647
9.45	0.785
9.5	0.946
9.55	1.13
9.6	1.35
9.65	1.6
9.7	1.88
9.75	2.19
9.8	2.53
9.85	2.9
9.9	3.3
9.95	3.72
10	4.15



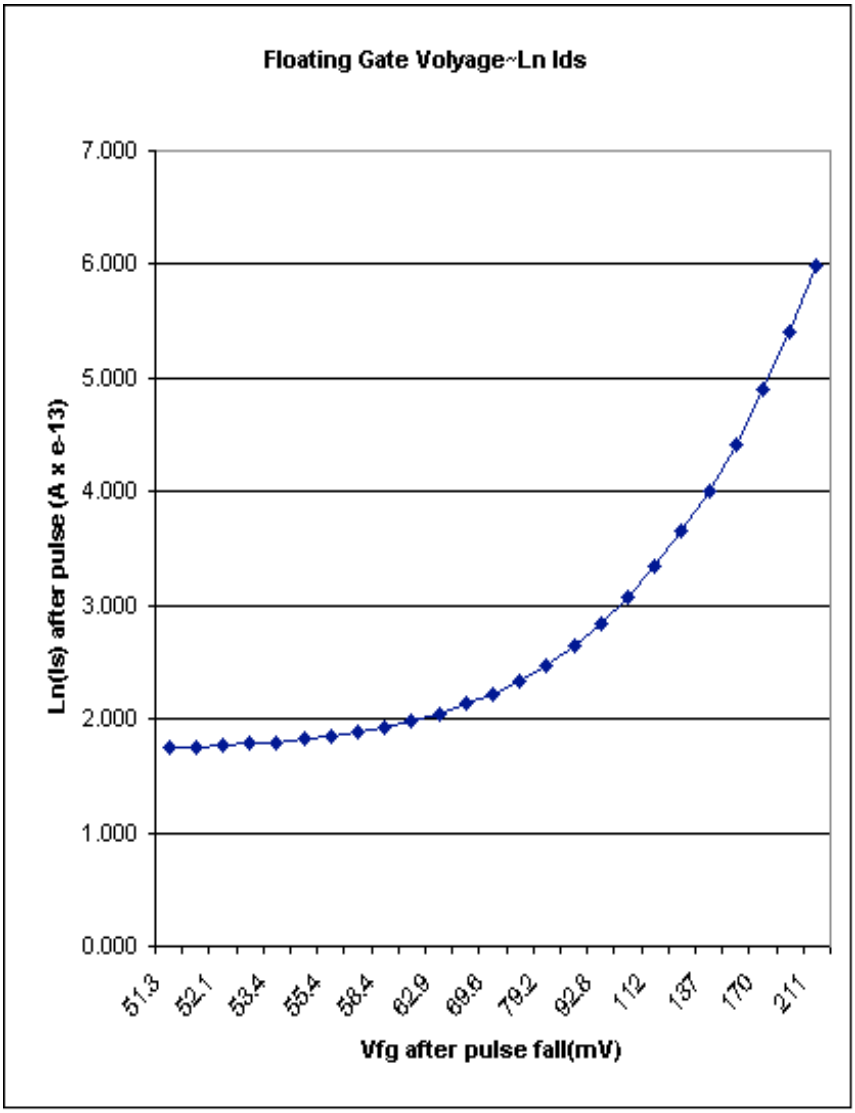
QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 3.
Fig.8.3.3.6. V_c = 0.5V, V_{ds} = 2V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 8.8 – 10V in steps of 0.05V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

Tunnel Voltage (Volts)	Is at end of pulse before fall x e-13(A)
8.8	8.4
8.85	8.51
8.9	8.63
8.95	8.78
9	8.97
9.05	9.2
9.1	9.49
9.15	9.86
9.2	10.3
9.25	10.9
9.3	11.7
9.35	12.7
9.4	14
9.45	15.7
9.5	18.1
9.55	21.4
9.6	26.1
9.65	32.9
9.7	43.1
9.75	59.1
9.8	84.9
9.85	128
9.9	205
9.95	347
10	624



QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 3.
Fig.8.3.3.7. V_c = 0.5V, V_{ds} = 2V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 8.8 – 10V in steps of 0.05V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

Vfg after pulse fall (mV)	Is after pusle removed x e-13(A)	Ln (Is) x e-13(A)
51.3	5.71	1.742
51.7	5.77	1.753
52.1	5.84	1.765
52.7	5.93	1.780
53.4	6.04	1.798
54.3	6.18	1.821
55.4	6.37	1.852
56.8	6.6	1.887
58.4	6.89	1.930
60.5	7.27	1.984
62.9	7.77	2.050
65.9	8.41	2.129
69.6	9.26	2.226
74	10.4	2.342
79.2	11.9	2.477
85.4	14.1	2.646
92.8	17.1	2.839
101	21.5	3.068
112	28.2	3.339
123	38.5	3.651
137	55.2	4.011
152	83.3	4.422
170	133	4.890
189	224	5.412
211	402	5.996



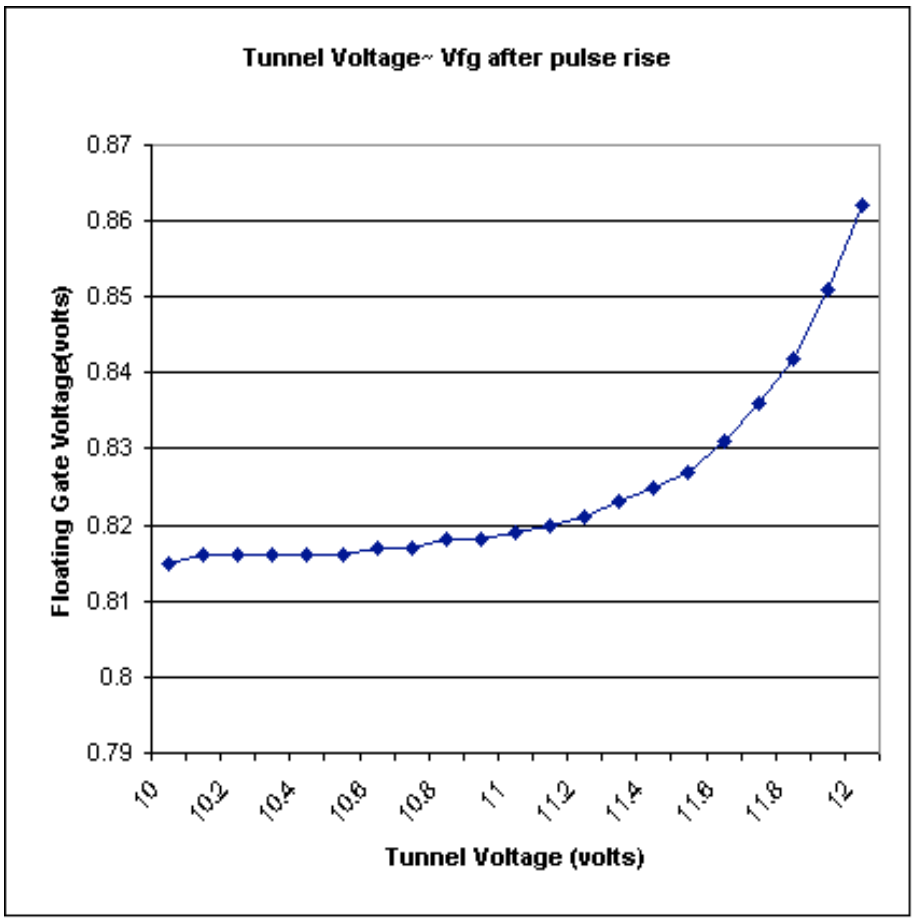
8.3.3.2. Summary of Series (3)

Results for Series (3): This simulation shows the subthreshold region with the contact voltage at 0.05V. Very little tunnelling takes place before the Fowler-Nordheim voltage, from 8.8 – 9.3V. At this stage tunnelling starts to accelerates, typically at 10V at the end of the pulse, the floating gate voltage has increased to 227mV which drops to 221mV after the pulse is removed. These values are reflected in the low levels of the tunnel current. As would be expected the tunnel current is highest at the start of the pulse and reduces at the end of the pulse due to charge accumulation on the floating gate and hence an increase in the floating gate voltage which in turn reduces the Fowler-Nordheim effect. For this simulation the drain-source current is low at low tunnel voltages (8.4xe-13A at V_{tun}=8.8V) however it does reach 624xe-13 at 10V. With a 10V pulse there is an increase in the floating gate voltage of 221mV that would enhance any contact voltage that is applied so shifting the threshold voltage.

8.3.4.1. Series (4)

QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 4.
Fig.8.3.4.1 V_c = 0.8V, V_{ds} = 0.1V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 10 – 12V in steps of 0.1V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

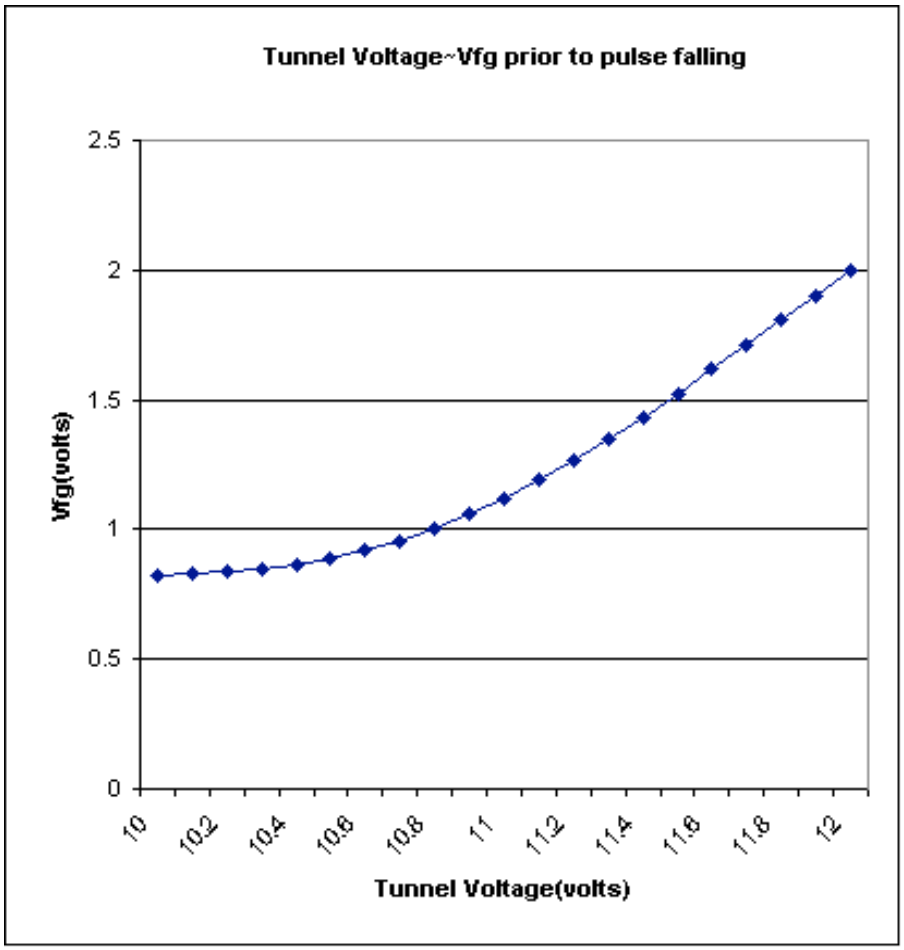
Tunnel Voltage (volts)	Vfg after pulse rise (volts)
10	0.815
10.1	0.816
10.2	0.816
10.3	0.816
10.4	0.816
10.5	0.816
10.6	0.817
10.7	0.817
10.8	0.818
10.9	0.818
11	0.819
11.1	0.82
11.2	0.821
11.3	0.823
11.4	0.825
11.5	0.827
11.6	0.831
11.7	0.836
11.8	0.842
11.9	0.851
12	0.862



QUCS Simulation data for floating gate MOS device based on EKV v 2.6 Series 4.

Fig.8.3.4.2. V_c = 0.8V, V_{ds} = 0.1V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 10 – 12V in steps of 0.1V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

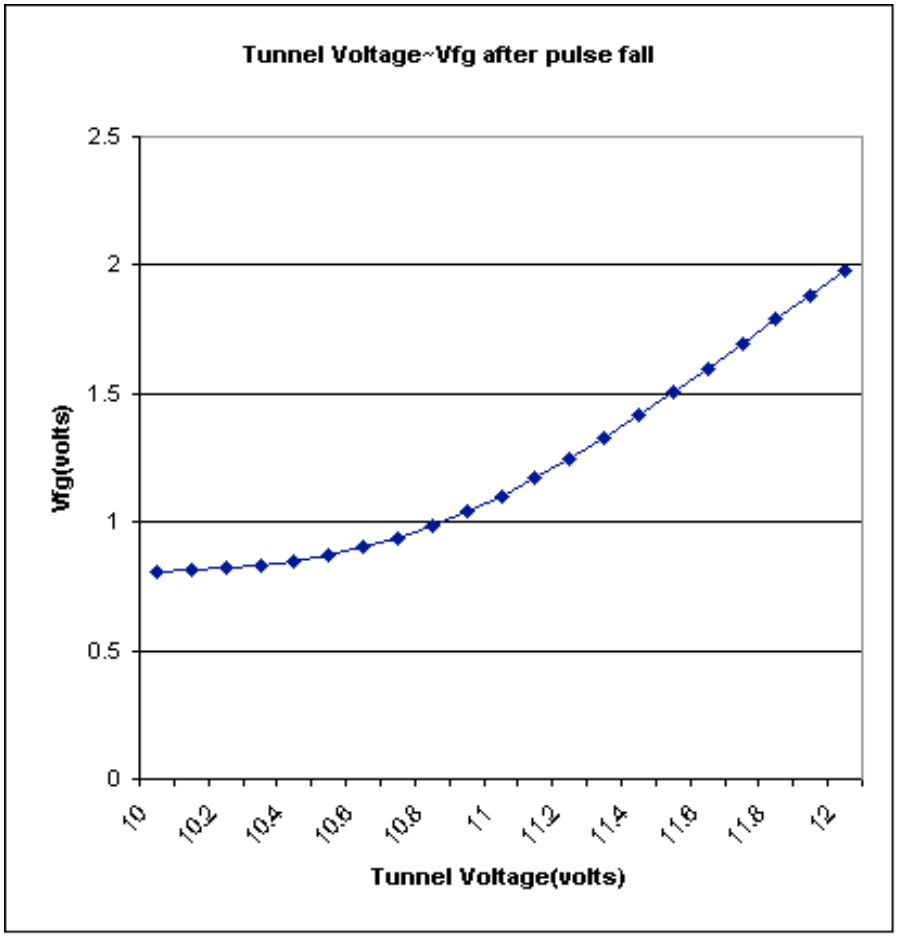
Tunnel Voltage (volts)	Vfg before pulse fall (volts)
10	0.826
10.1	0.831
10.2	0.84
10.3	0.851
10.4	0.867
10.5	0.889
10.6	0.918
10.7	0.955
10.8	1
10.9	1.06
11	1.12
11.1	1.19
11.2	1.27
11.3	1.35
11.4	1.43
11.5	1.52
11.6	1.62
11.7	1.71
11.8	1.81
11.9	1.9
12	2



QUCS Simulation data for floating gate MOS device based on EKV v 2.6 Series 4.

Fig.8.3.4.3. V_c = 0.8V, V_{ds} = 0.1V, T_1 = 0s, T_2 = 0.5ms, T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 10 – 12V in steps of 0.1V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

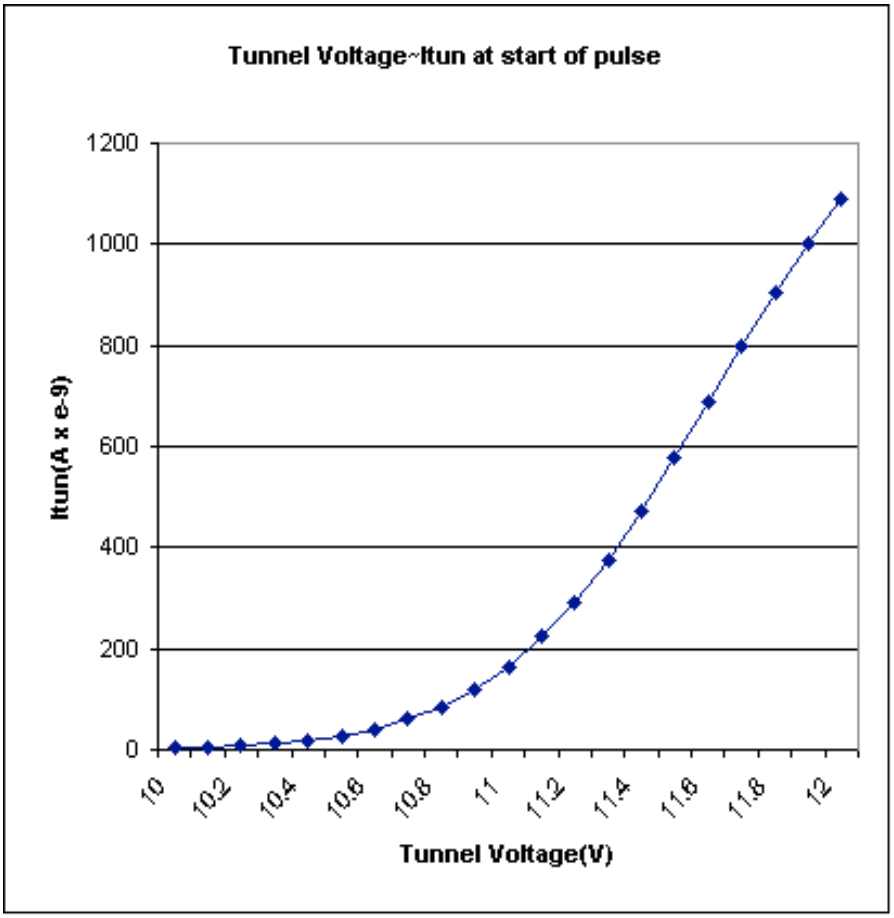
Tunnel Voltage (volts)	Vfg after pulse fall (volts)
10	0.809
10.1	0.815
10.2	0.823
10.3	0.834
10.4	0.85
10.5	0.872
10.6	0.901
10.7	0.938
10.8	0.983
10.9	1.04
11	1.1
11.1	1.17
11.2	1.25
11.3	1.33
11.4	1.42
11.5	1.51
11.6	1.6
11.7	1.69
11.8	1.79
11.9	1.88
12	1.98



QUCS Simulation data for floating gate MOS device based on EKV v 2.6
Series 4.
Fig.8.3.4.4. V_c = 0.8V, V_{ds} = 0.1V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 10 – 12V in steps of 0.1V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

start of pulse

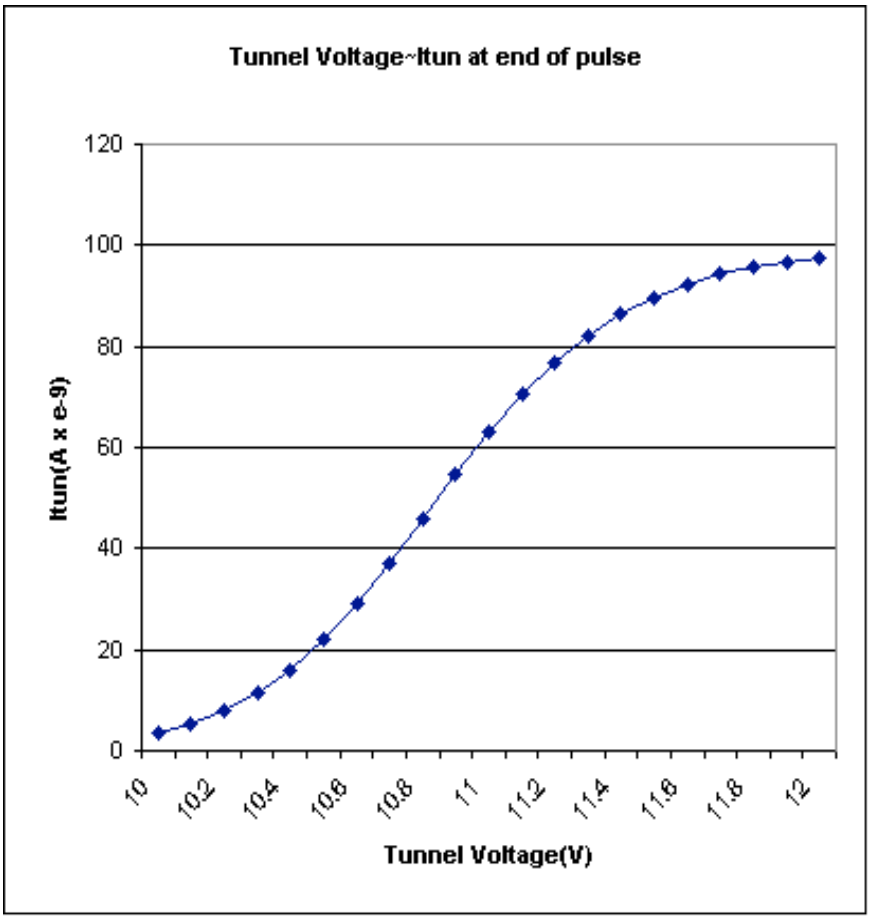
Tunnel Voltage (volts)	Itun during pulse x e-9(A)
10	3.68
10.1	5.65
10.2	8.59
10.3	12.9
10.4	19.3
10.5	28.4
10.6	41.4
10.7	59.6
10.8	84.6
10.9	118
11	163
11.1	227
11.2	290
11.3	375
11.4	472
11.5	578
11.6	689
11.7	799
11.8	905
11.9	1000
12	1090



QUCS Simulation data for floating gate MOS device based on EKV v 2.6 Series 4.

Fig.8.3.4.5. V_c = 0.8V, V_{ds} = 0.1V, T_1 = 0s, T_2 = 0.5ms, T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 10 – 12V in steps of 0.1V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

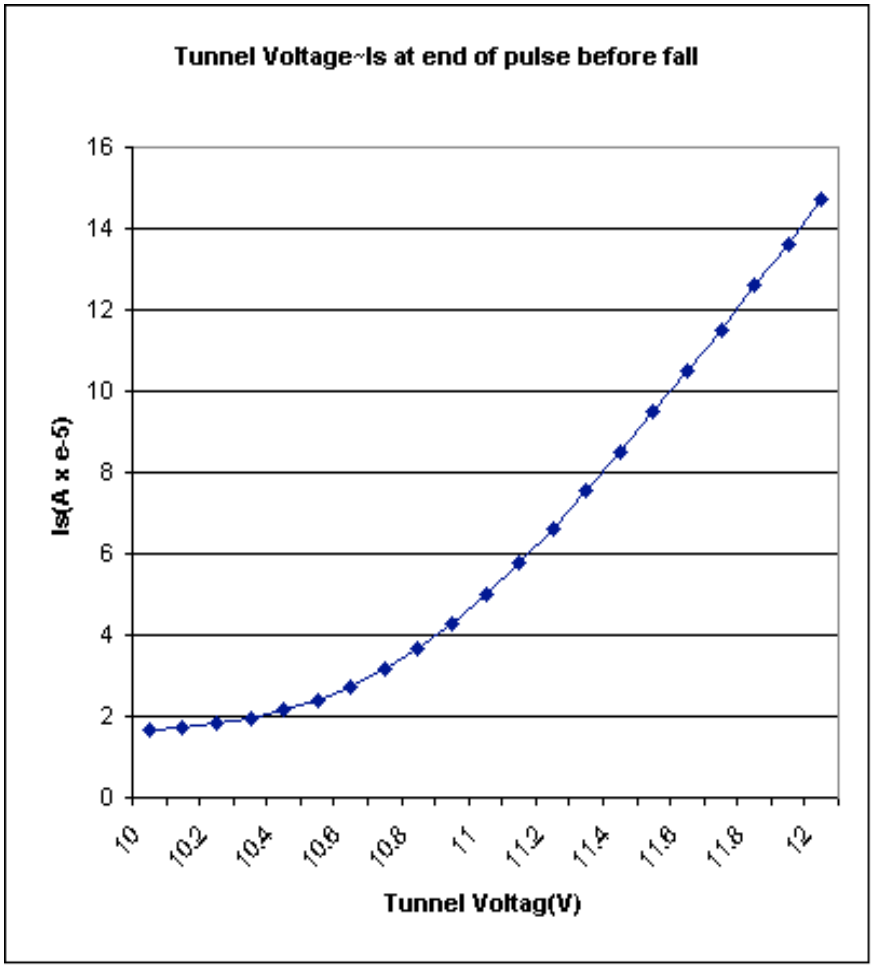
Tunnel Voltage (volts)	Itun during pulse x e-9(A) end of pulse
10	3.53
10.1	5.31
10.2	7.85
10.3	11.3
10.4	16
10.5	21.9
10.6	29
10.7	37.2
10.8	45.9
10.9	54.6
11	62.9
11.1	70.4
11.2	76.8
11.3	82.1
11.4	86.3
11.5	89.6
11.6	92.2
11.7	94.2
11.8	95.7
11.9	96.8
12	97.7



QUCS Simulation data for floating gate MOS device based on EKV v 2.6 Series 4.

Fig.8.3.4.6. V_c = 0.8V, V_{ds} = 0.1V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 10 – 12V in steps of 0.1V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

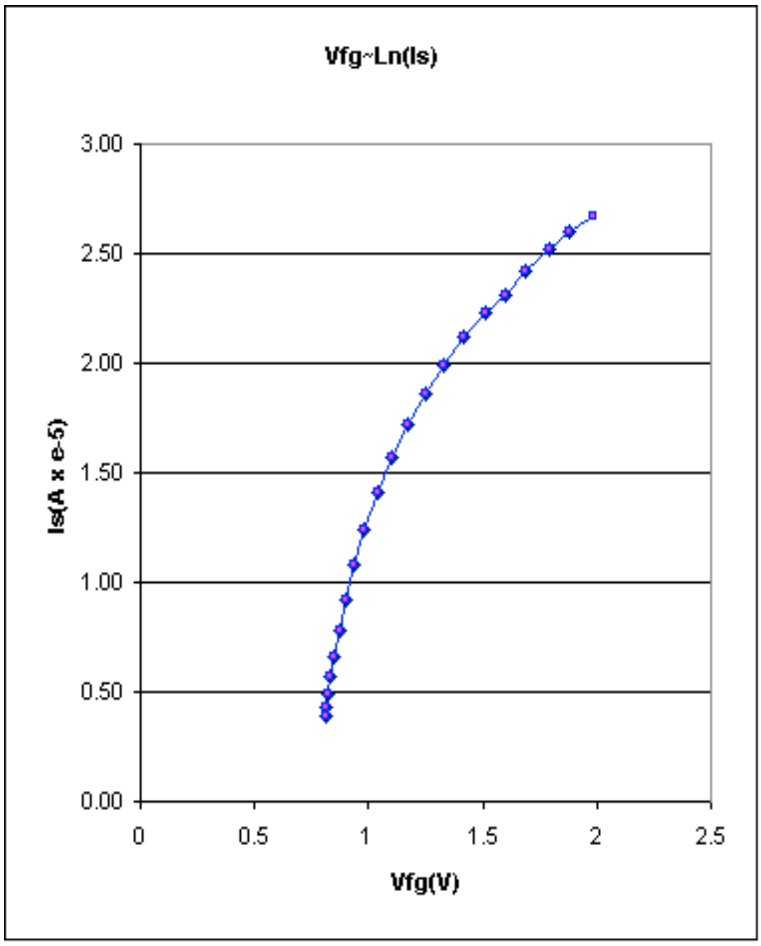
Tunnel Voltage (volts)	Is at end of pulse before fall x e-5(A)
10	1.67
10.1	1.73
10.2	1.82
10.3	1.95
10.4	2.14
10.5	2.39
10.6	2.72
10.7	3.15
10.8	3.67
10.9	4.28
11	4.99
11.1	5.77
11.2	6.63
11.3	7.54
11.4	8.5
11.5	9.49
11.6	10.5
11.7	11.5
11.8	12.6
11.9	13.6
12	14.7



QUCS Simulation data for floating gate MOS device based on EKV v 2.6 Series 4.

Fig.8.3.4.7. V_c = 0.8V, V_{ds} = 0.1V, T_1 = 0s, T_2 = 0.5ms,
T_r = 0.01ms and T_f = 0.01ms
V_{tun} variable from 10 – 12V in steps of 0.1V.
Total pulse duration = 50μs, T_r = 5μs and T_f = 5μs

Vfg after pulse fall (volts)	Is after pusle removed x e-5(A)	Ln(Is) x e-5(A)
0.809	1.48	0.392
0.815	1.54	0.432
0.823	1.63	0.489
0.834	1.76	0.565
0.85	1.94	0.663
0.872	2.19	0.784
0.901	2.52	0.924
0.938	2.95	1.082
0.983	3.47	1.244
1.04	4.09	1.409
1.1	4.79	1.567
1.17	5.58	1.719
1.25	6.43	1.861
1.33	7.34	1.993
1.42	8.29	2.115
1.51	9.28	2.228
1.6	10.03	2.306
1.69	11.3	2.425
1.79	12.4	2.518
1.88	13.4	2.595
1.98	14.5	2.674



8.3.4.2. Summary of Series (4)

Results for Series (4): The floating gate voltage rises slowly initially with change of tunnel pulse voltage but more rapidly after 11.5V when the Fowler-Nordheim takes effect. At the end of the pulse the floating gate voltage rose fairly slowly but almost linearly up to 10.6 V and more rapidly but remaining approximately linearly after 11V. After the pulse was removed there were small increase initially but gradually increased to 1.98V at a tunnel pulse voltage of 12V, showing heavy charge accumulation.

The tunnelling current at the start of the pulse is low before the onset of tunnelling, but increases around 11.4V, which indicates the start of Fowler-Nordheim tunnelling, this approximates to a square law relationship. The current at the end of the pulse is much smaller than at the beginning of the pulse although similar in shape until it starts to level off at approximately 11.8V.

The drain-source current was small ($2x10^{-5}$A) before Folwer-Nordheim tunnelling increases this due to charge accumulation on the floating gate.

The results clearly show that charge was transferred to the floating gate of this model so increasing it's voltage. Also this charge remained present once the tunnelling was removed.

Chapter 9

Summary, Conclusion and Future Work

9.1. Summary

The dissertation encompasses the investigation into the principles of floating gate devices. These devices have been extremely important in modern technology as analogue, and most importantly of all, as digital non-volatile memory elements. The principles and study of the transport of electronic charge through insulating material is well documented. The floating gate transistor relies on the storage of charge on an isolated gate. This stored charge modifies the transistors characteristics and as such can be used as a memory element.

For the design of complex modern electronic systems, simulators are essential to enable and speed up the design process. Within modern simulators there reside subcircuits and devices. New subcircuits and devices are modelled and added to these libraries as they develop.

SPICE has for long been the industrial standard for simulation, however in 2004, groups of engineers and scientists throughout the world decided to embark on a standardisation initiative for a General Public License simulator. This simulator was named QUCS and has since developed rapidly. Such developments require component, device, subcircuit and system models. The problem of creating a model for the floating gate device was that the gate was floating and it had no reference to ground. This meant that simulator analysis could not be carried out. However QUCS provide the opportunity to model this device with the use of EDDs, simulating charge transfer, and the use of an appropriate equivalent circuit for the device structure. The model was based on the EKV mosfet with the floating gate acting as the input to the transistor and contact and tunnelling coupling to the floating was achieved by means

of the associated structural capacitances. In order to make analysis possible large value resistors were added in parallel to the capacitors. D.C. and transient analysis was carried out to evaluate the change to the floating gate voltage when a suitable tunnel pulse was applied, typically 8 – 12.5V of 50ms duration. This equivalent circuit was then modelled within the QUCS environment and simulation then carried out for different sets of bias conditions and a range of tunnel pulses.

9.2. Conclusion

The model developed can now be used as an effective and adaptable model for a floating gate mosfet. The equivalent circuit created has overcome the problem of simulators not being able to analyse isolated nodes, by means of the use of an R-C network with an extended time constant. Theoretical analysis has been carried out for D.C. and transient analysis for Fowler- Nordheim tunnelling of the equivalent circuit created indicating the rate at which charge is transported to the floating gate and sensitive to the rate at which it varies. This indicates that the associated equation is implicit and any total solution may have to be interpolated. However, it is indicative of the charge transfer. Further work may be required on the original equations even at the Fowler-Nordheim level.

The floating gate model for simulation consists of R-C networks for the coupling of the contact and tunnelling terminals, plus an EDD controlling the Fowler-Nordheim tunnelling, and an EKV2v6 mosfet.

Simulations were carried out on a combination of biasing and various tunnelling pulses that assured electron tunnelling. These results have shown that the model is effective and charge transfer has taken place and that floating gate voltage levels are maintained at an increased level after the tunnelling pulse is removed.

The final conclusions from this work are:-

I. The principles of operation for a floating gate device are theoretically straight forward in that an isolated gate is used to vary the transistors characteristic. However it is the modelling, analysis and the implementation of that model in a simulator that is complex, because of the isolated gate.

II. Floating gate devices are difficult to model because of their inherent isolation. Whilst Fowler-Nordheim and Hot Electron Injection principles are well documented, modifications to their exact formulation may be required because of fabrication imperfections such as electron trapping and oxide imperfections.

III. A valid adaptable model has been created that can sit in the QUCS software library in order to accelerate the design process. Device parameters, such as dimensions, doping profiles and even new fabrication considerations can easily be changed or incorporated into the model.

IV. An equivalent circuit has been created for circuit analysis. This encompasses the idea of a large resistor in parallel with the device capacitances in order to give an extended time constant so that it will not effect simulation. Also an EDD is used to effect the tunnelling equation that is physics based.

V. The incorporation of EDDs into the model has been extremely useful. The EKV2v6 EDD model has been used and although the default parameters were mainly used, they can easily be changed. Based on the EKV2v6 EDD the required parameters were set for calculating the values for the contact resistor and capacitor, and the floating gate resistor and capacitor. Also an EDD was used to determine the tunnelling charge transfer to the floating gate. All design

aspects are easily adaptable to any required modifications or future developments.

VI. QUCS has been used to run simulations on the new model. The effective range of tunnelling voltage was varied from 8.8 – 10V (10 – 12.5V for a drain-source voltage of 2V), with a pulse width of 50ms. Detailed results are shown in chapter 9. But clearly charge has been transferred to the floating gate. The increase in floating gate voltage, from the ineffectual pre tunnelling voltage to the maximum tunnelling voltage used (10V for Vc=0.0.5V and 12.5V for Vc=0.05V), was of the order of 1.2 – 1.6V for Vc=0.8. This value of floating gate voltage would immediately drive the transistor into saturation and the contact gate would loose control. For the subthreshold value of contact voltage at 0.05V the increase is of the order of 160mV and allows the device to shift the effective threshold voltage but allows the contact gate to maintain control of the transistor.

The overall conclusion is that an effective and adaptive model has been created for a floating gate device that can be incorporated into the QUCS library. The model may be used to re-affirm the characteristics of devices already in the field or be adapted for the design of new floating gate devices using evolving fabrication techniques.

9.3.Future Work

As a non-volatile memory element, floating gate devices still have an expanding future in both digital and analogue electronics. Much of the demand is in increased densities and low power consumption. Innovative materials and fabrication procedures are overcoming some of these problems but inevitably new ones arise. Oxide thickness is nearing its limits even with the use of nitride floating gates.

Stacked structures are being designed with high-k, such as hafium based oxide, materials to replace the oxide layer, and gate electrodes made from materials such as Ru, Pt, Ir ,TiN and TaN. With the reduction in dimension more parasitic capacitance will have to be incorporated into models.

The model in this dissertation is being adapted at present to incorporate the discharging process using HEI, this involves placing some voltage regulation between the source terminal and ground by means of an EDD that operates according to the HEI equation and a voltage controlled current source. On completion of this work the full model can be placed into the QUCS library. At this stage the model will be available for manufacturers such as Altera, IEDM(Imec), Intersil, Hitachi and others to test the rigidity and adaptability of the model for their developing processes.

Adaptability to new smaller dimensions will be of particular importance along with retaining long duration remanence.

At present the great majority of floating gate designs are in digital electronics. However with a reliable model many more analogue circuit designs can be developed. These include analogue memory elements, capacitor-based circuits, adaptive circuits, and learning networks.

Design and simulation can be carried out with confidence in the anticipated results.

REFERENCES

1. C.C.Enz, R.A.Vittoz “Charge Based MOS Transistor Modelling, The EKV Model for Low Power and RF IC Design” Microelectronics Engineering. ISBN 13 978-0-470-85541-6. 2006.

2. M.E.Brinson, S.Jahn and M.Cullinan “Advances in Compact Semiconductor Device Modelling and circuit Macromodelling with Qucs GPL Circuit Simulator”. MOS-AK meeting IHP, Frankfurt(Oder), Germany. 2009.

3. S.Jahn, M.E.Brinson “Interactive Device Modelling using QUCS Equation Defined Devices” Journal of numerical modelling: Electronics, Networks, Devices and Fields, Vol.21, Issue 5 pp335-349. 2008.

4. M.E.Brinson “QUCS: Component, compact device and circuit modelling using symbolic equations”. http://qucs.sourceforge.net/contact.htm 2007.

5. P.Pavan, L.Archer, A.Marmiroli “Operation and Compact modelling” Klumer Academic Publishers, PP.140. ISBN 1-4020-7731-9. 2002

6. M.E.Brinson and S.Jahn “QUCS: AGPL software package for circuit simulation, compact device modelling and circuit macromodelling from DC to RF and beyond”, MOS-AK Meeting, MiPlaza, High Tech Campus, Eindhoven, The Netherlands. 2008.

7. A.Kolodny, S.T.K.Nieh, B.Eitean and J.Shappir “Analysis and Modeling of Floating-Gate EEPROM Cells” IEEE Transactions on Electronic Devices, vol.ED-33 No.6, 1986.

8. N.G.Tarr, D.L.Pulfery, D.L.Camporese, “An Analytical Model for MIS Tunnel Junctions”, IEEE Trns. Of Electronic Devices ED-30, pp.1760-1770. 1983.

9. G.Massobrio “Semiconductor Modelling with SPICE” Chapter(1) McGraw-Hill,Inc. ISBN 0-07-002107-4. 1994

10. M.E.Brinson “QUCs: Verilog-A implementation of the EKV v2.6 long and short channel MOSFET models”. http://qucs.sourceforge.net/contact.htm. 2008

11. W.Grabinski et al. “Advanced compact Modelling of deep sub micron technologies”, Journal of Telecommunications and Information, pp.31-32. 2000.

12. T.Ytterdal et al. “Device Modeling for analog and RF CMOS circuit Design” The EKV model pp.209-220. John Wiley and Sons Ltd. 2003.

13. W.Liu, “MOSFET models for SPICE simulation, including BSIM3v3 and BSIM4” Wiley Interscience Publications, ISBN 0-471-39697-4. 2008.

14. M.Lenzlinger, E.H.Snow ”Fowler-Nordheim Tunnelling into Thermally Grown SiO2” IEEE, Transactions on Electron Devices, pp686-688. 1968.

15. P.Hasler, A.Andreou, C.Diorio, B.A.Minch and C.Mead “Impact Ionization and Hot Electron Injection derived consistently from Boltzmann transport” . VLSI Design vol.8. No.14 pp455-461. 199

16. Y.Xu “ Electron Transport through thin film amorphous silicon – A Tunnelling Study” Ph.D. Thesis, Stanford University. 1992.

17. P.K. Ko “Hot Electron Effects in MOSFETs” Ph.D. Thesis, University of Berkley, Calafornia, USA. 1982.

18. P.Hasler, T.S. Lande “Overview of Floating Gate Devices, Circuits and Systems” IEEE, Transactions on Circuits and Systems II: Analog and digital Signal Processing. 2002.

19. W.Gao and W.M.Snelgrove. “The Floating Gate MOS Device as an Analog Element for Analog Trimming” IEEE, International Symposium on Circuits and Systems, Vol.4. 1994.

20. S.M.Sze. “VLSI Technology” McGraw-Hill. ISBN 0-07-062735-5.1988.

21. K.Rahhimi, C.Diorio, C.Hernandez, M.D.Brockhausen. “A Simulation Model for Floating-Gate MOS Synapse Transistors” IEEE International Symposium on Circuits and Systems, 2002.

22. M.Bucher, C.Lallement, C.Enz, F.Theodoloz and F.Krummenacher “The EPFL-EKV MOSFET Model Equations for Simulation” Technical report Swiss Federal Institute of technology(EPFL), Lausanne, Switzerland. 1998.

23. K.Kang and S.M.Sze “A floating Gate and its application to memory devices” IEEE Trans on Electron Devices, Vol.14 Issue 9.1967.

24. **PATENTS:** P.Bloome, A.Cacciato, G.Sankarkar, “Floating Gate Semiconductor Memory devices and Method of producing such a device” Feb. 2014. Patent No. US 8652902 B2 (also published as EP2495762A1, US 20120223378).

25. **PATENTS:** K.Takahashi, S.Fujutsu, “Method for manufacturing a semiconductor floating gate memory device” Patent No. EP1615266A3 (also published as CN1719597A: Jan. 2014)

26. P.Pavan et al. “A Complete Model of E2PROM Memory cells for Circuit Simulation”, IEEE Trans on CAD for ICs and Systems, Vol. 22 No.8. August 2003.

27. C.Diorio,P.Hasler, A.Minch, C.A. Mead. “A Floating Gate Learning Array with locally computed weight updates” IEEE, Transactions on Electron Devices, Vol 44, Issue 12, pp2281-2289. 1997.

28. M.Krajmer, J.Racko, D.Durackova. “A Novel Device Floating Gate Transistor for storing weights of neural networks” Dept. of Microelectronics, Faculty of Electrical Engineering and IT, Slovak University of Technology, Bratislava, Slovakia, 15th Conference on Microwave Techniques, 2010.

29. R.Bez et al. “Flash memories” Proceedings of IEEE S.T. Microelectronics, Vol19. No.4. 2003.

30. J.F. Zhang, H.K. Sii, G. Groesenken, R. Degraeve “Hole Trapping and Trap Generation in the gate SiO2” IEEE, transactions on Electronic Devices, Vol. 48, Issue 6, pp1127-1135. 2001

31. N.M.Hossain, M.H.Chowdury. “Multilayer Graphene Nanoribbon Floating Gate Transistors for Flash Memory”, IEEE, Int. Symposium on Circuits and Systems pp806-809. 2014.

32. J.Gray, R.Robucci, P.Hasler. “The Design and Simulation Model of an Analog Floating Gate Computational element for use in large scale analog reconfigurable systems” Proceedings of Mid west Symposium on Circuits and Systems, Vo.1. pp.253-256. 2008.

33. A.B.Bhattacharyya. “Compact MOSFET Models for VLSI Design” John Wiley & Sons ISBN 978-0-470-82342-2. 2010.

34. A.Thomsen, M.A.Brooke. “Use of electron tunnelling in standard CMOS double poly process”IEEE Electronic Devices Letters, Vol.12 pp.111-113. 1993.

35. M.Drakaki, G.Fikos, S.Siskos. “Sub Threshold behaviour modelling of FGMOS Transistors using ACM and the BSIM3v3 models” Aristotle University of Thessaloniki, Dept. of Physics. 2004.

36. A.Mondragon-Torres, M.Schneider, E.Sanchez-Sinencio. “Extraction of Electrical parameters of Floating Gate Devices for circuit analysis, simulation and design” Proceedings of Mid west Symposium on Circuits and Systems, Vo.1. pp.I. 311-314. 2002.

11. Appendices

Appendix 1 [1.b.]

QUCS Verilog A code for EKV v2.6 MOSFET model

Qucs Verilog-A code for the EKV v2.6 MOSFET model

nMOS: EKV equation numbers are given on the right-hand side of code lines

```
//    Qucs EPFL-EKV 2.6 nMOS model:
//
//    The structure and theoretical background to the EKV 2.6
//    Verilog-a model is presented in the Qucs EPFL-EKV 2.6 report.
//    Typical parameters are for 0.5um CMOS (C) EPLFL-LEG 1999.
//    Geometry range: Short channel W>= 0.8um, L >= 0.5um
//                    Long channel  W>= 2um,   L >= 2um
//    Voltage range:  |Vgb| < 3.3V, |Vdb| < 3.3V, |Vsb| < 2V
//
//    This is free software; you can redistribute it and/or modify
//    it under the terms of the GNU General Public License as published by
//    the Free Software Foundation; either version 2, or (at your option)
//    any later version.
//
//    Copyright (C), Mike Brinson, mbrin72043@yahoo.co.uk, May 2008.
//
`include "disciplines.vams"
`include "constants.vams"

//
 module EKV26nMOS (Drain, Gate, Source, Bulk);
 inout Drain, Gate, Source, Bulk;
electrical Drain, Gate, Source, Bulk;
// Internal nodes
electrical Drain_int, Source_int;
`define attr(txt) (*txt*)
// Device dimension parameters
 parameter real LEVEL = 1 from [1 : 2]
        `attr(info="long = 1, short = 2");
 parameter real L = 0.5e-6 from [0.0 : inf]
        `attr(info="length parameter" unit = "m" );
 parameter real W = 10e-6 from [0.0 : inf]
        `attr(info="Width parameter" unit = "m");
 parameter real Np = 1.0 from [1.0 : inf]
        `attr(info="parallel multiple device number");
 parameter real Ns = 1.0 from [1.0 : inf]
        `attr(info="series multiple device number");
// Process parameters
```

```
 parameter real Cox = 3.45e-3 from [0 : inf]
        'attr(info="gate oxide capacitance per unit area" unit = "F/m**2" );
 parameter real Xj = 0.15e-6 from [0.01e-6 : 1.0e-6]
        'attr(info="metallurgical junction depth" unit = "m");
 parameter real Dw = -0.02e-6 from [-inf : 0.0]
        'attr(info="channel width correction" unit = "m");
 parameter real Dl = -0.05e-6 from [-inf : 0.0]
        'attr(info="channel length correction" unit = "m");
// Basic intrinsic model parameters
 parameter real Vto = 0.6 from [1e-6 : 2.0]
        'attr(info="long channel threshold voltage" unit="V" );
 parameter real Gamma = 0.71 from [0.0 : 2.0]
        'attr(info="body effect parameter" unit="V**(1/2)");
 parameter real Phi = 0.97 from [0.3 : 2.0]
        'attr(info="bulk Fermi potential" unit="V");
 parameter real Kp = 150e-6 from [10e-6 : inf]
        'attr(info="transconductance parameter" unit = "A/V**2");
 parameter real Theta = 50e-3 from [0.0 : inf]
        'attr(info="mobility reduction coefficient" unit = "1/V");
 parameter real E0 = 88.0e6 from [1.0e6 : inf]
        'attr(info="mobility coefficient" unit="V/m");
 parameter real Ucrit = 4.5e6 from [2.0e6 : 25.0e6]
        'attr(info="longitudinal critical field" unit="V/m");
// Channel length and charge sharing parameters
 parameter real Lambda = 0.23 from [0.1 : inf]
        'attr(info="depletion length coefficient");
 parameter real Weta = 0.05 from [0.0 : inf]
        'attr(info="narrow-channel effect coefficient");
 parameter real Leta = 0.28 from [0.0 : inf]
        'attr(info="longitudinal critical field");
// Reverse short channel effect parameters
 parameter real Q0 = 280e-6 from [0.0 : inf]
        'attr(info="reverse short channel charge density" unit="A*s/m**2");
 parameter real Lk = 0.5e-6 from [0.0 : inf]
        'attr(info="characteristic length" unit="m");
// Intrinsic model temperature parameters
 parameter real Tcv = 1.5e-3
        'attr(info="threshold voltage temperature coefficient" unit="V/K");
 parameter real Bex = -1.5
        'attr(info="mobility temperature coefficient");
 parameter real Ucex = 1.7
        'attr(info="Longitudinal critical field temperature exponent");
 parameter real Ibbt = 0.0
        'attr(info="Ibb temperature coefficient"  unit="1/K");
// Series resistance calculation parameters
 parameter real Hdif = 0.9e-6 from [0.0 :inf]
        'attr(info="heavily doped diffusion length" unit = "m");
 parameter real Rsh = 510.0 from [0.0 : inf]
        'attr(info="drain/source diffusion sheet resistance" unit="Ohm/square");
 parameter real Rsc = 0.0 from [0.0 : inf]
        'attr(info="source contact resistance" unit="Ohm");
 parameter real Rdc = 0.0 from [0.0 : inf]
        'attr(info="drain contact resistance" unit="Ohm");
// Gate overlap capacitances
 parameter real Cgso = 1.5e-10 from [0.0 :inf]
        'attr(info="gate to source overlap capacitance" unit = "F/m");
 parameter real Cgdo = 1.5e-10 from [0.0 : inf]
        'attr(info="gate to drain overlap capacitance"  unit=  "F/m");
 parameter real Cgbo = 4.0e-10 from [0.0 : inf]
        'attr(info="gate to bulk overlap capacitance"   unit=  "F/m");
// Impact ionization related parameters
 parameter real Iba = 2e8 from [0.0 :inf]
        'attr(info="first impact ionization coefficient" unit = "1/m");
 parameter real Ibb = 3.5e8 from [1.0e8 : inf]
        'attr(info="second impact ionization coefficient" unit="V/m");
```

```
 parameter real Ibn = 1.0 from [0.1 : inf]
        'attr(info="saturation␣voltage␣factor␣for␣impact␣ionization");
// Flicker noise parameters
 parameter real Kf = 1.0e-27 from [0.0 :inf]
        'attr(info="flicker␣noise␣coefficient");
 parameter real Af = 1.0 from [0.0 : inf]
        'attr(info="flicker␣noise␣exponent" );
// Matching parameters
 parameter real Avto = 0.0 from [0.0 :inf]
        'attr(info="area␣related␣theshold␣voltage␣mismatch␣parameter" unit = "V*m");
 parameter real Akp = 0.0 from [0.0 : inf]
        'attr(info="area␣related␣gain␣mismatch␣parameter" unit="m");
 parameter real Agamma = 0.0 from [0.0 : inf]
        'attr(info="area␣related␣body␣effect␣mismatch␣parameter" unit="sqrt(V)*m");
// Diode parameters
 parameter real N=1.0 from [1e-6:inf]
        'attr(info="emission␣coefficient");
 parameter real Is=1e-14 from [1e-20:inf]
        'attr(info="saturation␣current" unit="A" );
 parameter real Bv=100 from [1e-6:inf]
        'attr(info="reverse␣breakdown␣voltage" unit="V");
 parameter real Ibv=1e-3 from [1e-6:inf]
        'attr(info="current␣at␣reverse␣breakdown␣voltage" unit="A");
 parameter real Vj=1.0 from [1e-6:inf]
        'attr(info="junction␣potential" unit="V");
 parameter real Cj0=300e-15 from [0:inf]
        'attr(info="zero-bias␣junction␣capacitance" unit="F");
 parameter real M=0.5 from [1e-6:inf]
        'attr(info="grading␣coefficient");
 parameter real Area=1.0 from [1e-3:inf]
        'attr(info="diode␣relative␣area");
 parameter real Fc=0.5 from [1e-6:inf]
        'attr(info="forward-bias␣depletion␣capcitance␣coefficient");
 parameter real Tt=0.1e-9 from [1e-20:inf]
        'attr(info="transit␣time" unit="s" );
 parameter real Xti=3.0 from [1e-6:inf]
        'attr(info="saturation␣current␣temperature␣exponent");
// Temperature parameters
 parameter real Tnom = 26.85
        'attr(info="parameter␣measurement␣temperature" unit = "Celsius");
// Local variables
real epsilonsi, epsilonox, Tnomk, T2, Tratio, Vto_T, Ucrit_T, Egnom, Eg, Phi_T;
real Weff, Leff, RDeff, RSeff, con1, con2, Vtoa, Kpa,Kpa_T,Gammaa, C_epsilon, xi;
real nnn, deltaV_RSCE, Vg, Vs, Vd, Vgs, Vgd, Vds, Vdso2, VG, VS, VD;
real VGprime, VP0, VSprime, VDprime, Gamma0, Gammaprime, Vp;
real n, X1, iff, X2, ir, Vc, Vdss, Vdssprime, deltaV, Vip;
real Lc, DeltaL, Lprime, Lmin, Leq, X3, irprime, Beta0, eta;
real Qb0, Beta0prime, nq, Xf, Xr, qD, qS, qI, qB, Beta, Ispecific, Ids, Vib, Idb, Ibb_T;
real A, B, Vt_T2, Eg_T1, Eg_T2, Vj_T2, Cj0_T2, F1, F2, F3, Is_T2;
real Id1, Id2, Id3, Id4, Is1, Is2, Is3, Is4, V1, V2, Ib_d, Ib_s, Qd, Qs, Qd1, Qd2, Qs1, Qs2;
real qb, qg, qgso, qgdo, qgbo, fourkt, Sthermal, gm, Sflicker, StoDswap, p_n_MOS;
//
analog begin
// Equation initialization
p_n_MOS = 1.0; // nMOS
A=7.02e-4;
B=1108.0;
epsilonsi = 1.0359e-10;      // Eqn 4
epsilonox = 3.453143e-11;    // Eqn 5
Tnomk = Tnom+273.15;                 // Eqn 6
T2=$temperature;
Tratio = T2/Tnomk;
Vto_T = Vto-Tcv*(T2-Tnomk);
Egnom = 1.16-0.000702*Tnomk*Tnomk/(Tnomk+1108);
Eg =    1.16-0.000702*T2*T2/(T2+1108);
```

```
Phi_T = Phi*Tratio - 3.0*$vt*ln(Tratio)-Egnom*Tratio+Eg;
Ibb_T = Ibb*(1.0+Ibbt*(T2 -Tnomk));
Weff = W + Dw;     // Eqn 25
Leff = L + Dl;     // Eqn 26
RDeff = ( (Hdif*Rsh)/Weff)/Np + Rdc;
RSeff = ( (Hdif*Rsh)/Weff)/Np + Rsc;
con1 = sqrt(Np*Weff*Ns*Leff);
Vt_T2='P_K*T2/'P_Q;
Eg_T1=Eg-A*Tnomk*Tnomk/(B+Tnomk);
Eg_T2=Eg-A*T2*T2/(B+T2);
Vj_T2=(T2/Tnomk)*Vj-(2*Vt_T2)*ln(pow((T2/Tnomk),1.5))-((T2/Tnomk)*Eg_T1-Eg_T2);
Cj0_T2=Cj0*(1+M*(400e-6*(T2-Tnomk)-(Vj_T2-Vj)/Vj));
F1=(Vj/(1-M))*(1-pow((1-Fc),(1-M)));
F2=pow((1-Fc), (1+M));
F3=1-Fc*(1+M);
Is_T2=Is*pow( (T2/Tnomk), (Xti/N))*limexp((-Eg_T1/Vt_T2)*(1-T2/Tnomk));
con2 = (Cox*Ns*Np*Weff*Leff);
fourkt = 4.0*'P_K*T2;
//
if (LEVEL == 2)
 begin
  Ucrit_T = Ucrit*pow(Tratio, Ucex);
  Vtoa = Vto+Avto/con1;                  // Eqn 27
  Kpa = Kp*(1.0+Akp/con1);               // Eqn 28
  Kpa_T = Kpa*pow( Tratio, Bex);         // Eqn 18
  Gammaa = Gamma+Agamma/con1;            // Eqn 29
  C_epsilon = 4.0*pow(22e-3, 2);         // Eqn 30
  xi = 0.028*(10.0*(Leff/Lk)-1.0);       // Eqn 31
  nnn = 1.0+0.5*(xi+ sqrt(pow(xi,2) + C_epsilon));
  deltaV_RSCE = (2.0*Q0/Cox)*(1.0/pow(nnn,2)); // Eqn 32
 end
//
// Model branch and node voltages
//

Vg = p_n_MOS*V(Gate, Bulk);
Vs = p_n_MOS*V(Source, Bulk);
Vd = p_n_MOS*V(Drain, Bulk);
VG=Vg;          // Eqn 22
if ( (Vd-Vs) >= 0.0)
        begin
          StoDswap = 1.0;
          VS=Vs;    // Eqn 23
          VD=Vd;    // Eqn 24
        end
else
        begin
          StoDswap = -1.0;
          VD=Vs;
          VS=Vd;
        end
if (LEVEL == 2)
    VGprime=VG-Vto_T-deltaV_RSCE+Phi_T+Gamma*sqrt(Phi_T);  // Eqn 33  nMOS equation
else
    VGprime=Vg-Vto_T+Phi_T+Gamma*sqrt(Phi_T);

//
if (LEVEL == 2)
 begin
  if (VGprime > 0)
        VP0=VGprime-Phi_T-Gammaa*(sqrt(VGprime+(Gammaa/2.0)*(Gammaa/2.0))
              -(Gammaa/2.0));   // Eqn 34
  else
        VP0 = -Phi_T;
  VSprime=0.5*(VS+Phi_T+sqrt(pow( (VS+Phi_T),2) + pow( (4.0*$vt),2)));  // Eqn 35
```

```
  VDprime=0.5*(VD+Phi_T+sqrt(pow( (VD+Phi_T),2) + pow( (4.0*$vt),2)));   // Eqn 35
  Gamma0=Gammaa-(epsilonsi/Cox)*((Leta/Leff)*(sqrt(VSprime)+sqrt(VDprime))
                -(3.0*Weta/Weff)*sqrt(VP0+Phi_T));   // Eqn 36
  Gammaprime = 0.5*(Gamma0+sqrt( pow(Gamma0,2) +0.1*$vt ));   // Eqn 37
  if (VGprime > 0.0 )
          Vp = VGprime-Phi_T-Gammaprime*(sqrt(VGprime+(Gammaprime/2.0)*
               (Gammaprime/2.0)) - (Gammaprime/2.0)); // Eqn 38
  else
       Vp = -Phi_T;
  n = 1.0 +Gammaa/(2.0*sqrt(Vp+Phi_T+4.0*$vt));   // Eqn 39
 end
else
  begin
   if (VGprime > 0)
       Vp=VGprime-Phi_T-Gamma*(sqrt(VGprime+(Gamma/2.0)*(Gamma/2.0))
          -(Gamma/2.0));   // Eqn 34
   else
       Vp = -Phi_T;
   n = 1.0 +Gamma/(2.0*sqrt(Vp+Phi_T+4.0*$vt));   // Eqn 39
end
//
X1 = (Vp-VS)/$vt;
iff = ln(1.0+limexp(X1/2.0))*ln(1.0+limexp(X1/2.0));    // Eqn 44
X2 = (Vp-VD)/$vt;
ir = ln(1.0+limexp(X2/2.0))*ln(1.0+limexp(X2/2.0));     // Eqn 57
//
if (LEVEL == 2)
 begin
   Vc = Ucrit_T*Ns*Leff;   // Eqn 45
   Vdss = Vc*(sqrt( 0.25 + (($vt/(Vc))*sqrt(iff))) -0.5);   // Eqn 46;
   Vdssprime = Vc*(sqrt( 0.25 + ($vt/Vc)*(sqrt(iff)-0.75*ln(iff))) - 0.5)
               +$vt*(ln(Vc/(2.0*$vt)) - 0.6 ); // Eqn 47
   if (Lambda*(sqrt(iff) > (Vdss/$vt) ) )
         deltaV = 4.0*$vt*sqrt(Lambda*(sqrt(iff) -(Vdss/$vt))
                  + (1.0/64.0) );   // Eqn 48
   else
         deltaV = 1.0/64.0;
   Vdso2 = (VD-VS)/2.0;          // Eqn 49
   Vip = sqrt( pow(Vdss, 2) + pow( deltaV,2)) - sqrt( pow( (Vdso2 - Vdss), 2)
       + pow (deltaV, 2));  // Eqn 50
   Lc = sqrt( (epsilonsi/Cox)*Xj);   // Eqn 51
   DeltaL = Lambda*Lc*ln(1.0+((Vdso2-Vip)/(Lc*Ucrit_T)));   // Eqn 52
   Lprime = Ns*Leff - DeltaL + ( (Vdso2+Vip)/Ucrit_T); // Eqn 53
   Lmin = Ns*Leff/10.0;   // Eqn 54
   Leq = 0.5*(Lprime + sqrt( pow(Lprime, 2) + pow(Lmin, 2)));    // Eqn 55
   X3 = (Vp-Vdso2-VS-sqrt( pow(Vdssprime, 2) + pow( deltaV, 2))
       + sqrt( pow( (Vdso2-Vdssprime), 2) + pow(deltaV,2)))/$vt;
   irprime = ln(1.0+limexp(X3/2.0))*ln(1.0+limexp(X3/2.0));   // Eqn 56
   Beta0 = Kpa_T*(Np*Weff/Leq);       // Eqn 58
   eta = 0.5;   // Eqn 59 - nMOS
   Qb0 = Gammaa*sqrt(Phi_T);   // Eqn 60;
   Beta0prime = Beta0*(1.0 +(Cox/(EO*epsilonsi))*Qb0);   // Eqn 61
   nq = 1.0 +Gammaa/(2.0*sqrt(Vp+Phi_T+1e-6));            // Eqn 69
 end
else
 nq = 1.0 +Gamma/(2.0*sqrt(Vp+Phi_T+1e-6));             // Eqn 69
//
Xf = sqrt(0.25+iff);      // Eqn 70
Xr = sqrt(0.25+ir);       // Eqn 71
qD = -nq*( (4.0/15.0)*((3.0*pow( Xr,3) + 6.0*pow( Xr, 2)*Xf + 4.0*Xr*pow( Xf, 2)
     + 2.0*pow(Xf, 3))/(pow( (Xf+Xr), 2) ) ) -0.5);   // Eqn 72
qS = -nq*( (4.0/15.0)*((3.0*pow( Xf,3) + 6.0*pow( Xf, 2)*Xr + 4.0*Xf*pow( Xr, 2)
     + 2.0*pow(Xr, 3))/(pow( (Xf+Xr), 2) ) ) -0.5);   // Eqn 73
qI = -nq*( (4.0/3.0)*( (pow(Xf,2)+(Xf*Xr)+pow(Xr,2))/(Xf+Xr)) - 1.0);     // Eqn 74
if (LEVEL == 2)
```

```
  if (VGprime > 0)
        qB = (-Gammaa*sqrt(Vp+Phi_T+1e-6))*(1.0/$vt) - ( (nq-1.0)/nq)*qI;   // Eqn 75
  else
        qB = -VGprime/$vt;
else
    if (VGprime > 0)
        qB = (-Gamma*sqrt(Vp+Phi_T+1e-6))*(1.0/$vt) - ( (nq-1.0)/nq)*qI;   // Eqn 75
  else
        qB = -VGprime/$vt;
//
if (LEVEL == 2)
   Beta = Beta0prime/(1.0 + (Cox/ (EO*epsilonsi))*$vt*abs(qB+eta*qI));       // Eqn 62
else
   Beta = Kp*(Weff/Leff)/(1+Theta*Vp);
//
Ispecific = 2.0*n*Beta*pow( $vt, 2);     // Eqn 65
//
if (LEVEL == 2)
  begin
   Ids = Ispecific*(iff-irprime);            // Eqn 66
   Vib = VD-VS-Ibn*2.0*Vdss;                 // Eqn 67
   if ( Vib > 0.0)
    Idb = Ids*(Iba/Ibb_T)*Vib*exp( (-Ibb_T*Lc)/Vib);    // Eqn 68
   else
   Idb = 0.0;
  end
else
   Ids = Ispecific*(iff-ir);           // Eqn 66
//
Sthermal = fourkt*Beta*abs(qI);
gm = Beta*$vt*(sqrt( (4.0*iff/Ispecific) +1.0) - sqrt( (4.0*ir/Ispecific) + 1.0) );
Sflicker = (Kf*gm*gm)/(Np*Weff*Ns*Leff*Cox);
//
qb = con2*$vt*qB;
qg = con2*$vt*(-qI-qB);
qgso = Cgso*Weff*Np*(VG-VS);
qgdo = Cgdo*Weff*Np*(VG-VD);
qgbo = Cgbo*Leff*Np*VG;
// Drain and source diodes
if (StoDswap > 0.0)
      begin
         V1=p_n_MOS*V(Bulk, Drain_int);
         V2=p_n_MOS*V(Bulk, Source_int);
      end
else
      begin
         V2=p_n_MOS*V(Bulk, Drain_int);
         V1=p_n_MOS*V(Bulk, Source_int);
      end
Id1= (V1>-5.0*N*$vt) ? Area*Is_T2*(limexp( V1/(N*Vt_T2) )-1.0) : 0;
Qd1=(V1<Fc*Vj)? Tt*Id1+Area*(Cj0_T2*Vj_T2/(1-M))*(1-pow((1-V1/Vj_T2),(1-M))):0;
Id2=(V1<=-5.0*N*$vt) ? -Area*Is_T2 : 0;
Qd2=(V1>=Fc*Vj)? Tt*Id1+Area*Cj0_T2*(F1+(1/F2)*(F3*(V1-Fc*Vj_T2)+(M/(2.0*Vj_T2))
      *(V1*V1-Fc*Fc*Vj_T2*Vj_T2))):0;
Id3=(V1 == -Bv) ? -Ibv  : 0 ;
Id4=(V1<-Bv) ?-Area*Is_T2*(limexp(-(Bv+V1)/Vt_T2)-1.0+Bv/Vt_T2) : 0;
Ib_d = Id1+Id2+Id3+Id4;
Qd = Qd1+Qd2;
//
Is1= (V2>-5.0*N*$vt) ? Area*Is_T2*(limexp( V2/(N*Vt_T2) )-1.0) : 0;
Qs1=(V2<Fc*Vj)? Tt*Is1+Area*(Cj0_T2*Vj_T2/(1-M))*(1-pow((1-V2/Vj_T2),(1-M))):0;
Is2=(V2<=-5.0*N*$vt) ? -Area*Is_T2 : 0;
Qs2=(V2>=Fc*Vj)? Tt*Is1+Area*Cj0_T2*(F1+(1/F2)*(F3*(V2-Fc*Vj_T2)+(M/(2.0*Vj_T2))
      *(V2*V2-Fc*Fc*Vj_T2*Vj_T2))):0;
Is3=(V2 == -Bv) ? -Ibv  : 0 ;
```

```
Is4=(V2<-Bv) ?-Area*Is_T2*(limexp(-(Bv+V2)/Vt_T2)-1.0+Bv/Vt_T2) : 0;
Ib_s = Is1+Is2+Is3+Is4;
Qs = Qs1+Qs2;
// Current and noise contributions
if ( StoDswap > 0.0)
 begin
      if (RDeff > 0.0)
         I(Drain, Drain_int) <+ V(Drain, Drain_int)/RDeff;
      else
         I(Drain, Drain_int) <+ V(Drain, Drain_int)/1e-7;
      if (RSeff > 0.0)
         I(Source, Source_int) <+ V(Source, Source_int)/RSeff;
      else
         I(Source, Source_int) <+ V(Source, Source_int)/1e-7;
   I(Drain_int, Source_int) <+ p_n_MOS*Ids;
   if (LEVEL == 2)
       I(Drain_int, Bulk) <+ p_n_MOS*Idb;
   I(Gate, Drain_int) <+ p_n_MOS*0.5*ddt(qg);
   I(Gate, Source_int) <+ p_n_MOS*0.5*ddt(qg);
   I(Drain_int, Bulk) <+ p_n_MOS*0.5*ddt(qb);
   I(Source_int, Bulk) <+ p_n_MOS*0.5*ddt(qb);
   I(Gate, Source_int) <+ p_n_MOS*ddt(qgso);
   I(Gate, Drain_int)  <+ p_n_MOS*ddt(qgdo);
   I(Gate, Bulk)   <+ p_n_MOS*ddt(qgbo);
   I(Bulk, Drain_int) <+ p_n_MOS*Ib_d;
   I(Bulk, Drain_int) <+ p_n_MOS*ddt(Qd);
   I(Bulk, Source_int) <+ p_n_MOS*Ib_s;
   I(Bulk, Source_int) <+ p_n_MOS*ddt(Qs);
   I(Drain_int, Source_int) <+ white_noise(Sthermal,"thermal");
   I(Drain_int, Source_int) <+ flicker_noise(Sflicker, Af, "flicker");
   I(Drain, Drain_int) <+ white_noise(fourkt/RDeff, "thermal");
   I(Source, Source_int) <+ white_noise(fourkt/RSeff, "thermal");
end
else
 begin
      if (RSeff > 0.0)
         I(Drain, Drain_int) <+ V(Drain, Drain_int)/RSeff;
      else
         I(Drain, Drain_int) <+ V(Drain, Drain_int)/1e-7;
      if (RDeff > 0.0)
         I(Source, Source_int) <+ V(Source, Source_int)/RDeff;
      else
         I(Source, Source_int) <+ V(Source, Source_int)/1e-7;
   I( Source_int, Drain_int) <+ p_n_MOS*Ids;
   if (LEVEL == 2)
       I(Source_int, Bulk) <+ p_n_MOS*Idb;
   I( Gate, Source_int) <+ p_n_MOS*0.5*ddt(qg);
   I( Gate, Drain_int) <+ p_n_MOS*0.5*ddt(qg);
   I( Source_int, Bulk) <+ p_n_MOS*0.5*ddt(qb);
   I( Drain_int, Bulk) <+ p_n_MOS*0.5*ddt(qb);
   I( Gate, Drain_int) <+ p_n_MOS*ddt(qgso);
   I( Gate, Source_int)  <+ p_n_MOS*ddt(qgdo);
   I( Gate, Bulk)   <+ p_n_MOS*ddt(qgbo);
   I( Bulk, Source_int) <+ p_n_MOS*Ib_d;
   I( Bulk, Source_int) <+ p_n_MOS*ddt(Qd);
   I( Bulk, Drain_int) <+ p_n_MOS*Ib_s;
   I( Bulk, Drain_int) <+ p_n_MOS*ddt(Qs);
   I( Source_int, Drain_int) <+ white_noise(Sthermal,"thermal");
   I( Source_int, Drain_int) <+ flicker_noise(Sflicker, Af, "flicker");
   I( Source_int, Source) <+ white_noise(fourkt/RDeff, "thermal");
   I( Drain_int, Drain) <+ white_noise(fourkt/RSeff, "thermal");
 end
end
endmodule
```

Appendix 2 [1.b.]

Long channel model parameters (LEVEL = 1)

Name	Symbol	Description	Unit	Default nMOS	Default pMOS
LEVEL		Model selector		1	1
L	L	length parameter	m	$10e-6$	$10e-6$
W	W	width parameter	m	$10e-6$	$10e-6$
Np	Np	parallel multiple device number		1	1
Ns	Ns	series multiple device number		1	1
Cox	Cox	gate oxide capacitance per unit area	F/m^2	$3.4e-3$	$3.4e-3$
Xj	Xj	metallurgical junction length	m	$0.15e-6$	$0.15e-6$
Dw	Dw	channel width correction	m	$-0.02e-6$	$-0.02e-6$
Dl	Dl	channel length correction	m	$-0.05e-6$	$-0.05e-6$
Vto	Vto	long channel threshold voltage	V	0.5	-0.55
Gamma	$Gamma$	body effect parameter	$\sqrt{V}$	0.7	0.69
Phi	Phi	bulk Fermi potential	V	0.5	0.87
Kp	Kp	transconductance parameter	A/V^2	$50e-6$	$20e-6$
Theta	$Theta$	mobility reduction coefficient	$1/V$	$50e-3$	$50e-3$
Tcv	Tcv	threshold voltage temperature coefficient	V/K	$1.5e-3$	$-1.4e-3$
Hdif	$Hdif$	heavily doped diffusion length	m	$0.9e-6$	$0.9e-6$
Rsh	Rsh	drain-source diffusion sheet resistance	$\Omega/square$	510	510
Rsc	Rsc	source contact resistance	Ω	0.0	0.0
Rdc	Rdc	drain contact resistance	Ω	0.0	0.0
Cgso	$Cgso$	gate to source overlay capacitance	F	$1.5e-10$	$1.5e-10$
Cgdo	$Cgdo$	gate to drain overlay capacitance	F	$1.5e-10$	$1.5e-10$
Cgbo	$Cgbo$	gate to bulk overlay capacitance	F	$4e-10$	$4e-10$
N	N	diode emission coefficient		1.0	1.0
Is	Is	leakage current	A	$1e-1$	$1e-14$
Bv	Bv	reverse breakdown voltage	V	100	100
Ibv	Ibv	current at Bv	A	$1e-3$	$1e-3$
Vj	Vj	junction potential	V	1.0	1.0
Cj0	$Cj0$	zero bias depletion capacitance	F	$1e-12$	$1e-12$
M	M	grading coefficient		0.5	0.5
Area	$Area$	relative area		1.0	1.0
Fc	Fc	forward-bias depletion capcitance coefficient		0.5	0.5
Tt	Tt	transit time	s	$0.1e-9$	$0.1e-9$
Xti	Xti	saturation current temperature exponent		3.0	3.0
Kf	KF	flicker noise coefficient		$1e-27$	$1e-28$
Af	Af	flicker noise exponent		1.0	1.0
Tnom	$Tnom$	parameter measurement temperature	$^\circ C$	26.85	26.85
Temp	$Temp$	device temperature	$^\circ C$	26.85	26.85

Appendix 3 [1.b.]

Charge partitioning

The MOSFT is a four terminal device with a dynamic performance that requires accurate calculation of the charge at each terminal. Previous notes indicated that the intrinsic channel charge equals the sum of the drain and source charges. However, the exact proportion of intrinsic channel charge that belongs to the drain or to the source is often not known. The assignment of the proportion of the channel charge to the drain and source charges is called charge partitioning. The first release of the Qucs EKV v2.6 model used the 50/50 partitioning scheme where 50% of the channel charge is arbitrarily assigned to both drain and source. It's interesting to note that this partitioning scheme has no physical basis but depends entirely on convenience. A second partitioning scheme, called the 40/60 partitioning, does however, have a strong physical basis[9]. Yet a third charge partitioning is often employed for digital circuit simulation; this is known as the 0/100 partition. The second release of the Qucs EPFL-EKV v2.6 model includes an extra parameter called Xpart which allows users to set the partitioning scheme for dynamic simulation calculations. Xpart default is set at 0.4 which corresponds to the 40/60 partitioning scheme. Figure 10 illustrates a test circuit for determining the S-Parameters of an nMOS device connected as a capacitance. Both the device capacitance and associated series resistance can be extracted from S[1,1]. Qucs equation block Eqn1 gives the equations for extracting these properties. Other equations in Eqn1 show how the extracted capacitance can be represented as a ratio of the basic parallel capacitance given by

$$C\_parallel\_plate = W \cdot L \cdot Cox. \tag{30}$$

Modelling EKV v2.6 charge partitioning using Qucs EDD

Complex simulation results like those shown in Fig 10 suggest the question "How do we check the accuracy of the model being simulated?". One possible approach is to develop a second model of the same device based on the same physical principles and equations but using a different approach like the Qucs EDD/subcircuit modelling route shown in Fig. 11. It is an EDD/subcircuit model of a long channel EKV v2.6 nMOS device which includes charge partitioning. Figure 12 illustrated the same test circuit as Fig. 10 and the extracted capacitance and resistance values for the EDD model of the long channel nMOS device. A number of features observed from Fig. 10 and Fig. 11 are worth commenting on; firstly that good agreement is recorded between the two sets of results, secondly that the Verilog-A model includes both overlap capacitance and drain and gate source resistances. Hence the slight difference in the capacitance ratio and the recorded values of Rin above one Ohm for the Verilog-A model.

[9]William Liu, MOSFET models for SPICE simulation, including BSIM3v3 and BSIM4, 2001, Wiley-Interscience publications, ISBN 0-471-39697-4.

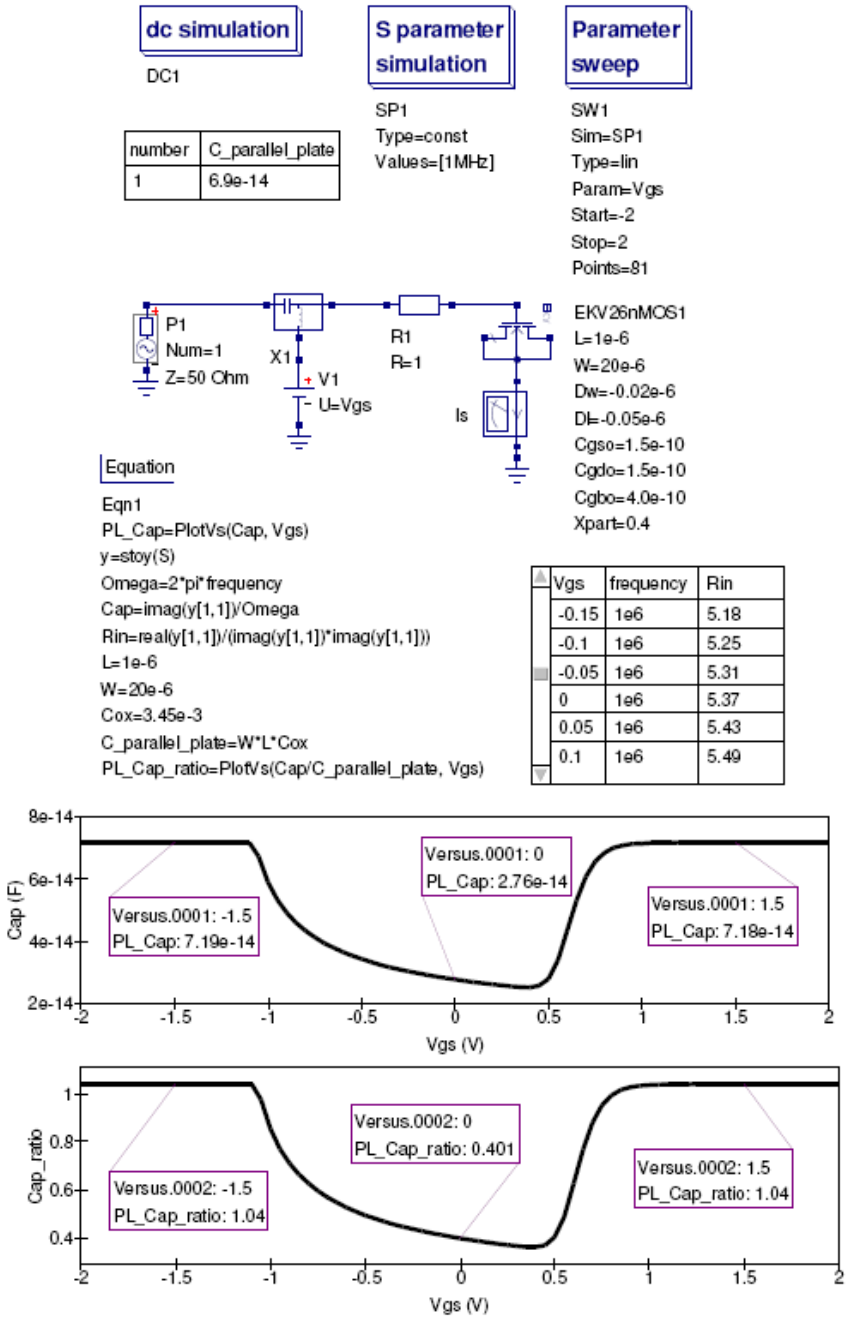


Figure 10: Test circuit for simulating EKV v2.6 charge partitioning effects: Xpart = 0.4 or QD/QS = 40/60

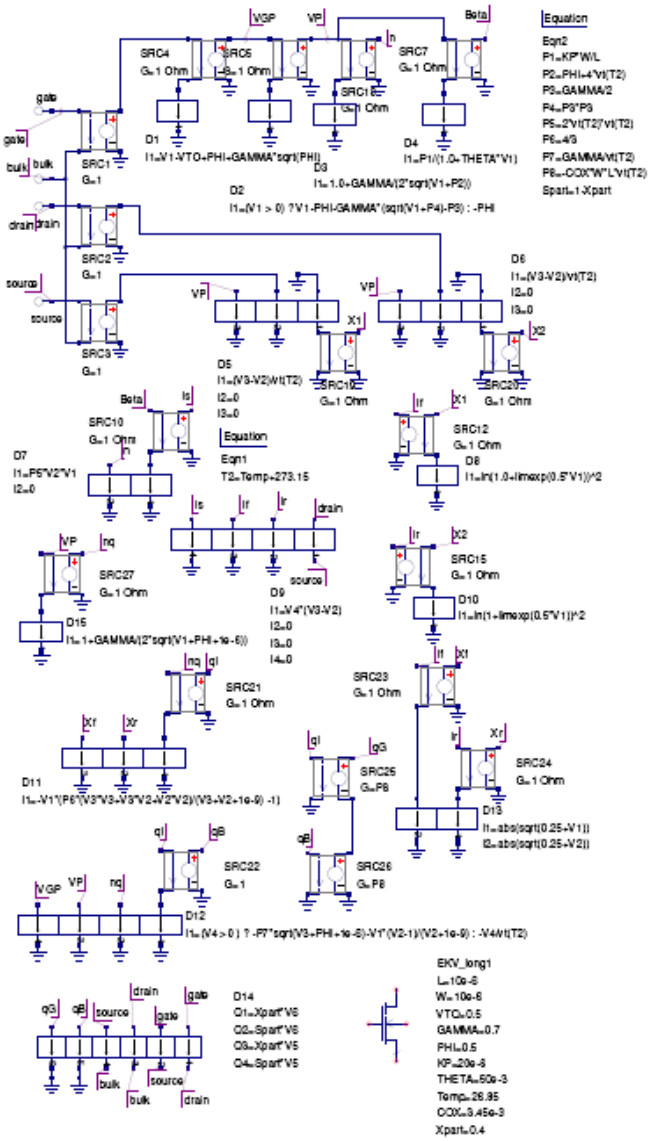


Figure 11: Qucs EDD model for a EKV v2.6 long channel nMOS device with charge partitioning

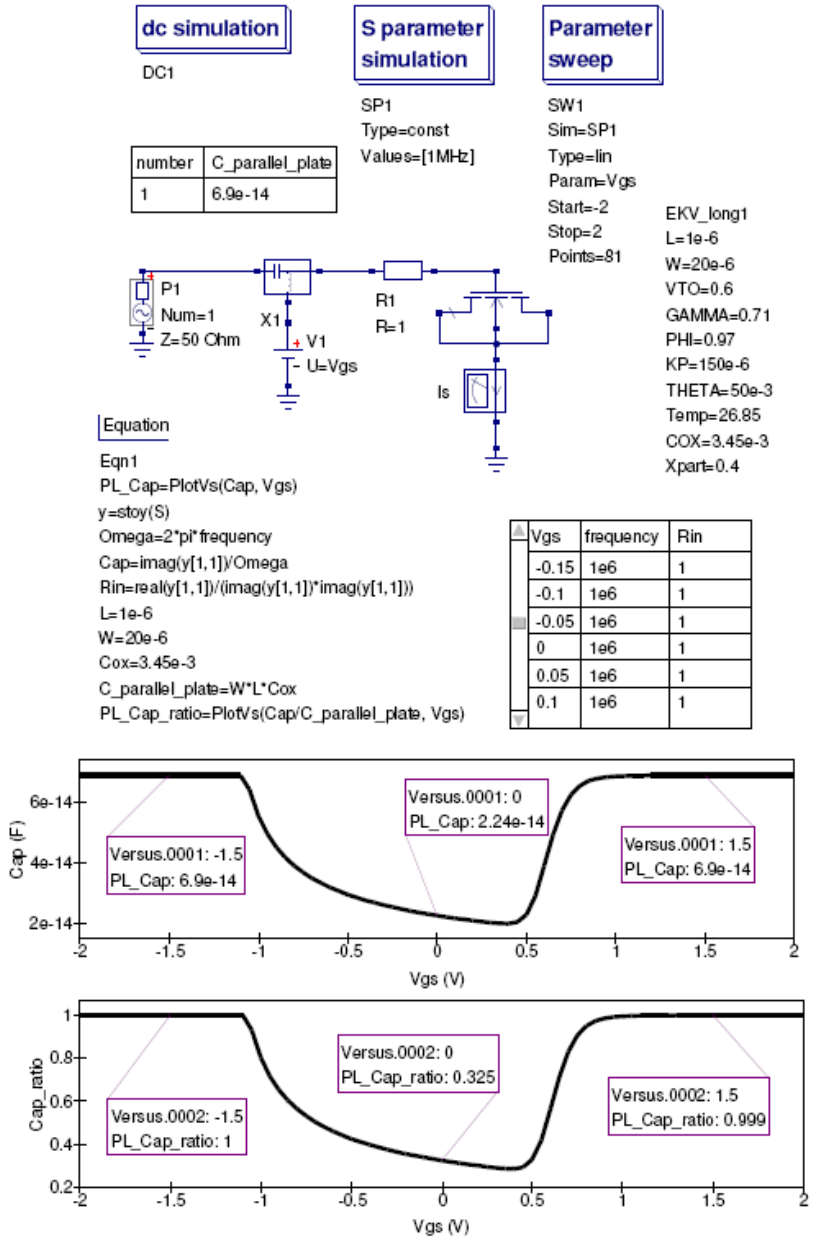


Figure 12: Test circuit for simulating EKV v2.6 EDD model charge partitioning effects: Xpart = 0.4 or QD/QS = 40/60

APPENDIX 4 [26]

Fundamental long channel DC model equations (LEVEL = 1)

<22> $Vg = V(Gate) - V(Bulk)$

<23> $Vs = V(Source) - V(Bulk)$

<24> $Vd = V(Drain) - V(Bulk)$

<33> $VGprime = Vg - Vto + Phi + Gamma \cdot \sqrt{Phi}$

<34> $Vp = VGprime - Phi - Gamma \cdot \left(\sqrt{VGprime + \left[\frac{Gamma}{2}\right]^2} - \frac{Gamma}{2} \right)$

<39> $n = 1 + \frac{Gamma}{2 \cdot \sqrt{Vp + Phi + 4 \cdot Vt}}$

<58, 64> $\beta = Kp \cdot \frac{W}{L} \cdot \frac{1}{1 + Theta \cdot Vp}$

<44> $X1 = \frac{Vp - Vs}{Vt} \qquad If = \left[ln\left\{ 1 + limexp\left(\frac{X1}{2}\right) \right\} \right]^2$

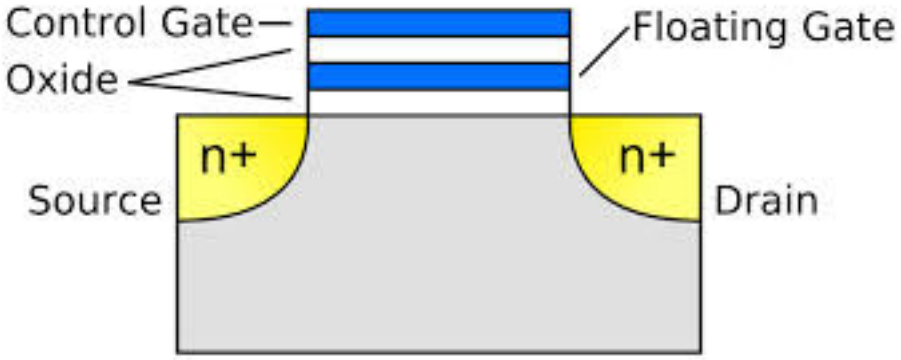
<57> $X2 = \frac{Vp - Vd}{Vt} \qquad Ir = \left[ln\left\{ 1 + limexp\left(\frac{X2}{2}\right) \right\} \right]^2$

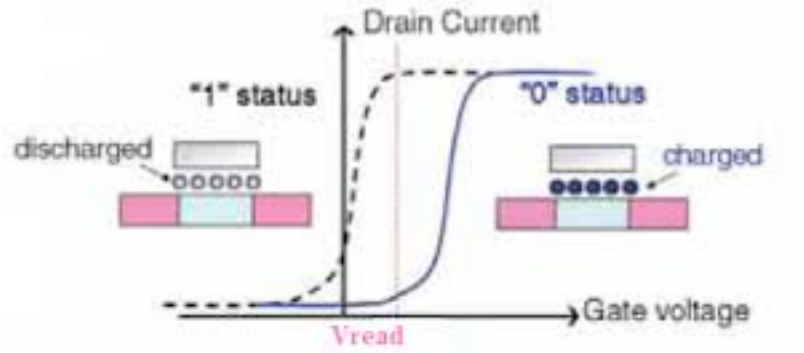
<65> $Ispecific = 2 \cdot n \cdot \beta \cdot Vt^2$

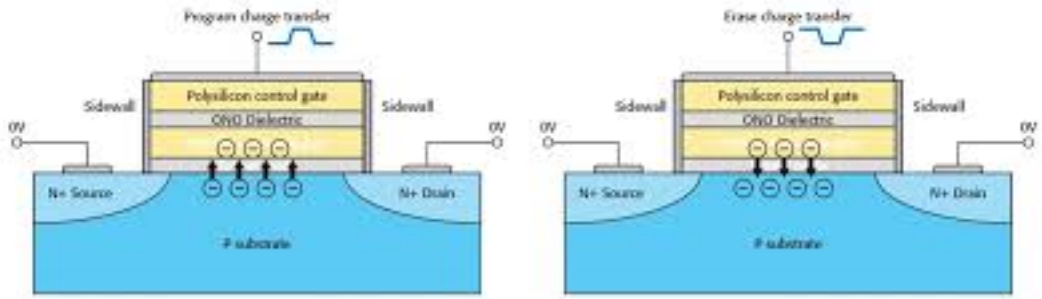
<66> $Ids = Ispecific \cdot (If - Ir)$

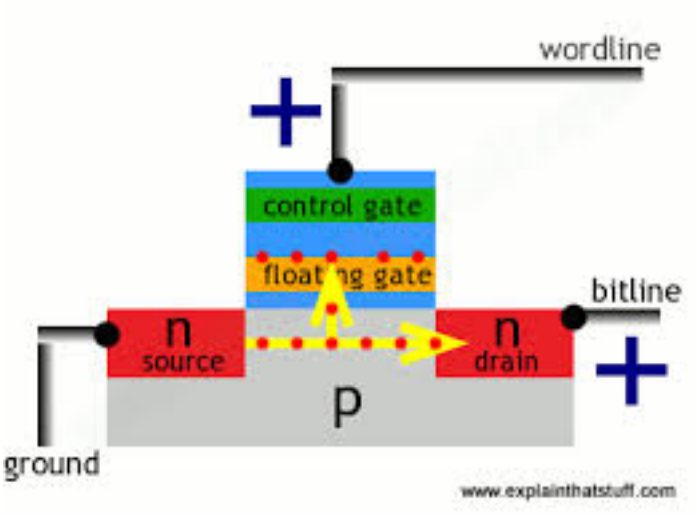
Where *Vgprime* is the effective gate voltage, *Vp* is the pinch-off voltage, *n* is the slope factor, β is the transconductance parameter, *Ispecific* is the specific current, *If* is the forward current, *Ir* is the reverse current, *Vt* is the thermal voltage at the device temperature, *Ids* is the drain to source current. EKV equation numbers are given in"<>" brackets at the left hand side of each equation.

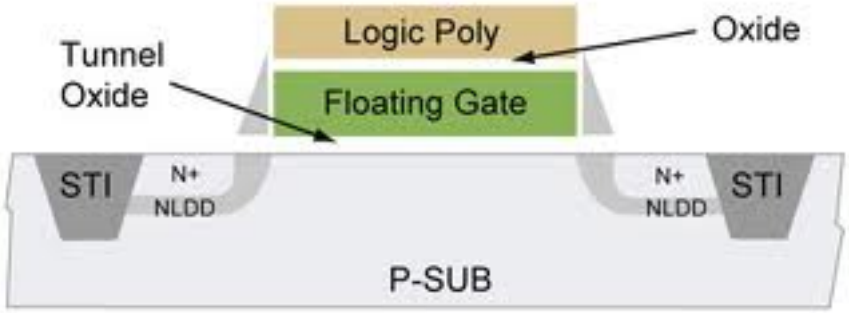
APPENDIX 5

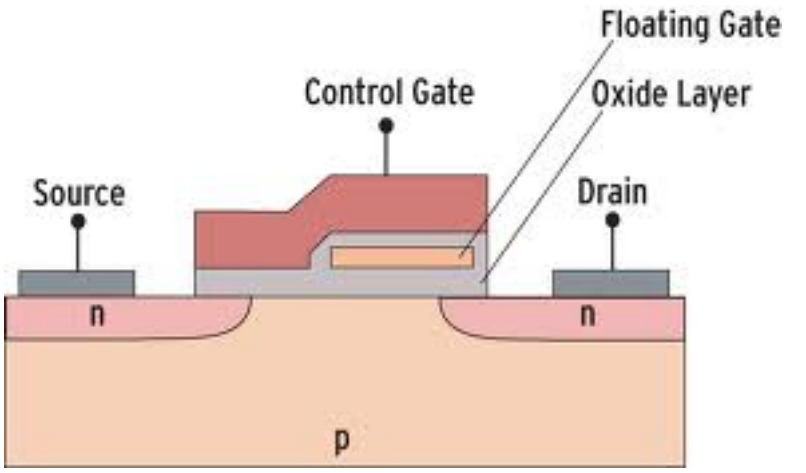

Control Gate
Oxide
Floating Gate
n+
n+
Source
Drain

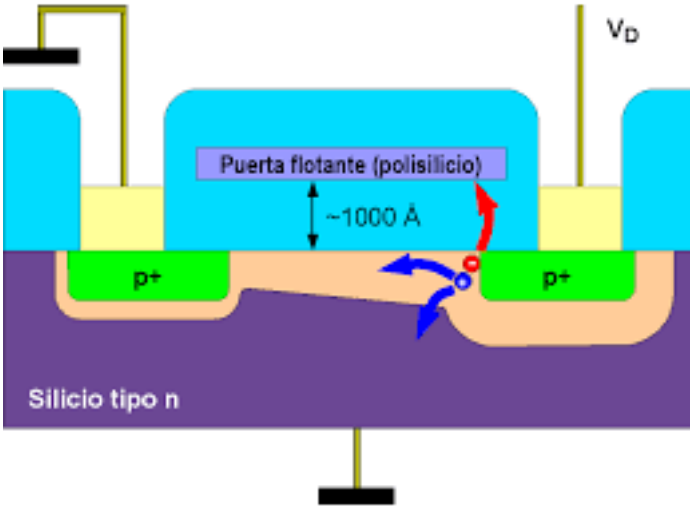

Drain Current
"1" status
"0" status
discharged
charged
Gate voltage
Vread

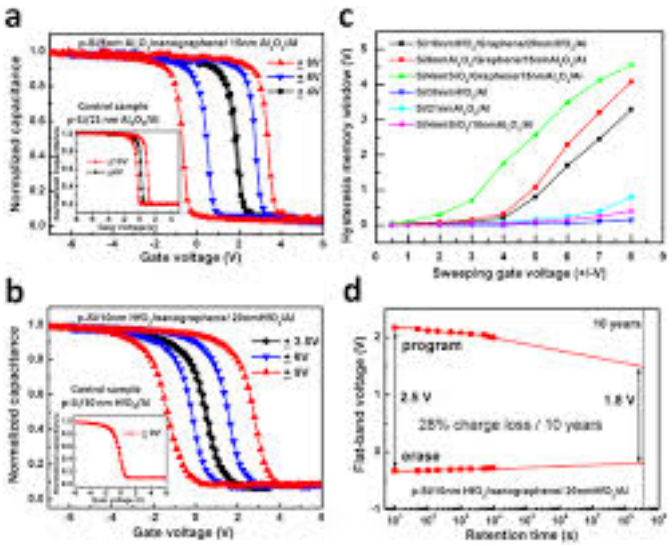

Program charge transfer
Sidewall
Polysilicon control gate
ONO Dielectric
Sidewall
0V
0V
N+ Source
N+ Drain
P substrate
Erase charge transfer
Sidewall
Polysilicon control gate
ONO Dielectric
Sidewall
0V
0V
N+ Source
N+ Drain
P substrate


wordline
control gate
floating gate
bitline
n
source
n
drain
p
ground
www.explainthatstuff.com


Logic Poly
Oxide
Tunnel
Oxide
Floating Gate
STI
N+
NLDD
N+
NLDD
STI
P-SUB


Floating Gate
Control Gate
Oxide Layer
Source
Drain
n
n
p


V_D
Puerta flotante (polisilicio)
~1000 Å
p+
p+
Silicio tipo n


a
c
b
d
Gate voltage (V)
Sweeping gate voltage (+I-V)
Gate voltage (V)
program
erase
2.6 V
1.8 V
25% charge loss / 10 years
10 years
Retention time (s)

APPENDIX 6

Simulation Results Tables