6.2. General schematic circuit modelling.

The schematic construction, simulation and results display for QUCS for standard circuits using library elements is similar to SPICE with a typical circuit being shown in Fig.6.2.1, reference [6] for specific procedure.

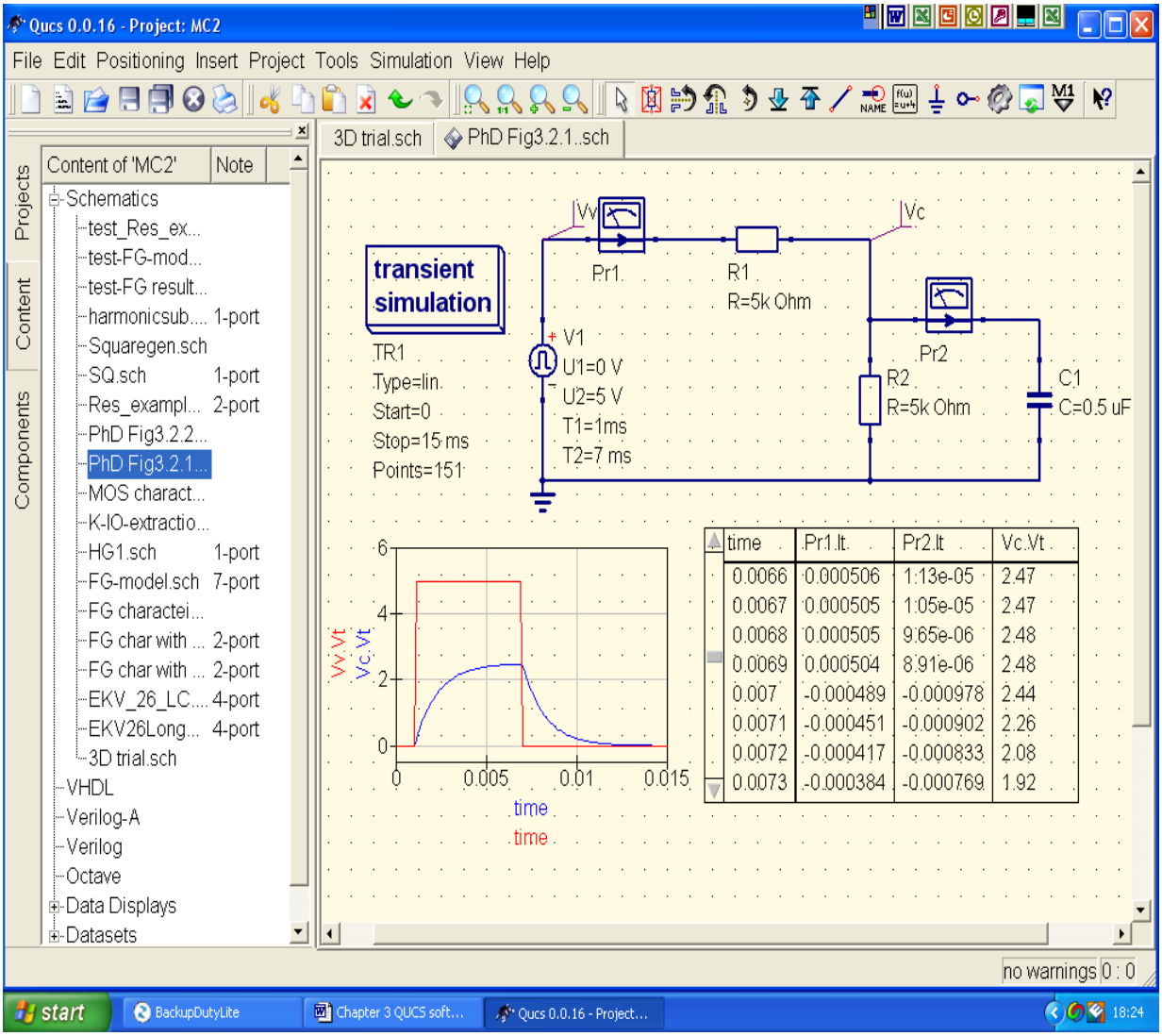

Fig.6.2.1. QUCS Transient response for RC network

The circuit in Fig.6.2.1, shows an edited transient simulation response to an edited applied voltage pulse connected to edited components from the QUCS library. The circuit has been simulated and shows tabulated and 2-dimensional responses. Within the library, available components can be seen up to QUCS version 0.0.16. for the version used for this work. The library is quite extensive and is being gradually

built up and it is intended that this work will add FGMOS devices. For the requisite responses it is often necessary to use equations to get the appropriate results. Mathematical equations can be created using the operators within QUCS and then graphical plots are obtained, either 2- or 3-dimensions being available. Fig.6.2.2, shows the response in a 3-dimensional format for the input pulse being swept over a range of voltages. Also shown is the use of the equation function where the mathematical operator **Diff** is used to obtain the rate at which the voltage across the capacitor is changing.

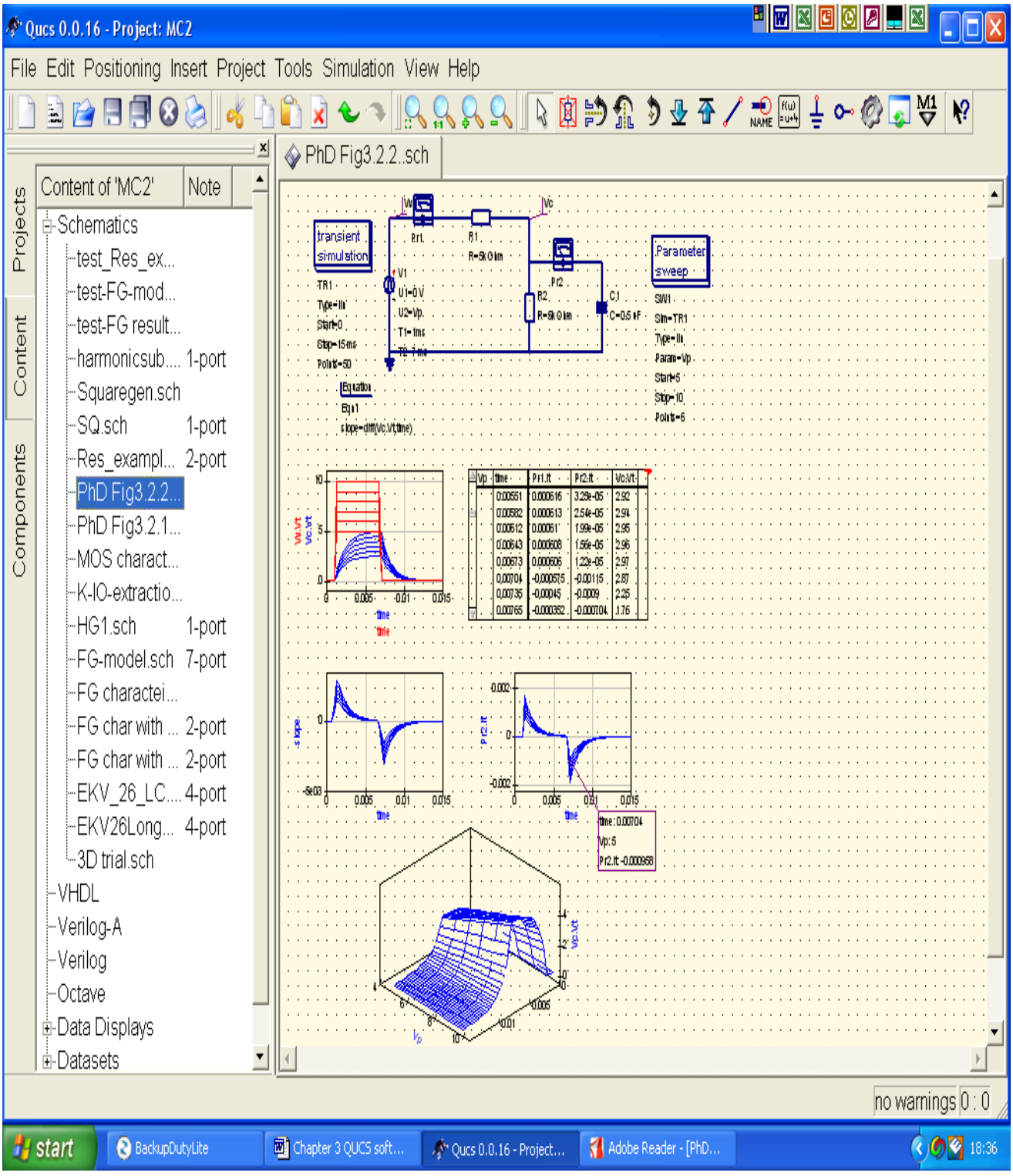

Fig.6.2.2. 2- and 3-dimensional responses for Vp sweep from 5 – 10V

6.3. Subcircuits

Subcircuits are an extremely common aspect of circuit simulators. However until recently many, including SPICE 2g6 and 3f5, did not allow parameters to be passed to the subcircuit. This restriction was removed from QUCS with version 0.0.11. so that parameters attached to circuit symbols could be used for subcircuit equation calculations. By using embedded design equations within subcircuits and parameter passing, it became possible to construct models with a combination of design procedures and the calculation of the values of individual components. As explained earlier with the release of version 0.0.12 the voltage, current and charge restrictions on equations were finally relaxed.

Fig.6.3.1. shows an example of a harmonic generator that could be created as a subcircuit.

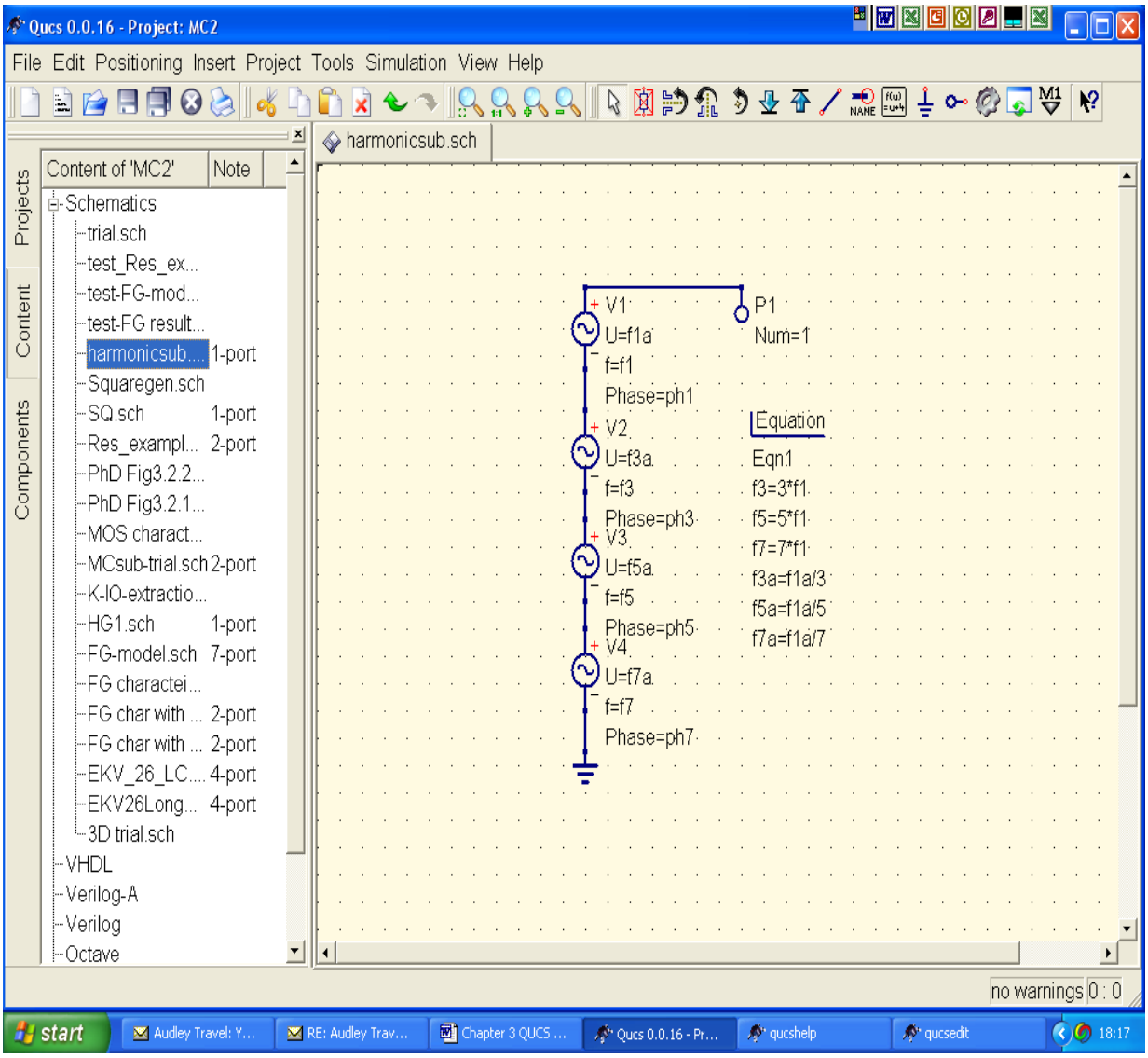

Fig.6.3.1. Subcircuit for square wave generator

Fig.6.3.2. shows a screen dump for a subcircuit created in Fig.6.3.1. that allows a sinewave to be squared. When the circuit is saved the port, P1, indicates that it is a subcircuit. This subcircuit can be pulled in to a new schematic area either as a circuit in it's own right or as part of a larger circuit. Fig.6.3.2, shows the subcicuit and the default parameters and the corresponding output.

If required the subcircuit symbol can be personalised. This may be achieved by going to the menu: **File → Edit Circuit Symbol**. From this the subcircuit symbol can be edited by means of the using **Paintings** and saved as such.

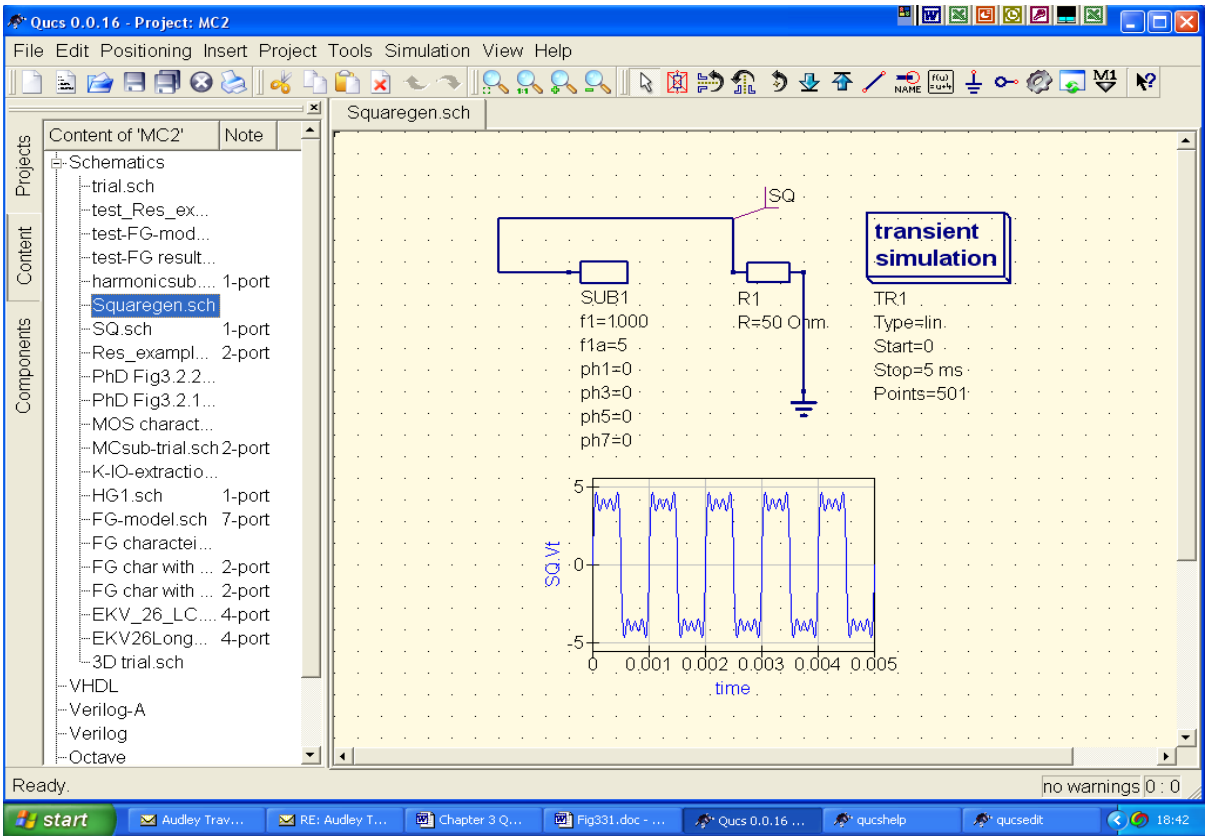

Fig.6.3.2. Use of subcircuit SUB1 for output

However it is by means of being incorporated as part of larger circuits that it shows it's true potential.

QUCS subcircuits can be nested to an arbitrary level and parameters can be passed down the nested subcircuits to any level required.

With the use of subcircuits universal macromodels can be built incorporating subcircuits that have had parameters passed to them.

6.4. Equation Defined Devices (EDD).

EDDs can be considered to be a fast interactive model prototyping method whose equations can be easily expressed in Verilog-A and compiled into C/C++ code for permanent inclusion in the QUCS simulator.

Symbolic equations enable a simulator to merge circuit design and analysis. Further if these equations are made functions of circuit variables then it turns the simulator into an extremely powerful tool. The accuracy required of modern microcircuits and devices demands detailed models taking into account the fundamental physical structures and parameters of the fabrication process. QUCS version 0.0.12 introduced an equation defined device that allows it's terminal current to be functions of voltage, and it's stored charge to be functions of voltage and current [10]. The EDD is capable of modelling complex compact devices. Because of the advanced nature of the EDD, it was thought appropriate to formulate the analysis of the operation and create a model for an adaptable Floating Gate MOS device. The modelling equations for a FGMOS need to be explicit in order to be used by EDDs in the QUCS environment.

Fig.6.4.1, shows an example of an EDD which multiplies two sinewaves, though the output can be considered the product of and two input voltage waveforms.

$$V_{out}(VIN_1, VIN_2) = VIN_1.VIN_2 \quad \ldots\ldots \quad (6.4.1)$$

This is an example of allowing the terminal currents to be functions of voltage. A current I1 is generated that is equal to the product of the terminal voltages V2 . V3. To complete the operation this current is converted to an output voltage, V*out*, by the use of a unity gain current controlled voltage source.

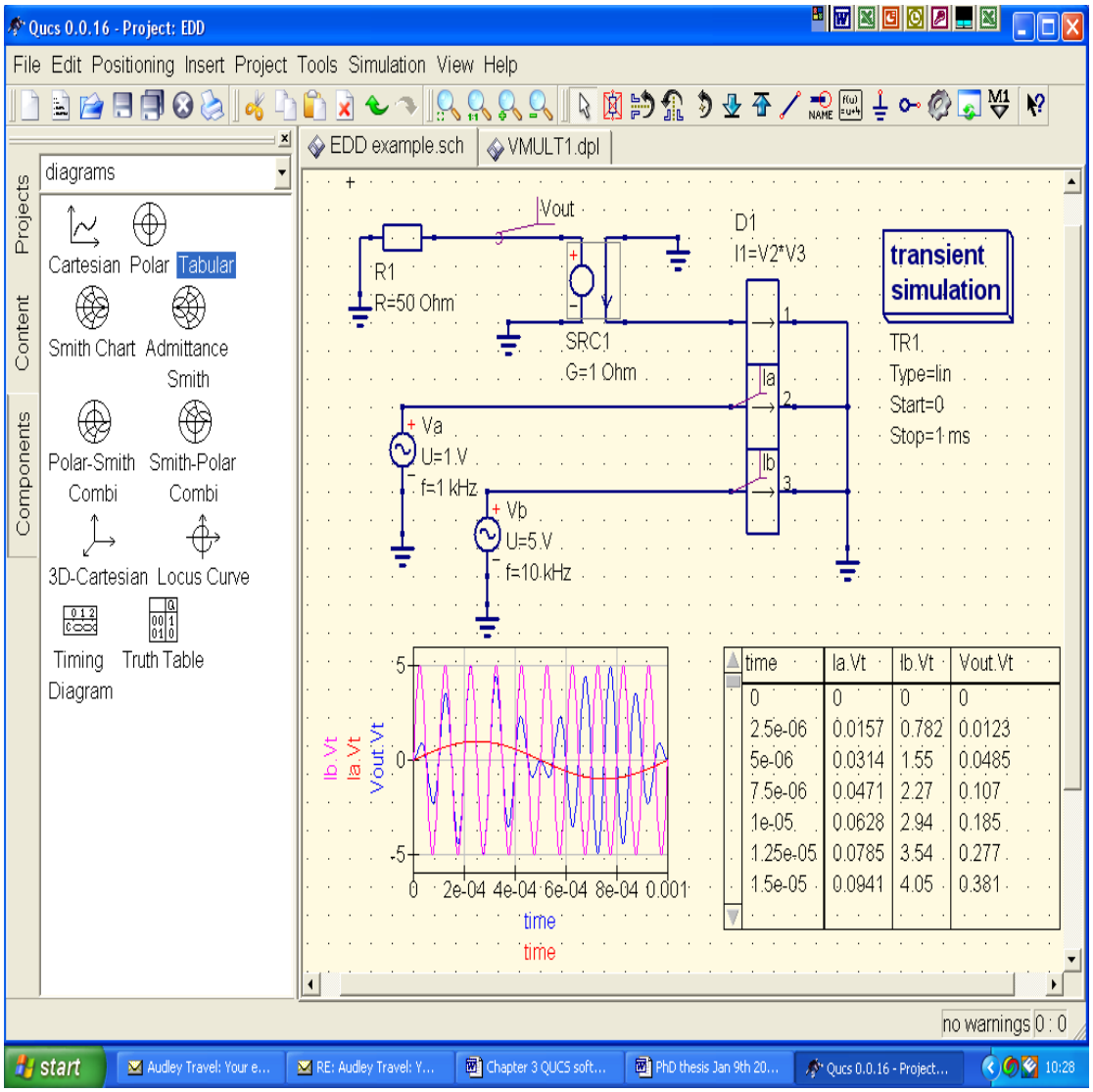

Fig.6.4.1. EDD Multiplication of two sinewaves

6.5. Compact Device modelling using EDD

The use of compact semiconductor models is an essential tool for circuit simulators. Models for semiconductor devices have been built upon since their original inception and most modern simulators are characterised by the same parameters used in SPICE 2g6 and SPICE 3f5. EDDs have been introduced to enable fast, easily implementable prototyping of semiconductor devices for QUCS software users. Following is an example of a compact model of a diode that can be referenced from

[4] and is included so the EKV v2.6 model and floating gate model may be understood more fully.

The D.C. diode current, I_d, can be expressed by the following functions of diode voltage, V_d, these are equations from the SPICE 2g6 diode model [34].

$$I_d = I_s.\left(exp\left(V_d/(n.V_t)\right) - 1\right) + V_d.GMIN, \quad \forall(-5.n.Vt \leq V_d) \quad \ldots\ldots \quad (6.5.1)$$

$$I_d = -I_s + V_d.GMIN, \quad \forall(-BV < V_d) \text{ and } (V_d < -5.n.Vt \leq V_d) \quad \ldots\ldots \quad (6.5.2)$$

$$I_d = -BV, \quad \forall(V_d = -BV) \quad \ldots\ldots \quad (6.5.3)$$

$$I_d = -I_s.\left(exp\left(-\frac{(BV + V_d)}{Vt}\right) - 1 + BV/Vt\right), \quad \forall(V_d < -BV) \quad \ldots\ldots \quad (6.5.3)$$

Where:-

- I_s =the saturation current
- *N = the emission coefficient*
- *GMIN* = a small conductance in parallel with the diode to help QUCS with the DC convergence
- *Vt* = *k*B.T/q, where T= diode temperature in Kelvin, *k*B = Boltzmann's constant and q = electronic charge
- *BV* = reverse breakdown voltage (ve+)
- *IBV* = reverse breakdown current (ve+)

Fig.6.5.1. shows the EDD model for the semiconductor diode. The diode current is the sum of EDD branch currents I_1 to I_4 where:-

- I_1 the current in the forward bias region
- I_2 the current in the reverse bias region
- I_3 plus I_4 the reverse bias breakdown region

When calculating the diode current a function called limexp() is used to help QUCS to converge to a solution during D.C. and transient analysis.

Results for a simulation of the EDD and the QUCS version of the SPICE model are shown that are an extremely close match in the forward bias direction but deviate slightly in the reverse bias direction at breakdown. This is due to the SPICE model not modelling the Zener breakdown as effectively as QUCS.

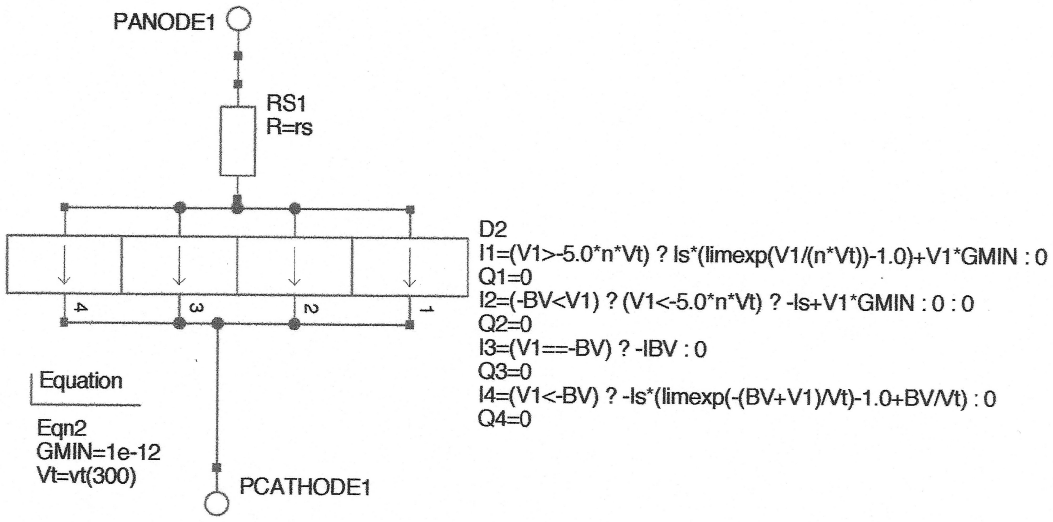

Fig.6.5.1.a. EDD representation of model diode

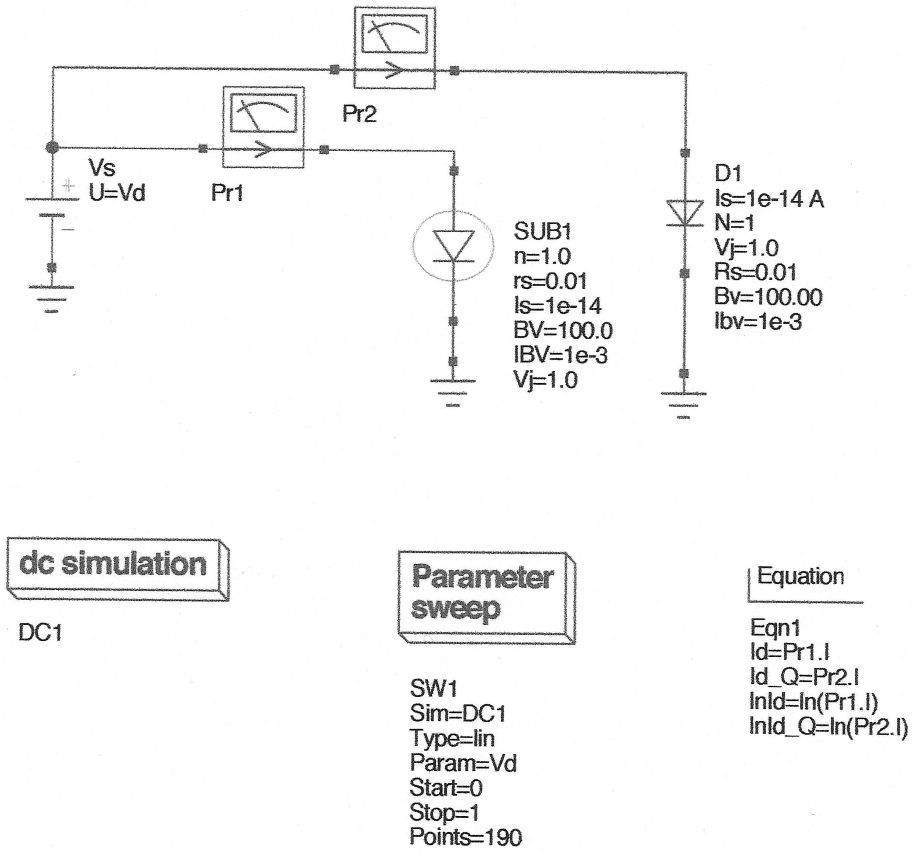

Fig.6.5.1.b. Schematic for diode test circuit for EDD QUCS and equivalent SPICE models

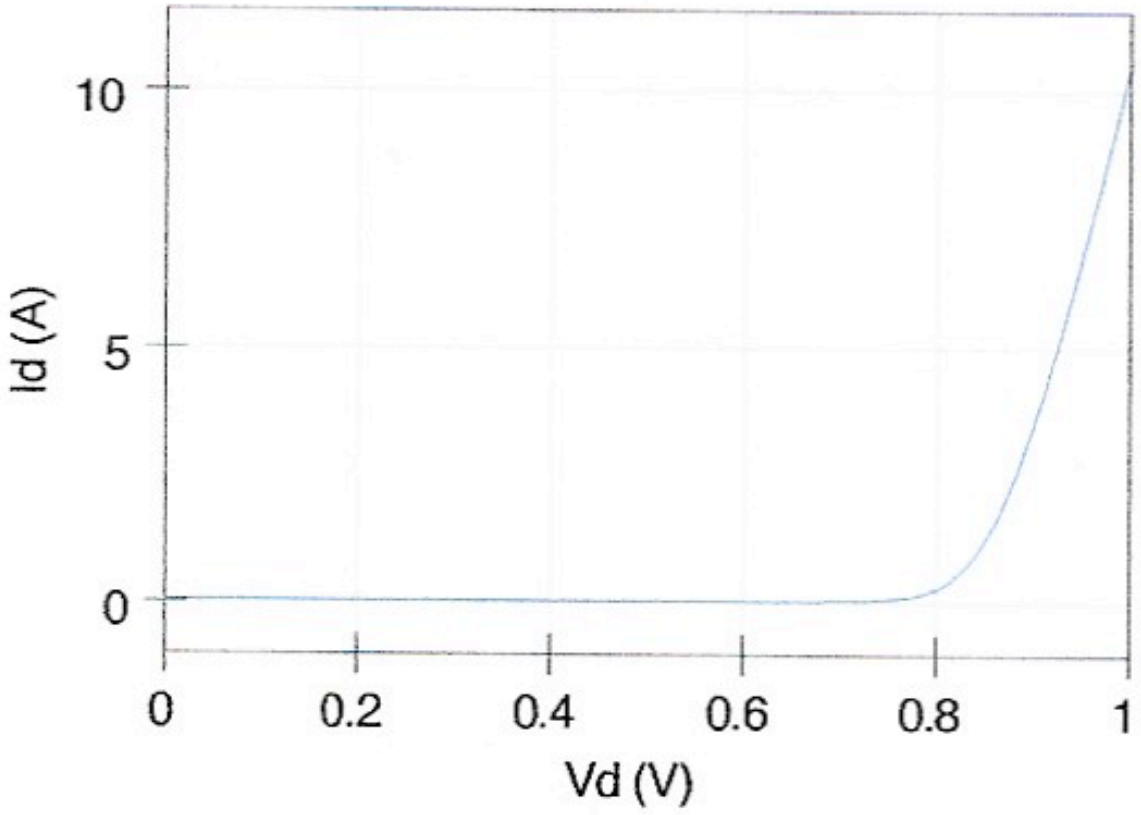

Fig.6.5.2.a. Forward bias SPICE model V_d v I_d

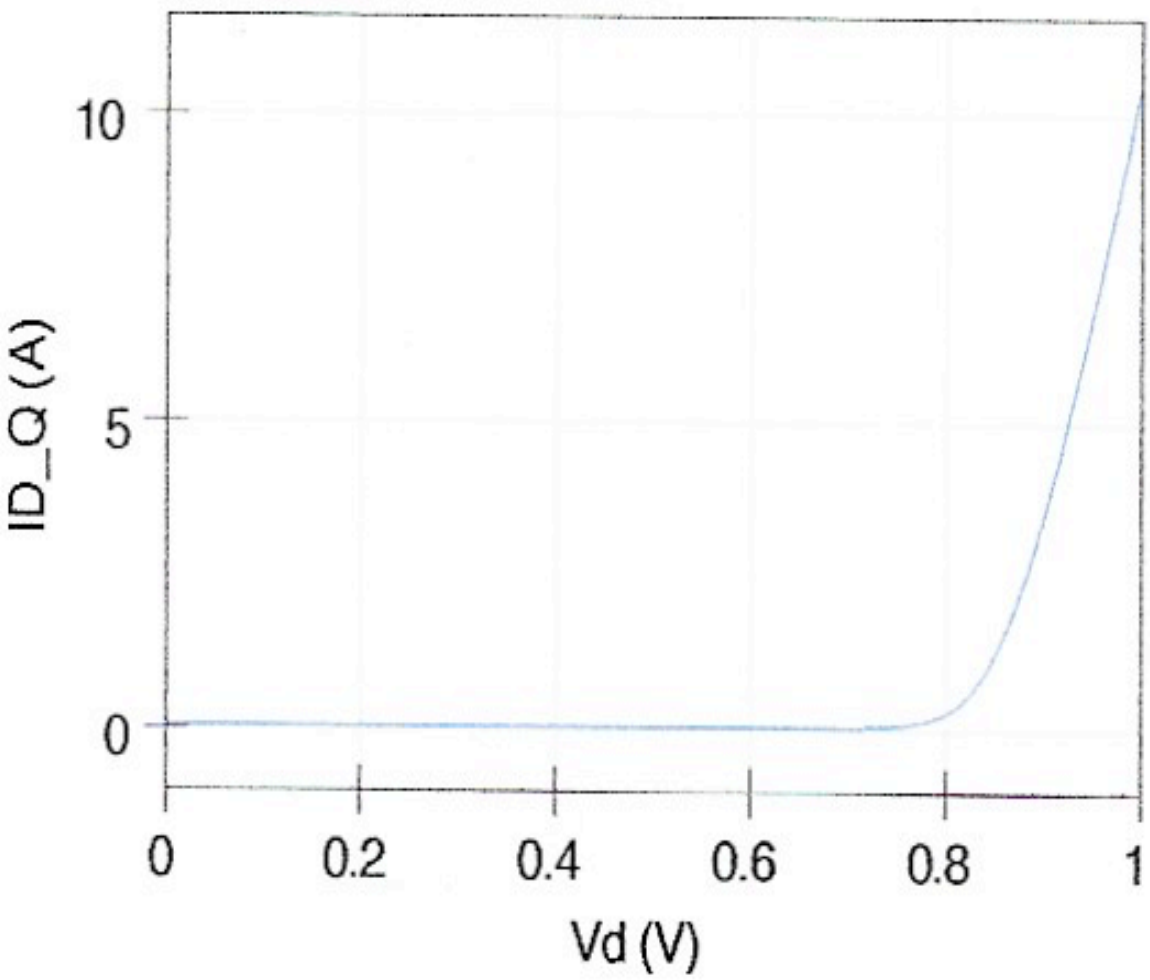

Fig.6.5.2.b. Forward bias QUCS model V_d v I_d

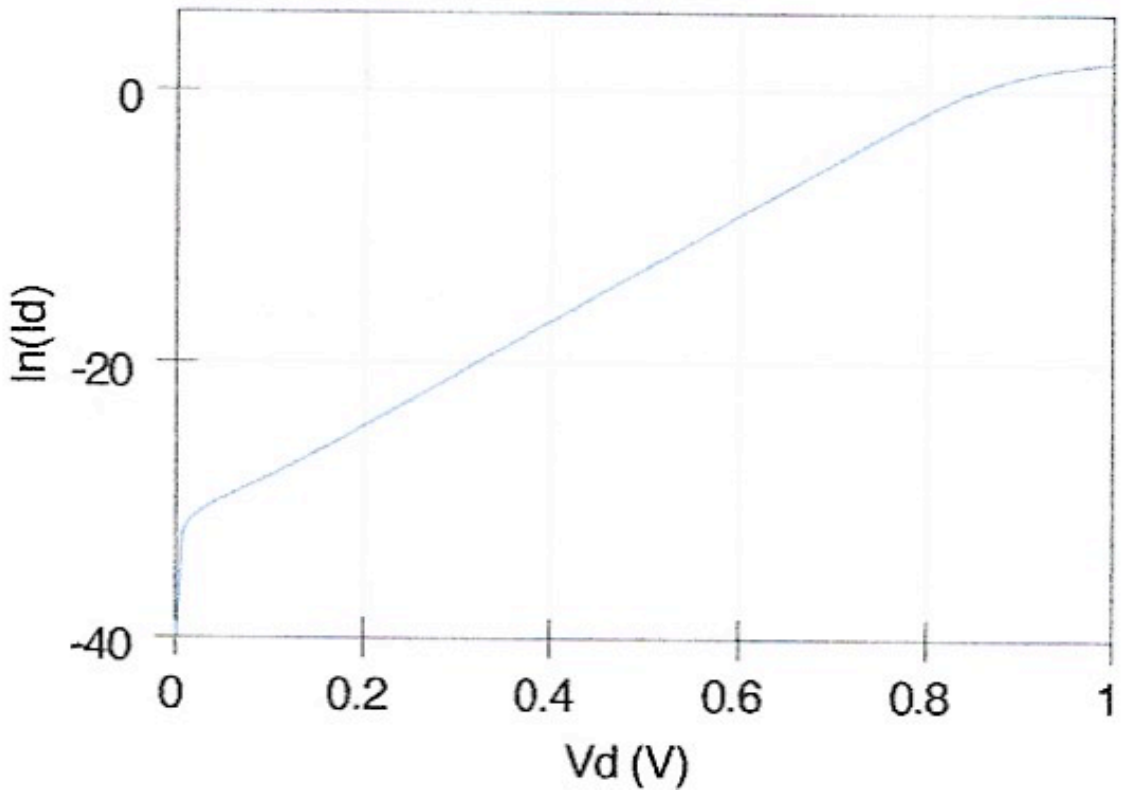

Fig.6.5.2.c. Forward bias SPICE model V_d v (ln)I_d

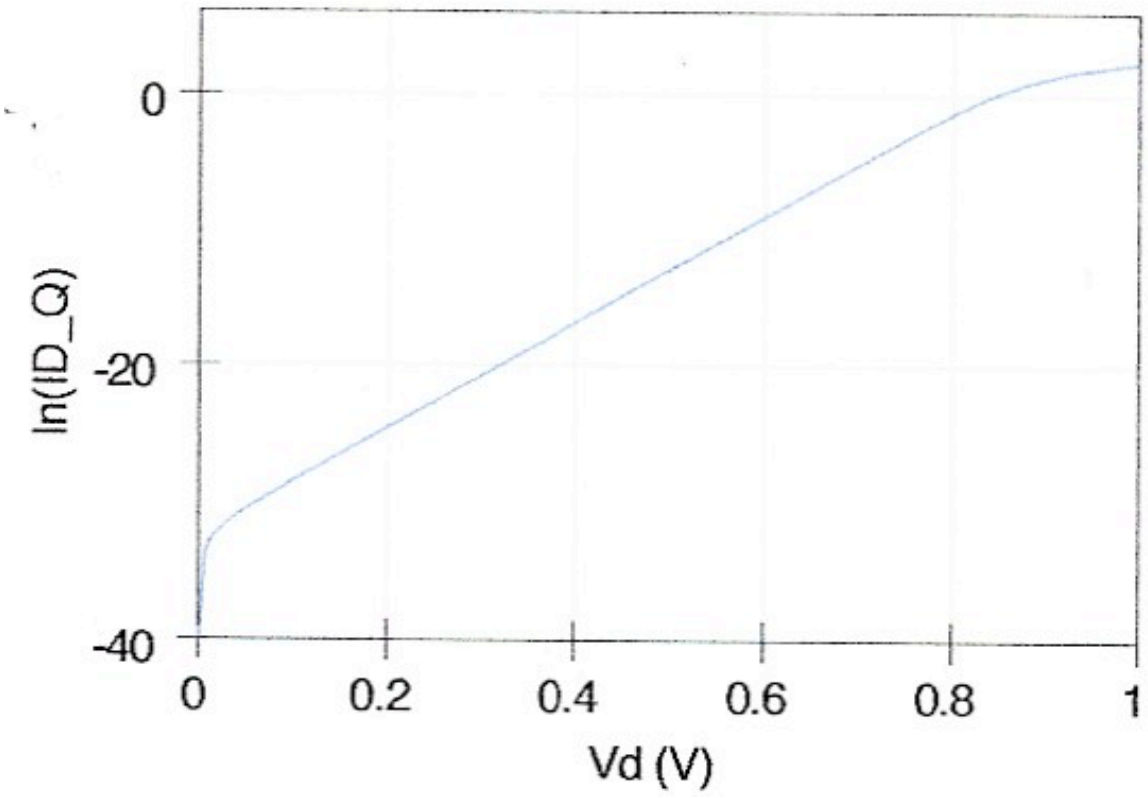

Fig.6.5.2.d. Forward bias QUCS model V_d v (ln)I_d

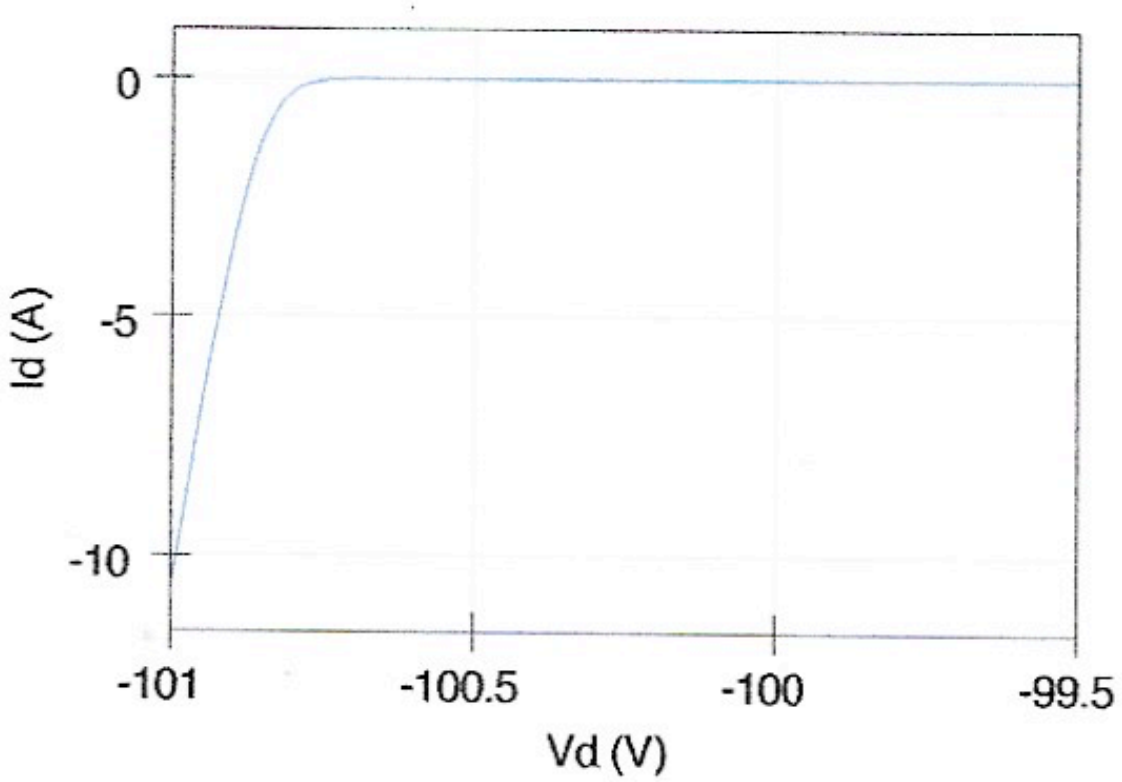

Fig.6.5.2.e. Reverse bias Zener Breakdown for

SPICE model V_d v I_d

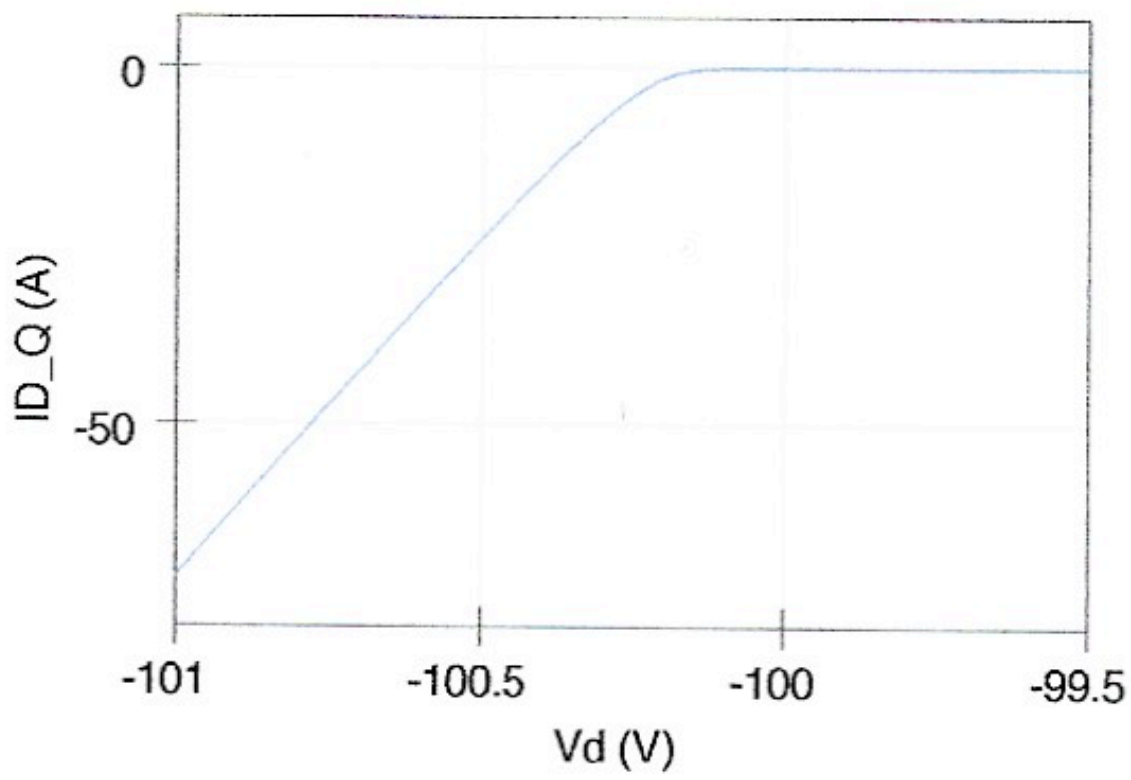

Fig.6.5.2.f. Reverse bias Zener Breakdown for

QUCS Model V_d v I_d

The two models show a high degree of matching in the forward bias direction and in the reverse bias direction up to approximately -100V. However when Zener breakdown starts to take place the QUCS model is more representative of actual operation.

6.6 Implementation of the EKV v2.6 Long Channel MOSFET Model

For the FG MOSFET the EKV long channel device was selected as the most appropriate structure for the inclusion of the floating gate because of the dimensional requirements of the floating gate itself. However once a model had been established other structures will be able to be analysed with relative ease. The model for the long channel device using non-linear equation defined devices were developed in 2007 using the QUCS Verilog-A compact device route [10] and the Verilog-A code for the

QUCS ADMS compiled version of the EKV v2.6 model is given in Appendix 1. These equations and schematic representations are developed in chapter (7)

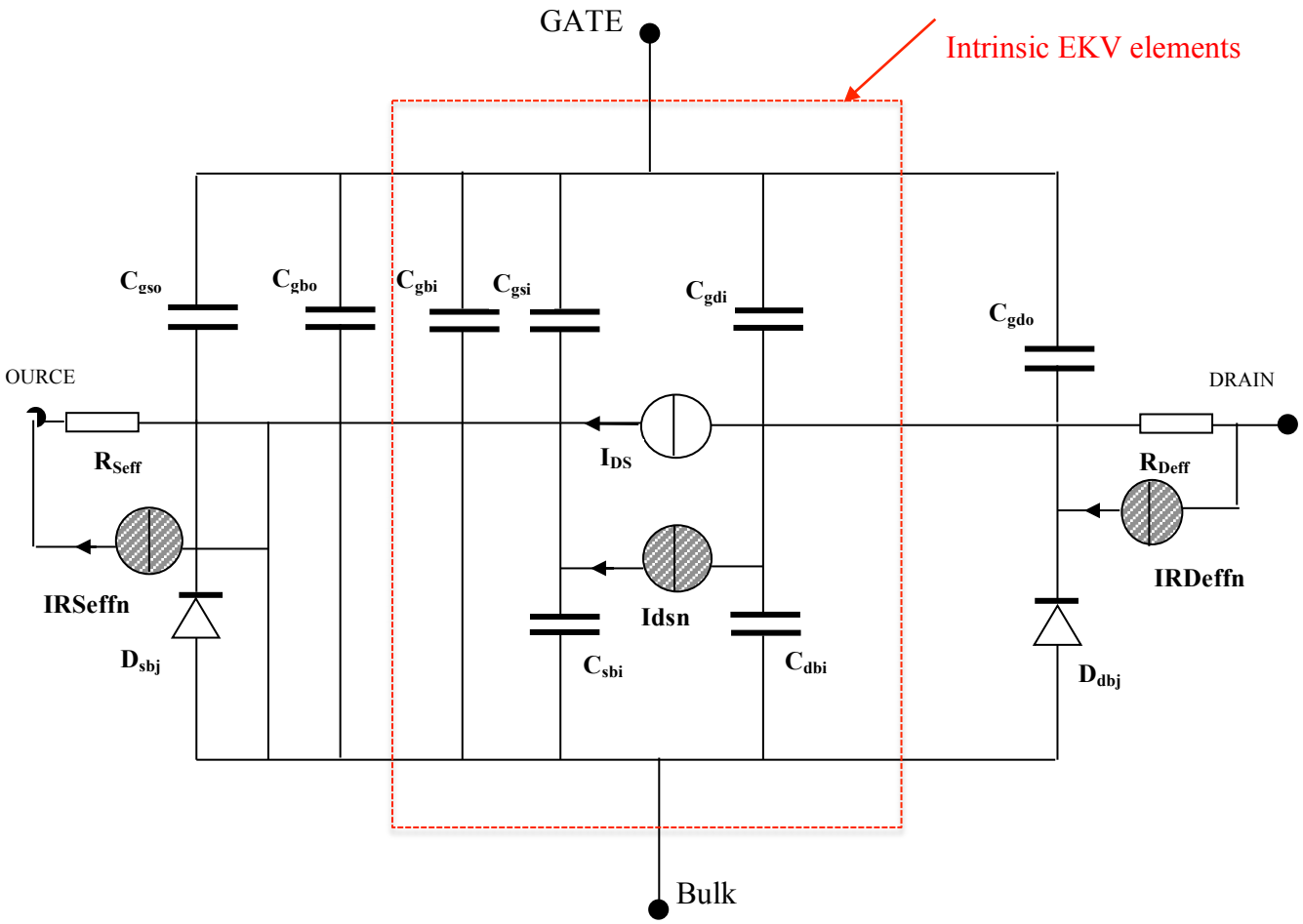

Fig.6.6.1. QUCS EKV v2.6 long channel nMOSFET Equivalent Circuit.

The equivalent circuit used for the QUCS EKV v2.6 long channel is shown in Fig.6.6.1. The separation of the extrinsic and intrinsic device, is denoted by the red dashed line, with the extrinsic components representing the physical connections of the device. The parameters are given in Appendix 2 and equivalent circuit equations in Appendix 4.

Table 6.6.1. EKV simulation model equivalent circuit model

Name	Description
C_{gso}	Gate –source overlap capacitance
C_{gbo}	Gate-base overlap capacitance
C_{gsi}	Intrinsic gate-source capacitance
C_{gdi}	Intrinsic gate-drain capacitance
C_{gdo}	Gate-drain overlap capacitance
C_{sbi}	Intrinsic source-substrate capacitance
C_{dbi}	Intrinsic drain-substrate capacitance
I_{DS}	Drain-source current
R_{Seff}	Source series resistance
R_{Deff}	Drain series resistance
D_{sbj}	Source-substrate junction diode
D_{dbj}	Drain-substrate junction diode

6.7. QUCS EKV v2.6. Long Channel nMOSFET EDD implementation

The EKV v2.6 MOSFET model is a physics based model that has been placed in the public domain by its developers,and it is ideal for submicron CMOS circuits.

The development equations were taken from ref. [10] which in turn were developed from ref.[22] which was presented as a paper at the MOS-AK Meeting, IHP, Frankfurt (Oder), Germany in April 2009[2].

For the EKV long channel nMOSFET shown in Fig.6.6.1. the red dashed box indicates the intrinsic elements and those outside represent the physical components connecting to the outside terminals.

For the EDD D.C. implementation of the EKVv2.6 long channel nMOSFET, the EPFL characteristic equations (Level 1)[4] are used. The interconnections of these EDD (Fig.6.7.1.) blocks are then used in order to create a macro block (Fig.6.7.2.) that is then used for further development of the intrinsic charge characteristics of the device. The schematic representation for this macromodel is shown in Fig.6.7.3.

$$Vg = V(gate) - V(bulk), \qquad Vs = V(source) - V(bulk), \qquad Vd = V(drain) - V(bulk) \quad \text{... 6.7.1.a.b.c.}$$

$$VGprime = Vg - VT0 + PHI + GAMMA.\sqrt{PHI} \quad \text{... ...} \quad 6.7.2.$$

$$Vp = VGprime - PHI - GAMMA.\left[\sqrt{VGprime + \left(\frac{GAMMA}{2}\right)^2} - \frac{GAMMA}{2}\right] \quad \text{....} \quad 6.7.3.$$

$$n = 1 + \frac{GAMMA}{2}.\sqrt{VP + PHI + 4.Vt} \quad \text{....} \quad 6.7.4.$$

$$BETA = KP.\frac{W}{L}.\frac{1}{1 + THETA.VP} \quad \text{....} \quad 6.7.5.$$

$$X1 = \frac{Vp - Vs}{Vt} \quad \text{....} \quad 6.7.6.$$

$$If = \left|\ln(1 + \text{limexp}(X1/2))\right|^2 \quad \text{....} \quad 6.7.7.$$

$$X2 = \frac{Vp - Vd}{Vt} \quad \text{....} \quad 6.7.8.$$

$$Ir = \left|\ln(1 + \text{limexp}(X2/2))\right|^2 \quad \text{....} \quad 6.7.9.$$

$$Ispecific = 2.n.BETA.vt^2 \quad .... \quad 6.7.10.$$

$$Ids = Ispecific.(If - Ir) \quad .... \quad 6.7.11.$$

Transferring these equations into EDD blocks we get the configuration shown in Fig.6.7.2. for the DC characteristic.

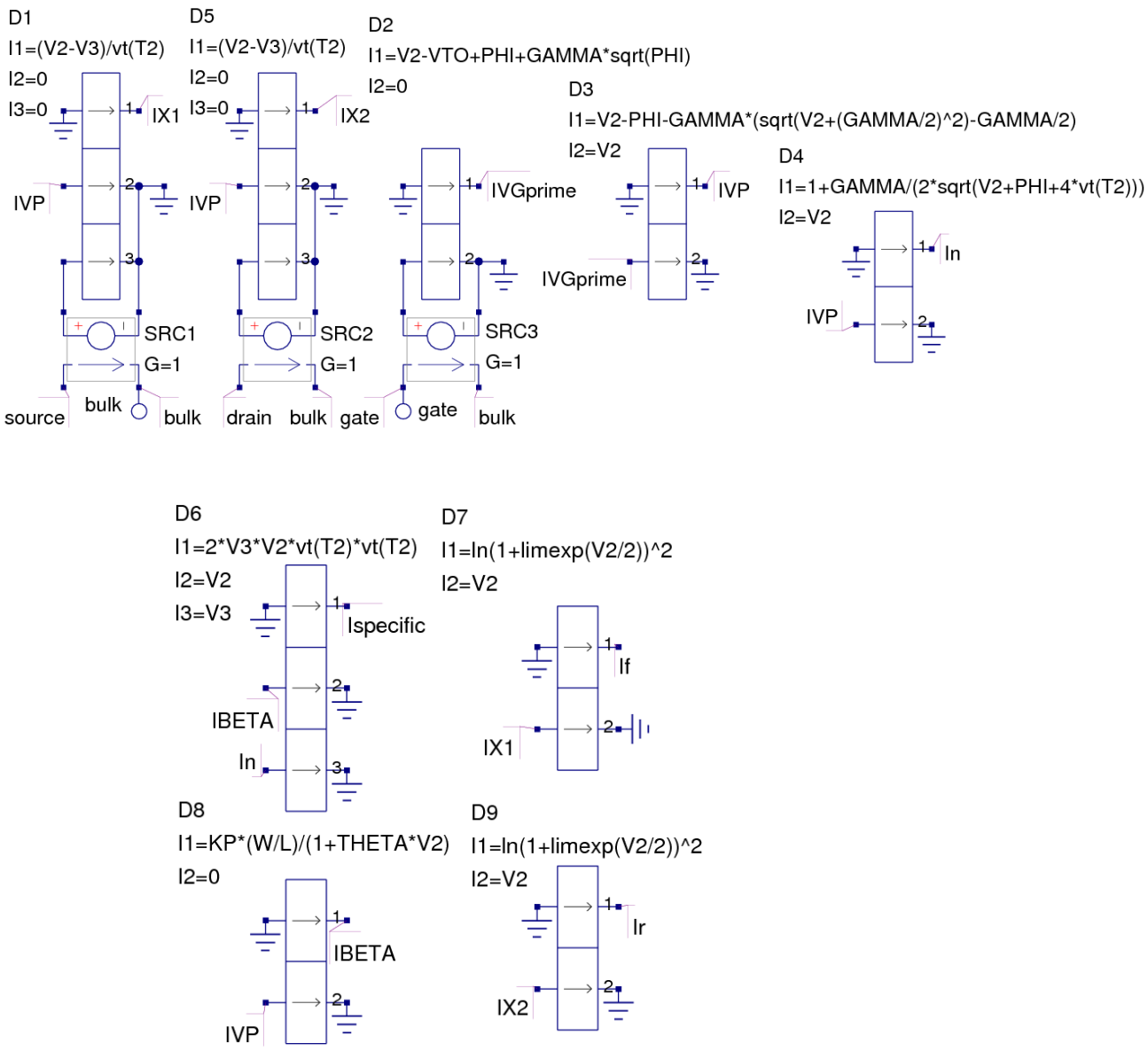

Fig.6.7.1. EDD blocks representing the EKVv2.6 equations 6.7.1 – 6.7.11.

The overall EDD representation is as shown in Fig.6.7.2.:-

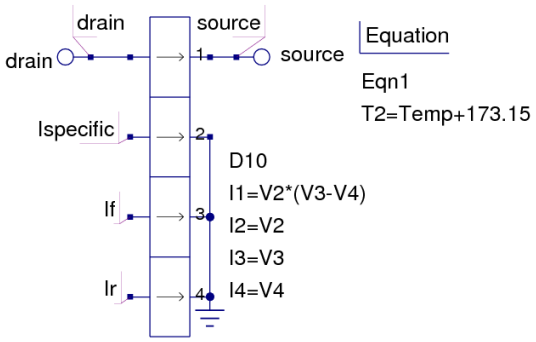

Fig.6.7.2. Amalgamation of EDD blocks D1 – D9 into a single EDD block

Symbolic representation in QUCS library including some associated parameters (remainder take on the default values).

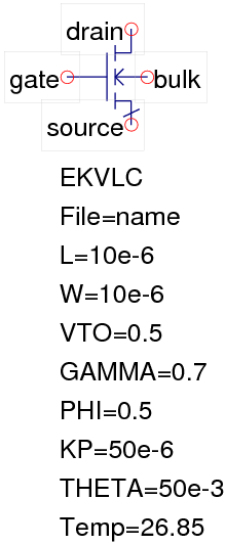

Fig.6.7.3. QUCS equation based model for DC characteristics

QUCS equation based model including charge characteristics[4].

Associated equations:_

$$nq = 1 + \frac{GAMMA}{2.\sqrt{VP + PHI + 1e-6}} \quad \ldots\ldots \quad (6.7.12)$$

$$Xf = \sqrt{0.25 + If} \quad \ldots\ldots \quad (6.7.13)$$

$$Xr = \sqrt{0.25 + Ir} \quad \ldots\ldots \quad (6.7.14)$$

$$qI = -nq.\left[\frac{4}{3}.\frac{(Xf^2 + Xf.Xr + Xr^2)}{Xf + Xr}\right] - 1 \quad \ldots\ldots \quad (6.7.15)$$

$$qB = \frac{-GAMMA.\sqrt{VP + phi + 1e-6}}{vt} - \left[nq - \frac{1}{nq}\right], \text{ when } VGprime > 0 \quad \ldots\ldots \quad (6.7.16)$$

$$qB = \frac{-VGprime}{vt}, \quad \text{when} \quad VGprime \leq 0 \quad \ldots\ldots \quad (6.7.17)$$

$$qG = -qI - qB, \quad \ldots\ldots \quad (6.7.18) \qquad Q(I,B,D,S,G) = Cox.vt.q(I,B,D,S,G) \quad \ldots (6.7.19)$$

Transferring these equations into EDD blocks we get the configuration shown in Fig.6.7.4. for the intrinsic charge characteristic.

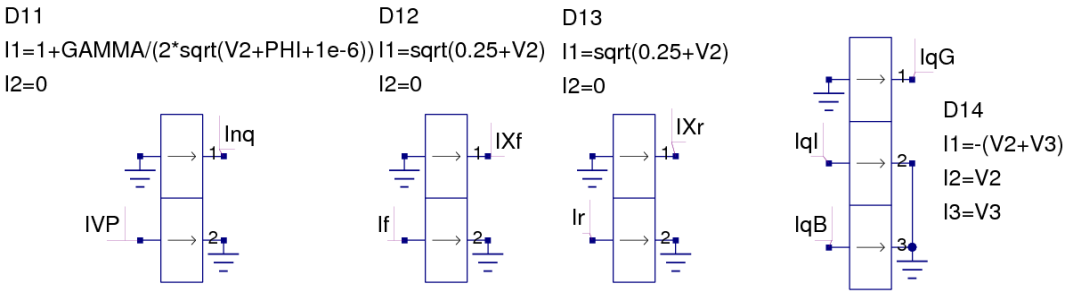

Fig.6.7.4. DC characteristic EDD blocks

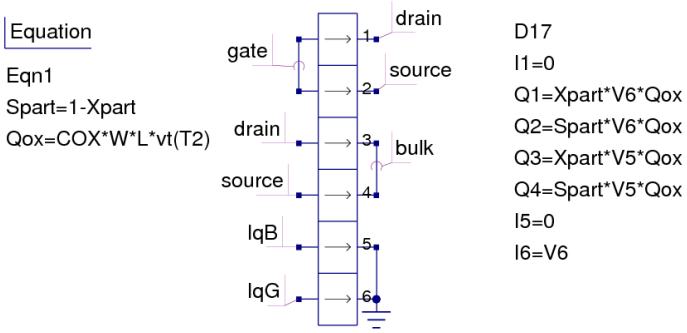

Fig.6.7.5. Combination of EDD blocks from Fig.6.7.1. and Fig.6.7.4. shows the complete EKV v2.6. EDD model

Symbolic representation in QUCS library including some associated parameter variations (remainder take on the default values).

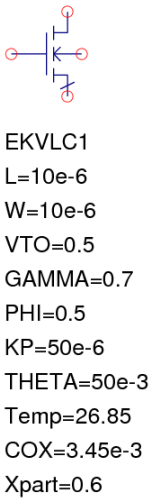

Fig.6.7.6. QUCS equation based schematic representation for EPFL-EKV v2.6 long channel model

Shown in Fig.6.7.6. is the EDD model that is included in QUCS, access can be made to this by dragging nMOS schematic into the workbook and press F9.