Equation Defined Device Modelling of Floating Gate M.O.S.F.E.Ts.

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Abstract

This research work covers the development of a novel compact model for a Floating Gate nMOSFET that will be added to the QUCS library. QUCS (Quite Universal Circuit Simulator) is a GPL simulation software package that was created in 2006 and is continuing to develop and evolve, and there is already a substantial library of components, devices and circuits. Fundamentally, a floating gate device is an analogue device, even though modern technology uses it mainly as a non-volatile memory element there are numerous uses for it as an analogue device.

A study has been carried out with regards to the principles of the physical phenomenon of charge transfer through silicon dioxide to a floating gate. The study has concentrated on the physical properties of the fabricated device and the principles of charge transfer through an oxide layer by Fowler–Nordheim principles. The EKV2.6 MOSFET was used as the fundamental device for the model that has been adapted by the addition of the floating gate. An equivalent circuit of an FGMOSFET was developed and analysed theoretically. This was then formulated into the QUCs environment and created as a compact model. Simulations were carried out and the results analysed to compare with the theoretical expectations and previous research works.

It is well documented that the creation of equivalent circuits for floating gate devices is complicated by the fact that the floating gate is isolated as a node and as such cannot be directly analysed by simulators.

For the equivalent circuit created, circuit analysis was achieved by the introduction of high value resistances connected in parallel with the capacitive

elements that are representative of the incursion of the floating gate that is intrinsic to a floating gate device. The resistance elements were of such value that the time constants were of the order of 10000s and did not interfere with the simulation. The equations from the analysis were formulated and the anticipated responses were shown. The analytical equations developed were then used within the QUCS environment with explicit use of EDDs(Equation Defined Devices) to create a novel model of a FGMOSFET.

Simulations of the model created were carried out with a range of voltage pulses being applied to the tunnelling terminal to affect a charge transfer to the floating gate by means of Fowler-Nordheim principles. The changes of the charge stored on the floating gate were clearly shown by the measured anticipated associated shift in the Threshold voltage.

Simulated results have been compared with previous research and development work and the new model is considered effective. Also because of the ability of the QUCS software to allow the variation of the multiplicity of the parameters associated with the fabrication process, it is considered to be adaptable to a range of modern floating gate device structures and materials.

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AMDG

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Acronyms

ADMS	Automatic Device Model Synthesizer, (Public domain software to translate Verilog-A models into C-models).
CLM	Channel Length Modulation.
CMOS	Complementary Metal-Oxide-Semiconductor.
EDD	Equation Defined Device.
EKVLC1	Enz, Krummenacher, Vittoz, Long Channel Model 1.
EKV2.6 MOSFET	Enz, Krummenacher, Vittoz, Metal-Oxide Semiconductor Field Effect Transistor model version 2.6.
EPFL	Ecole Polytechnique Federale de Lausaune.
FGMOSFET	Floating Gate Metal-Oxide Semiconductor Field Effect Transistor.
GPL	General Public License.
GUI	Graphical User Interface.
IHEI	Impact-Ionised Hot Electron Injection.
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor.
nMOSFET	n-Type Metal-Oxide-Semiconductor Field Effect Transistor.
QUCS	Quite Universal Circuit Simulator.
RC	Resistor Capacitor Time Constant.
SPICE	Simulation Program with Integrated Circuit Emphasis.

Chapter 1.

Introduction

1.1. Objective of the work

The objective was to create a compact model of a floating gate memory device that could be incorporated in the QUCS (Quite Universal Circuit Simulator) library of devices. QUCS is a rapidly developing open source electronic simulator released under GPL (General Public License). The model is to be considered adaptable not only in terms of the degree of programmability but also in terms of developing structures and materials.

This has required: -

(i) Investigation into the principles of operation of floating gate devices.

(ii) Research into the principles of tunnelling and injection through silicon dioxide.

(iii) Creation of a valid model for a floating gate device.

(iv) Circuit analysis of equivalent circuit model.

(v) The use of the QUCS package to create a compact EDD (Equation Defined Device) model of the equivalent circuit adopted.

(vi) The use of QUCS to substantiate the validity of the model using DC and Transient analysis.

1.2. Rationale

Floating gate devices are much used in modern electronic systems, typically as memory devices such as EPROMs, EEPROMs and flash memories, even though they are not inherently digital devices, and as such can be used in many facets where accurate analogue devices are required. This particular project was inspired by the use of weight storage elements for artificial neural networks. For the particular example of neural networks accurate values are required with low tolerances, although this is tempered by the fact that it is relative values that are most important when used on mass. Having stated this it must be mentioned that the uses of floating gate devices are numerous in modern technology.

As with nearly every aspect of modern scientific and commercial development, modelling and simulation is an essential part. In modern day electronics for the high level of complexity that is required, compact device modelling is extremely important. The problems associated with the modelling of a floating gate device are that it has an isolated node due to the floating gate and that the charging and discharging characteristics are extremely non-linear. This causes problems with creation of a valid model.

In 2004 a team of scientists and engineers made the decision to develop QUCS as a free piece of GPL software, which could compete with other commercially available software: http://qucs.sourceforge.net/contact.htm . As a relatively young piece it has gone through many release stages for open source simulation and is still being developed by an expanding group of scientists and engineers throughout the world and is continuing to develop. Since the release of Version 0.0.12 Equation Defined Devices based modelling has been available. This has allowed non-linear physical processes to be modelled. QUCS also allows the

subroutine parameters to be passed as component values to the circuit within a subcircuit. Within the QUCS environment a library of devices has been made available for schematic representation of circuit designs.

Often there are difficulties with the creation of, and problems with, the validity of potential models. A typical example of this is the floating gate device. For the floating gate device the problem is that the floating gate is an isolated node. Once the gate is charged/discharged the characteristics of the associated MOSFET can be measured but calculating and measuring the simulated voltage on the floating gate is extremely difficult. In order to create a floating gate model it is crucial to produce an equivalent circuit that can be analysed theoretically, and to ensure that it can be simulated in the chosen software. Once these requirements had been realised, then the use of QUCS made it possible to create a model of a floating gate device that could then become part of the device library. As part of the library it is anticipated that further design and development could take place in areas where Floating Gate devices are an intrinsic part of the design, and that future technological developments can be relatively easily incorporated in to the model created.

1.3. Original Features

(i) An adaptive floating gate equivalent circuit model was created.

(ii) Circuit analysis was carried out for the equivalent circuit for D.C. and transient conditions.

(iii) The equivalent circuit was built into a compact model in the QUCS software environment using design equations, subcircuit parameters, macromodels and equation defined device techniques.

(iv) The model was tested for validity of performance by creating the model in the QUCS environment, running simulations and comparing results with predicted theoretical performance.

(v) A compact device is now available for the QUCS library.

1.4. Relationship to previously published work

In respect of representing a floating gate device in the QUCS environment there are no previously published works outside the QUCS development team, however in order to create the compact model, reference can be made to a large number of previously published works[1 – 13]. Detailed studies have been carried out on the development of MOSFET compact models (chapter 2), structures of FGMOSFETs (chapter 3), charge transfer through insulating oxide and oxide /nitride/oxide layers (chapter 3), equivalent circuits and analysis of Floating Gate devices (chapter 4), and the extremely important development carried out in the QUCS simulation package (chapter 5).

Within the QUCS environment the Verilog-A implementation of the EKV v 2.6 MOSFET is to be used as the foundation of the floating gate device. The n-type enhancement mode transistor will be considered, as this will allow the modelling of a floating gate device by means of Fowler-Nordheim tunnelling for both charging and discharging of the floating gate. It is anticipated that once the model has been substantiated the principle can be extended to the p-type enhancement device

where Impact-Ionised Hot Electron Injection (IHEI) can be used for floating gate discharge.

The principles of charging and discharging a floating gate are based on Fowler-Nordheim Tunnelling [14,] and (IHEI) [16,16,17], such as EEPROMs. Although, these techniques for charging and discharging are reasonably well documented they have mainly been applied to specific structures [14, 17]. However the characterisation of FGMOSFETs are heavily dependent on fabrication processes and device geometry [18]. W.N.Gao et al [19] has suggested along with others that the corners introduced through lithography can enhance the electric field in oxide layer and hence increase charge transfer. Other effects have been reported such as the erase operation being complicated by the formation of a deletion layer in the channel and under the tunnel oxide [20].

Many of the suggestions made for models are highly empirical such as K.Rahhimi et al [21] who proposed an empirical expression for the IHEI process that uses only drain, gate and source potentials as parameters. In general, these sorts of parameter tolerances, and material and structural variations can be incorporated in the general Fowler-Nordheim and IHEI equations.

1.5. Methodology.

The floating gate device to be modelled was based upon the EKV v2.6 long channel MOSFET model that already sits in the QUCS library, as this is the preferred geometric structure for ease of access to the tunnel terminal. This was adapted by the addition of a floating gate, and may be assumed a polysilicon material or silicon nitride, for modelling purposes. The model of the EKv2.6 MOSFET [10,22] was then modified to take into account the intrusion of the gate electrode. This consisted of the coupling capacitive effects of the floating gate with the control gate, drain,

source, substrate, and tunnelling electrode. In order to analyse such a structure it was decided to place high value resistances in parallel with the associated capacitors so that the time constants were irrelevant to the simulation duration.

From the detailed consideration of the physical structure of floating gate devices the equivalent circuit was created. This was then theoretically analysed for the D.C. and Transient responses. From this analysis equations were formulated showing the charging of the floating gate.

The characterization of FGMOSFETs was based on the QUCS software. QUCS is a rapidly developing open source electronic circuit simulator released under GPL. It allows graphical user interface and circuit simulation. It has a developing library of circuits and devices and it is intended to add to this library with a FGMOSFET model.

The flow chart shown in Fig.1.1. shows the useful nature of the QUCS software and how it is fully integrated from design through to the simulation for an analogue/digital component or circuit. Simulators invariably have common overall structures where circuits are represented by textual netlists, or schematic diagrams. This allows the simulator to have access to the defined structure of the circuit and carry out the desired analysis. The other element required is a simulation engine that enables the analysis calculations to be carried out. In this case it was a D.C. and Transient analysis. The final element for the simulator is a post processor that allows data to be presented in both tabular and graphical forms. Simulators rely on mathematical models of components, devices (linear and non-linear), ICs, subcircuits and nested circuits. Without models the design of complicated electronic systems would not be possible.

Fig.1.1. shows the various modelling routes that are available within QUCS. The route taken for this research was to construct a model from standard circuit components that were available. By the time this work was undertaken QUCS version 0.0.16 had been released and was used for simulation. This allowed the use of EDDs and allowed device current to be formulated as a function of voltage, and also device charge to be formulated as functions of voltage and current (chapter 5). The EDD modelling technique is an interactive process, which acts as a precursor to the component modelling procedures based on the Verilog-A description language [2, 3].

The essential purpose of the proposed work was to develop a model of a FGMOSFET so that it can reside in the QUCS library, and can be developed and re-modelled relatively easily as research and manufacturing techniques evolve. Without component modelling the science of circuit simulation would not have developed to today's present stage, and would not be able to develop in the future.

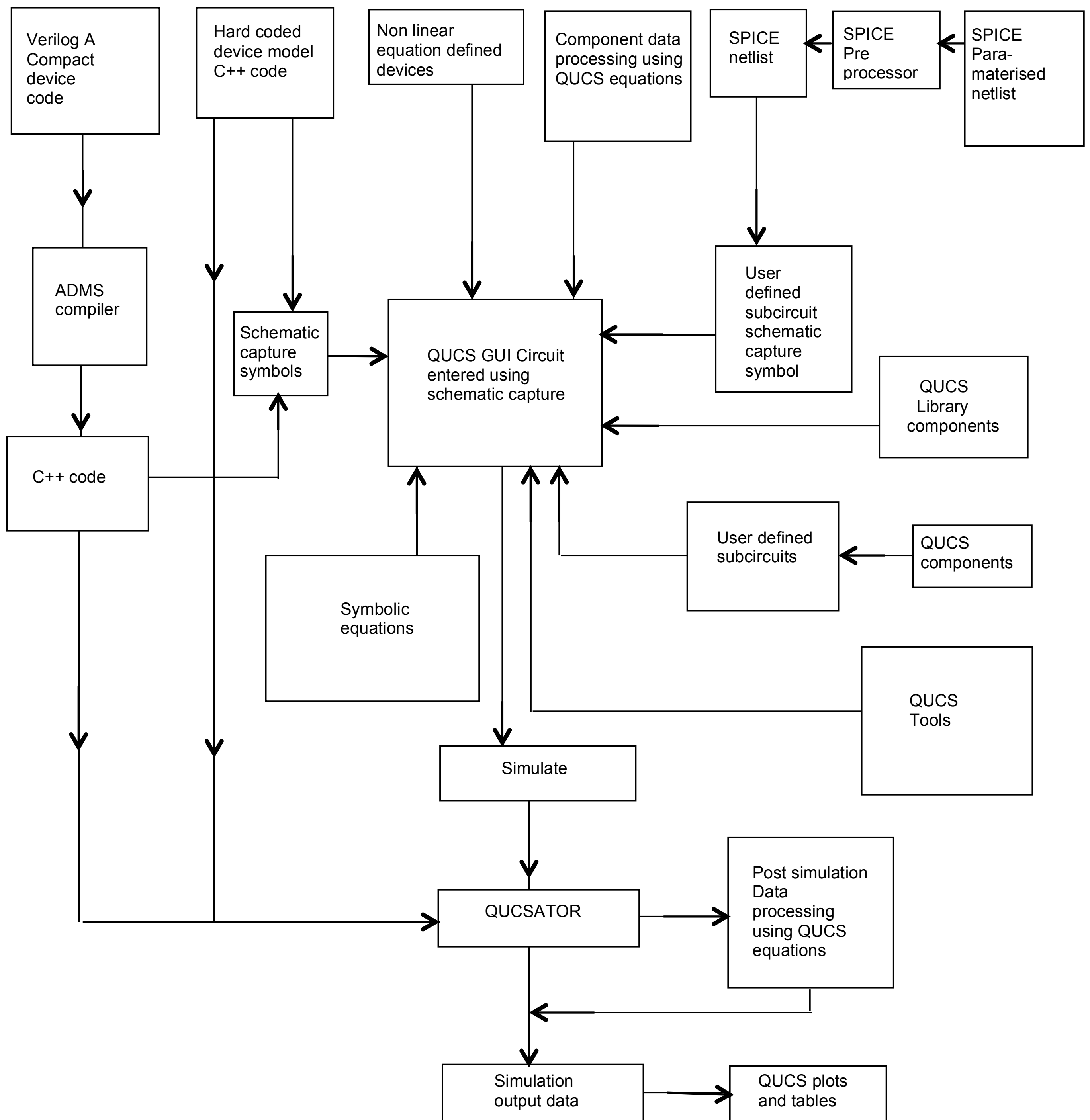


Fig.1.1. Overall architectural structure for the implementation of QUCS [4]

1.6. Structure of Thesis

Chapter 1 sets out the objectives of the work, the reasons it is considered a research area and the approach that has been taken to creating an original solution. The chosen simulation software was QUCS and has been used to create an adaptable compact model. For the work it was necessary to study, investigate and develop the topics simultaneously, however, individual chapters have been dedicated to major sections of the work.

Chapter 2 investigates the fundamental building block required for a floating gate device, that is, the n-type enhancement MOSFET. The model for this device is decided upon and the equivalent circuit is presented.

Chapter 3 deals with the operation of floating gate devices with specific emphasis on structures, movement of charge and the development of the total model.

Chapter 4 carries out the theoretical analysis of the created model of the floating gate device. This gives the indicative responses of the model that are anticipated when simulations are carried out in the QUCS environment.

In Chapter 5, these anticipated responses draw comparison from, well documented, previous practical quantitative works.

Chapter 6 is dedicated to the details of the chosen QUCS software. Important sections of this chapter are on Equation Defined Devices and the use of EDDs for implementing the EKVv2.6 Long Channel MOSFET.

Chapter 7 considers the simulation process that took place in order to draw comparison between the theoretical analysis and the simulated model.

Chapter 8 examines a substantial amount of simulation data, presenting the data both numerically and graphically. These data are then critically assessed by

drawing comparison between the theoretical analysis and simulation responses, in respect of the characteristics of floating gate devices.

Finally, Chapter 9 summarises the achievements of the work and recommendations for future work, development and research.

Chapter 2.

Basic principle of n-type enhancement M.O.S.F.E.Ts

2.1. Operation of n-type enhancement MOSFETs

Basic Structure

The principle of operation of an mos device has not changed since the initial inception. This is the modulation of a conductive path between two terminals by a third terminal. Fig.2.1. shows the basic structure used in such a device.

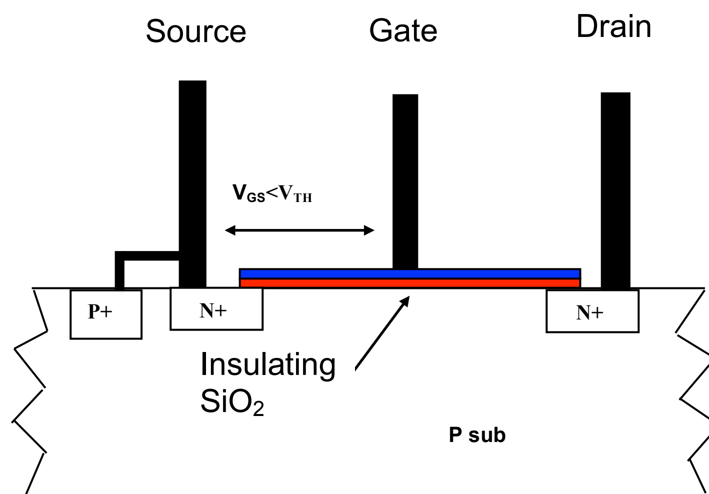


Fig.2.1.1.a. M.O.S. Sub threshold

The n-type enhancement MOSFET shown in Fig.2.1.1a. is a simple representation which can indicate the basic principles of operation but whose physics has become increasingly more complicated with advancing technology and circuit implementation demands.

The source and drain consist of two heavily doped n-type regions, a gate which is usually made of heavily doped polysilicon, while the bulk substrate is p-type, which is usually lightly doped.

Inversion Layer

For the purposes of this description it is assumed that the substrate is the same potential as the source.

If the voltage, on the gate, $V_{GS,}$ is gradually increased, holes will be increasingly be repelled from the substrate interface surface. If the gate voltage is further increased

then the surface becomes depleted of holes until the holes become the minority charge carries and electrons become the majority, forming a conduction channel between the source and the drain. This conduction channel is known as an "inversion layer" and the voltage at which it occurs is the "threshold voltage, V_{TH}".

If there is no potential difference between the drain and the source then the charge density is uniform along the channel as shown in Fig.2.1.1.b.

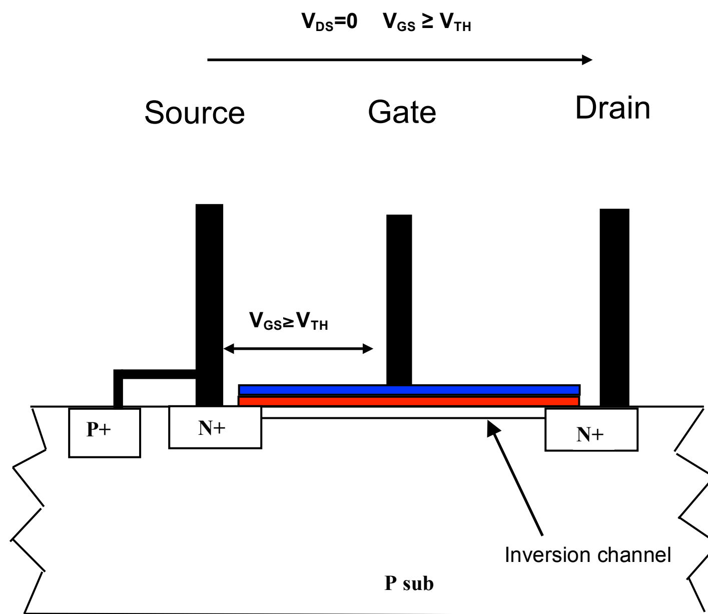


Fig.2.1.1.b. M.O.S. with uniformly charged inversion layer

If the device drain is made positive with respect to the source, $V_{DS,}$ then the voltage will increase from 0V at the source to V_D at the drain. The result of this is that the effective voltage available along the channel is gradually reduced from source to drain. The effective voltage at the source end of the channel being $V_G - V_S = V_{GS}$ and at the drain being $V_G - V_D = V_{GD}$. That is, the net value of voltage available to induce an inversion layer gradually reduces from source to drain, and therefore so does the channel charge carrier density [13,14].

The charge density can be defined as:

$$Q_n(y) = -C_{ox}\{[V_{GS} - V_{(y)}] - V_{TH}\} \quad \dots\dots\dots\dots \quad (2.1.)$$

the minus sign indicating that the charge is made up of electrons for an nMOS

where $Q_n(y)$ = the charge density at position y

$C_{ox} = \varepsilon_{ox}/t_{ox}$ where C_{ox} is the oxide capacitance per unit area

ε_{ox} is the oxide permeability

and t_{ox} is the oxide thickness

And $V_{(y)}$ = the channel potential at position y

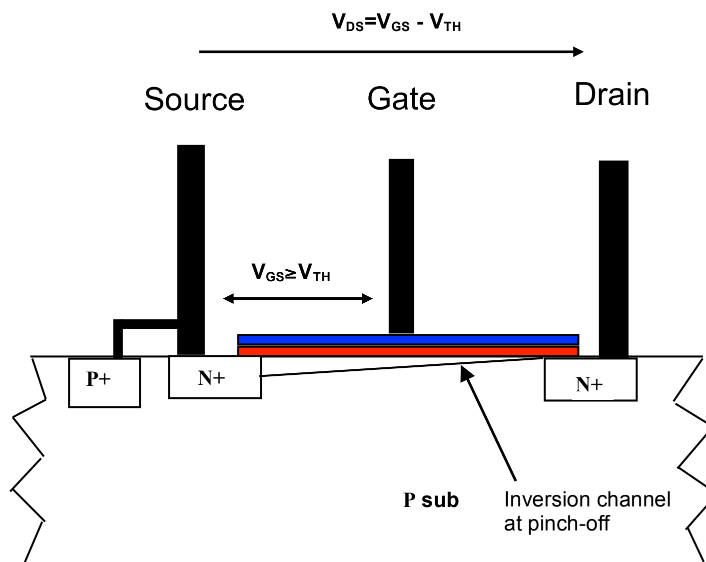


Fig.2.1.1.c. M.O.S. Saturation region at Pinch-off

Linear Region

The Linear region of operation is defined as where V_{GS} is sufficient to maintain an inversion channel between source and drain, this value will be dependent on V_{DS}. The point at which the inversion layer is reduced to zero at the drain is known as the "pinch off". From eq.2.1 it can seen that this happens when:

$$\left[V_{GS} - V_{(y)}\right] - V_{TH} = 0 \quad \dots\dots\dots\dots \quad (2.2.)$$

For the linear region the drain current:

$$I_D = -WQ_n(y).\upsilon(y) \quad \dots\dots\dots \quad (2.3.)$$

where, W is the width of the device.

Assuming a long channel device, the velocity of the charge carriers, $\upsilon(y)$, is the product of the mobility, μ_n, and electric field, E. This gives:

$$I_D = -WQ_n(y).\mu_n.E \quad \dots\dots\dots \quad (2.4.)$$

This can be modified for short channel devices,

Substituting eq.2.1. in to eq.2.4. we have:

$$I_D = -W.C_{ox}\{[V_{GS} - V_{(y)}] - V_{TH}\}.\mu_n.E \quad \dots\dots\dots \; (2.5.)$$

assuming a long channel device with low electric field, we have:

$E = -\frac{dV}{dy} \dots\dots\dots \; (2.6.)$

and therefore:

$$I_D = W.C_{ox}\{[V_{GS} - V_{(y)}] - V_{TH}\}.\mu_n.\frac{dV}{dy} \quad \dots\dots\dots \; (2.7.)$$

re-arranging eq.2.7. we get:

$$I_D.\,dy = W.C_{ox}\{[V_{GS} - V_{(y)}] - V_{TH}\}.\mu_n.dV \quad \dots\dots\dots \; (2.8.)$$

In order to obtain the drain current, eq.2.8. can be integrated along the length, L, of the channel:

$$\int_0^L I_D\,.dy = \int_0^{V_{DS}} W\,.C_{ox}.\mu_n\{[V_{GS} - V_{(y)}] - V_{TH}\}.dV \quad \dots\dots\dots \; (2.9.)$$

Integrating eq.2.9. we have:

$$I_D = \frac{W}{L}.C_{ox}.\mu_n\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] \quad \dots\dots\dots \; (2.10.)$$

As can be seen from eq.2.10. the drain current will be nearly linear for small values of V_{DS}.

Saturation Region

When V_{DS} reaches a high enough value the channel becomes pinched off and starts to shorten. This is the point when the characteristic enters the Saturation Region. The value of I_D when this happens can be calculated from eq.2.10. This occurs when the value of $V_{DS} = V_{DSat}$ which mean:

$$V_{GS} - V_{TH} \equiv V_{sat} \quad \dots\dots\dots \; (2.11.)$$

substituting eq.2.11. into eq.2.10. we have:

$$I_D = \frac{W}{L}.C_{ox}.\mu_n\left[(V_{GS} - V_{TH})V_{DSat} - \frac{V_{DSat}^2}{2}\right] \quad \dots\dots\dots \; (2.12.)$$

giving:

$$I_D = \frac{W}{2L}.C_{ox}.\mu_n\,(V_{GS} - V_{TH})^2 \quad \dots\dots\dots \; (2.13.)$$

This approximates to a square law dependency on V_{GS} and almost independent of V_{DS} however in practice this is not the case.

The primary reason for a nonzero conductance is channel length modulation (CLM). This is because the drain forms a depletion region with the surrounding substrate that is dependent on the drain voltage, as indicated in Fig.2.1.1.d. and as such causes the effective channel length to shorten.

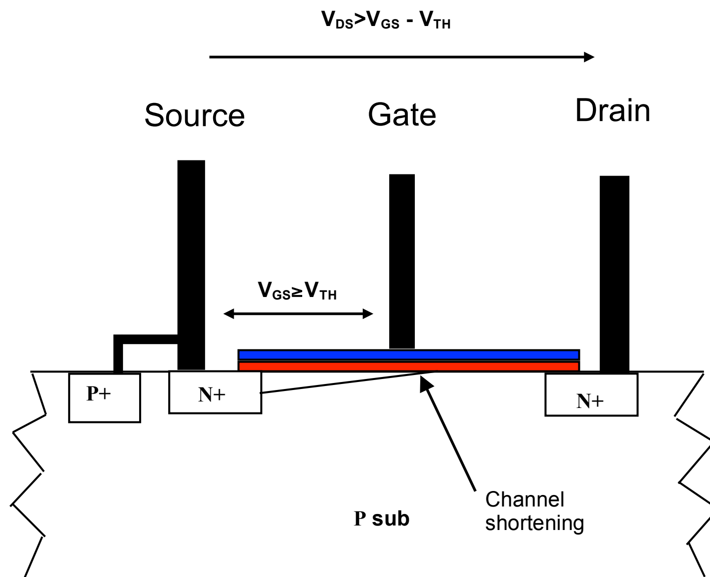


Fig.2.1.1.d. M.O.S. Saturation Mode

This results in the drain current increasing and to take account of this effect the drain current equations are modified both in the linear and saturation region by the following:

$$i_D = (1 + \lambda . V_{DS}). i_{D0} \quad \dots\dots\dots \quad (2.14.)$$

where, i_{D0} is the value of i_D when CLM is ignored

and λ is an empirical value (units 1/V).

The characteristic relationship between the current flowing between the drain and the source, Ids, and the voltage between the drain and the source, V_{DS}, for varying values of the voltage on the control terminal, V_{GS}, can be obtained analytically, by measurement or by simulation. Shown in Fig.2.1.2. is a circuit used for such measurements and the relationship is plotted.

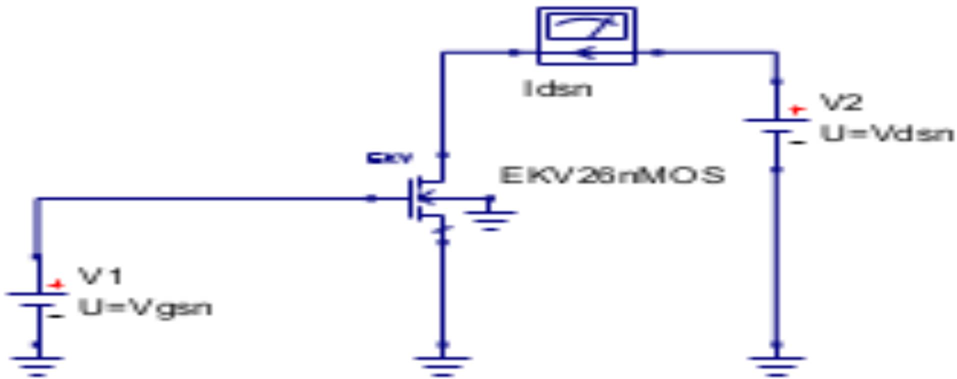


Fig.2.1.2.a Circuit for Vds v Ids (measurement or simulation)

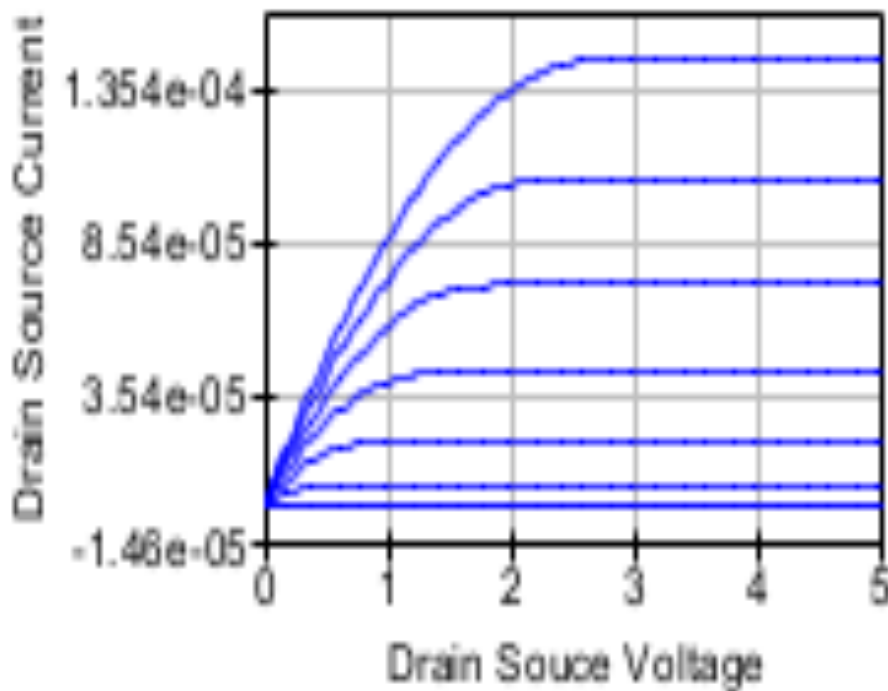


Fig.2.1.2.b. Resultant characteristic curves for different Vgs

So far this section has given a brief outline of the D.C. operation of an nMOS device. With the addition of a floating gate (ref. chapter 3.) within the oxide layer,

charge can placed upon the floating gate and as such can modify the characteristics of the device.

As the model to be designed needs to take into account the accumulation of charges on the floating gate, the process of charge accumulation needs to taken into account, and the model created needs to able to be analysed with respect to the floating gate which is an isolated node. For the model created the D.C. and transient analyses will be taken into account and is of pre-eminent importance in this work.

Due to the construction of the device there will be elements that perform the fundamental operation of the device and others that are parasitic and detract from the operation of the device. Essential to an nMOS device is the capacitance between the gate and the channel, others that can be detrimental to performance include:-

- The capacitance associated with the reverse biased junctions between the drain and the source with the substrate.
- The overlap capacitors associated with the gate overlapping with the source and drain.
- The capacitance between the channel and the substrate and the way in which the charge is partitioned.

A typical table for calculating approximate associated value for capacitance of capacitors is shown for the different operating conditions in Table 2.1.1

Table 2.1.1. Approximate MOS terminal capacitance that could be used in First order model: OV=overlap: j=junction.

	OFF	Linear Region	Saturation
C_{GS}	C_{OV}	$C_{GC}/2 + C_{OV}$	$2C_{GC}/3 + C_{OV}$
C_{GD}	C_{OV}	$C_{GC}/2 + C_{OV}$	C_{OV}
C_{GB}	$C_{GC}\ C_{CB}/(C_{GC} + C_{CB})$ $< C_{GB} < C_{GC}$	0	0
C_{SB}	C_{jSB}	$C_{jSB} + C_{CB}/2$	$C_{jSB} + 2C_{CB}/3$
C_{DB}	C_{jDB}	$C_{jDB} + C_{CB}/2$	C_{jDB}

Where:- C_{GS} = gate-source capacitance

C_{GD} = gate-drain capacitance

C_{GB} = gate-substrate capacitance

C_{DB} = drain-substrate capacitance

Short Channel Devices

As I.C. technology has developed there has been a continuous drive for a higher level of integration and as such deice geometries have shrunk. This has meant that even with the use of moderately low voltages, high field effects have to be considered. The primary high field effect is that of velocity saturation. Scattering due to high energy photons eventually causes the carrier velocity to stop increasing with an increasing field. In silicon, as the electric field approaches about 10^6 V.m^{-1}, the electron drift velocity displays less dependence on electric field strength and tends to level off at 10^5 m.s^{-1}.

Previously for long channel devices, the saturation current was assumed to correspond to the drain current at pinch off. In short channel devices the current saturates when the drift velocity stops increasing.

The original long channel saturation current was eq.(2.13.)

$$I_D = \frac{W}{2L}.C_{ox}.\mu_n\,(V_{GS} - V_{TH})^2 \ldots\ldots\ldots \quad (2.13.)$$

this can be re-written as:

$$I_D = \frac{W}{2L}.C_{ox}.\mu_n\,(V_{GS} - V_{TH}).V_{Dsatl} \quad \ldots\ldots\ldots\ (2.15.)$$

where, V_{Dsatl} indicates the long channel value and is $(V_{GS} - V_{TH})$

For a short channel device the drain current may be approximated to:

$$I_D = \frac{W}{2L}.C_{ox}.\mu_n\,(V_{GS} - V_{TH}).[\,(V_{GS} - V_{TH})\,||(L\,E_{sat})]\ \ldots\ldots\ldots\ (2.16.)$$

where E_{sat} the field strength where the carrier velocity has dropped to half the value at low field. The important ratio in eq.2.16. is $\frac{(V_{GS}-V_{TH})}{L}$ to E_{sat}. If this ratio is small then the device will behave like a long channel device. A typical value for E is ≈ 4 x 10^6 $V.m^{-1}$, but it is process dependent. When the ratio $\frac{(V_{GS}-V_{TH})}{L}$ to E_{sat} becomes large, the relationship between drain current and gate-source voltage becomes more linear rather than the previous square-law.

Models have evolved and have been modified and improved as technology has improved both with understanding of the physics of devices and with the ability of the fabrication process to make the devices, often in a symbiotic manner. The EPFL-EKV models were developed and introduced between 1997 and 1999 and since that time they have been widely used in industry and academic development.

2.2. EPFL-EKV2.6 MOS Transistor Model.

Invariably modern circuit design is carried out using circuit simulators and as such the software has to be capable of modelling the various circuit elements that are an integral part of that design. Whilst it is impossible to model any physical system with one hundred per cent accuracy, in order to take in to account all eventualities,

models can be developed and evolved to be more accurate and take into account new technological developments.

With this in mind, and taking into account the general structure of a floating gate transistor, the EPFL - EKV2.6 MOSFET model, within the QUCS environment, was selected to be incorporated in the floating gate model [10]. Whist still being updated, it has shown itself to be reliable even though it is still to be fully optimized. The EKV model takes into account the fundamental physical properties of the MOS structures and processing steps. It is compact and scalable and therefore is adaptable, but fundamentally used for low voltage, low current analogue and mixed mode systems using sub micron technologies [Appendix 1].

The effects modelled include:-

- Basic geometrical and process aspects such as oxide thickness, junction depth, effective channel length and width.
- Effective doping profiles and substrate doping.
- Modelling of weak, moderate and strong inversion.
- Mobility effects due to vertical, lateral and velocity saturation.
- Short channel effects such as channel-length modulation, source and drain charge-sharing and reverse short channel effects.
- Modelling of substrate current due to impact ionisation
- Effect of impact ionization on substrate current.
- Quasi-static charge based dynamic model
- A first order non-quasistatic model for transconductance
- Short distance geometry and bias dependent device matching.

In threshold based models, expressions can be obtained for the drain current operating in the weak, moderate and strong inversion regions assuming the dominant transport mechanism being drift or diffusion [13]. This assumes an abrupt transition when $V_{GS} = V_{TH}$. Physically there is a region where neither mechanism dominates, and this is the weak inversion region. For low voltage, low power and analogue design this region becomes important and the modelling of this region is complex. In the EKV model the problem is overcome by interpolation so that there is a gradual transition for the drain current and the derivative between the two regions [1,10,12]. The EKV model is a charge based compact interpolation model.

The fundamental Long Channel and Short Channel parameters and equations are given in Appendices 2 and 4. However the Long Channel device has been chosen as dimensionally appropriate for the modelling of a floating gate device.

2.3. Model Equivalent Circuit for EKV MOSFET

The equivalent circuit adopted for the original EKV model is shown in Fig.2.3.1 and specific component parameter values are calculated from the design equations used by the simulation equations shown in Appendix 2. Initially the design specification will have been set out and adopted by the design engineers who will have a comprehensive knowledge of the fabrication processes and limitations. The model is a scalable and compact simulation model that has been built on the fundamental physics of the MOS structure. It was created to be used to assist the design of low voltage, low current analogue and mixed analogue-digital circuits using submicron CMOS. Parameters could be extracted from simulation equations and inserted in to the model and from this circuit designs could be simulated in order to accelerate the design process.

From Fig.2.3.1. it can be seen that the extrinsic part of the device is separated from the intrinsic part as it is often common to a range of MOS devices. This extrinsic part includes resistances associated with the source and drain diffusions, also include are the junction currents and capacitances. Descriptions of the symbols in the EKV model are shown in Table.2.3.1.

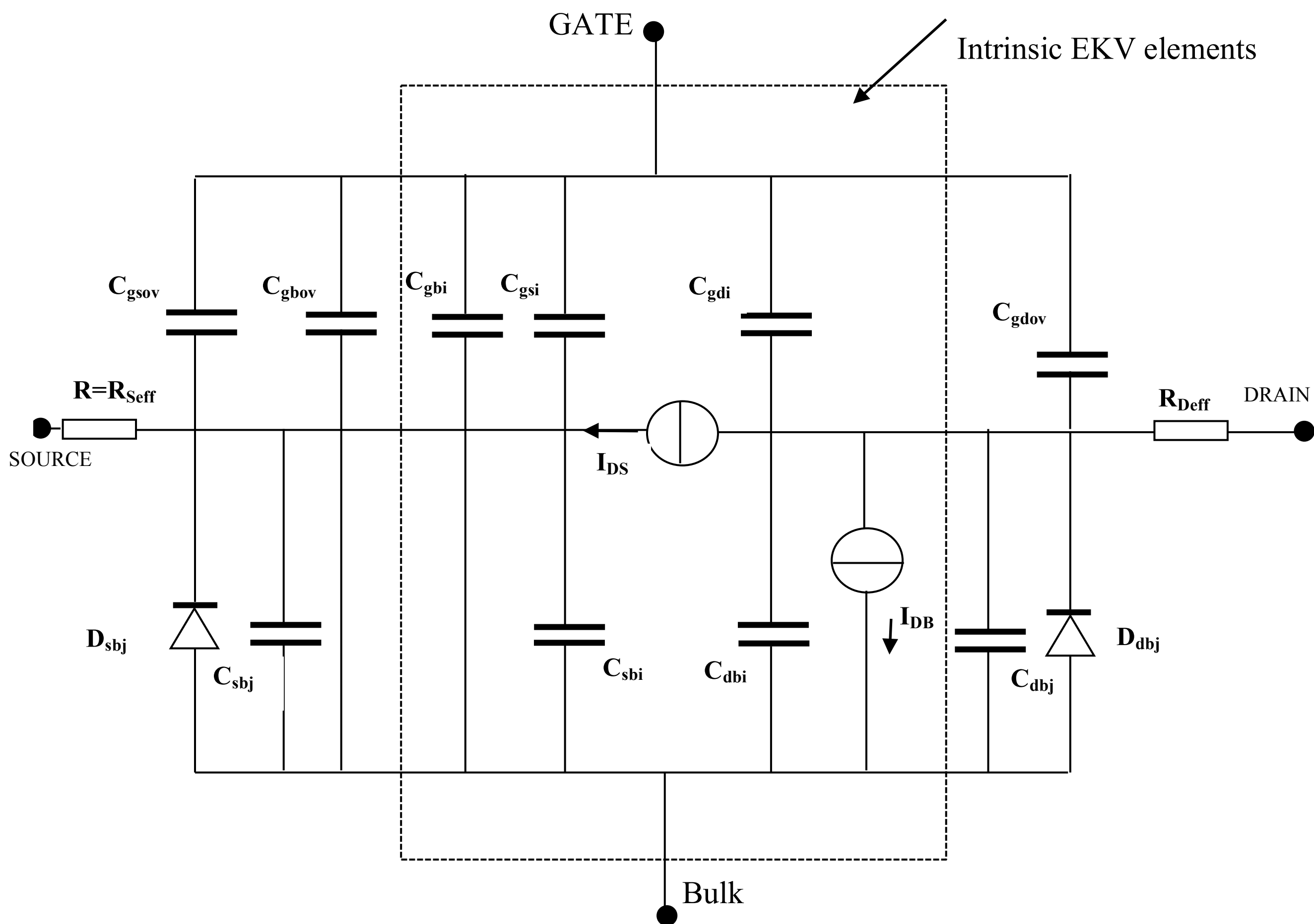


Fig.2.3.1. Initial equivalent circuit for EKV model [10]

Table 2.3.1.EKV original equivalent circuit model

Name	Description
C_{gsov}	Gate –source overlap capacitance
C_{gbov}	Gate-base overlap capacitance
C_{gbi}	Intrinsic gate-substrate capacitance
C_{gsi}	Intrinsic gate-source capacitance
C_{gdi}	Intrinsic gate-drain capacitance
C_{gdov}	Gate-drain overlap capacitance
C_{sbj}	Source-substrate junction capacitance
C_{sbi}	Intrinsic source-substrate capacitance
C_{dbi}	Intrinsic drain-substrate capacitance
C_{dbj}	Drain-substrate junction capacitance
I_{DS}	Drain-source current
I_{DB}	Drain-substrate current
R_{Seff}	Source series resistance
R_{Deff}	Drain series resistance
D_{sbj}	Source-substrate junction diode
D_{dbj}	Drain-substrate junction diode

2.4. Chapter Summary

Chapter 2 has dealt with the basic building element for the floating gate device, this is the n-type enhancement MOSFET. The details of the structure for the device defining it's electronic behaviour have been presented. Classic characteristic equations have been shown, and the sub-threshold, linear and saturation regions have been described. A QUCS simulation shows the characteristic plot for V_{DS} ~ I_{DS}

for various values of V_{GS}. These graphs are to be referenced in order to confirm that the designed floating gate model is operating correctly according to the charge stored on the floating gate.

Although the long channel device is the main MOSFET to be considered for modelling a floating gate device, the short channel device was also described, this will allow for any future developments involving short channel devices.

Naturally, for simulation purposes, it is necessary for the transistor model created to be capable of being analysed. For these purposes the physical operation of the transistor has been outlined. The transistor model to be used, the EKVv2.6 was selected as this was already in the QUCS library, it is modelled in detail and is adaptable to manufacturers parameter variations and future development. Representation of the EKV v2.6 model is shown and the Appendix reference is given, showing in details the intrinsic parameters.

Chapter 3

Principles of operation of floating gate devices

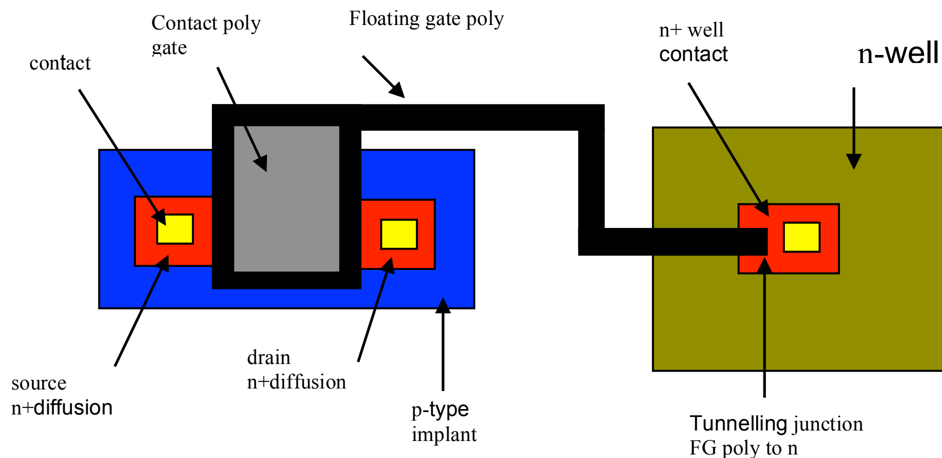
3.1. Floating Gates

Floating gate devices use the principle of storing charge on an electrically isolated material, either polysilicon or other charge storage material. Once the charge has been placed on the floating gate it will remain there and thus can be used to store data [23]. Although there is inevitably a gradual leakage the discharge rate is designed to be so small that the device can be considered to be non-volatile.

The structure is basically a modified nMOSFET which has an extra layer, typically polysilicon or more usually silicon nitride with modern devices, deposited within the oxide layer so that there is no direct electrical contact to any of the device terminals i.e. there is only capacitive coupling. This general structure is common to all FG devices but geometries, dimensions, materials, and fabrication techniques are continuing to develop for increased densities, speed of operation and applied applications [24,25,26,27,28, 29]. As an example of this is the replacement of the floating gate material. Theoretically because the FG is isolated the charge should be stored permanently, however because of demands to speed up programming times and lowering of charging voltage, the oxide layer through which Fowler-Nordheim charging takes place has be reduced to << 100Å. The polysilicon within the oxide layer is effectively an isolated conductor and hence charges can freely move. Any oxide defects will allow these charges to leak away. Typically polysilicon has been replaced by a silicon nitride, Si_3N_4, layer that is an insulator and any charges injected onto the nitride are effectively trapped [8, 30, 31,32].

A typical device is shown in Fig.3.1.1.

(a)



(b)

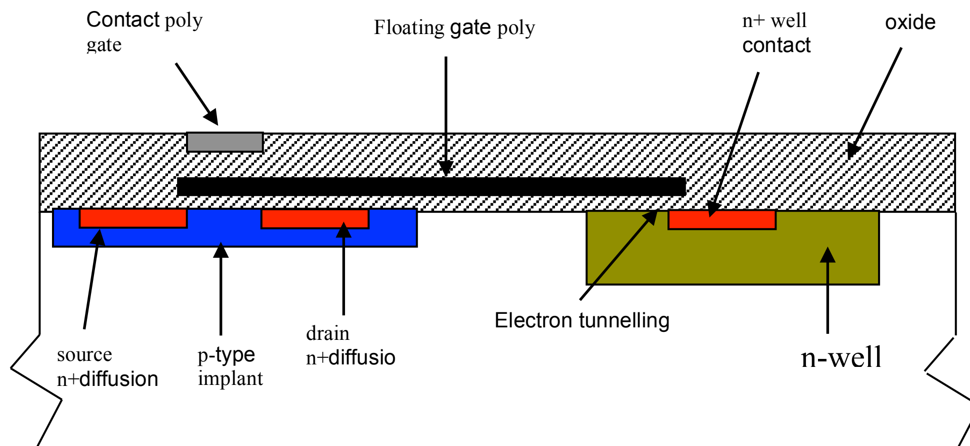


Fig.3.1.1. Floating Gate nMOSFET (a) plan view (b) sectional view

In order to develop equations that describe the operation of the FGMOS, the basic operation of the MOS can be used to model the FGMOS. When charge is stored on the floating gate the characteristic of the MOS device is modified, and as such when this characteristic is monitored, it can indicate stored information, both digital and less accurately analogue. For this work the charging of the device to be considered utilises the well documented Fowler-Nordheim principle [14].

Present day devices only require a small number of electrons to be moved for charging, of the order 10^3-10^5, which can change the voltage by as much as 0.32V for a 1fF capacitor. The specific control of the charge movement is difficult to control and even more difficult to predict due to the physical parameters already stated. Digitally this is easier to handle than for analogue devices, however analogue devices that utilise relative voltage levels are suitable.

An adaptable compact model for a FG device will be highly advantageous for researchers and development engineers. Previous attempts to model the FG device have relied on pseudo floating node often connected to voltage generators that predict the floating gate voltage [8,29,32,33,34,35,36]. The QUCS software package overcomes this problem with the introduction of Equation Defined Devices (ref. chapter 6), and allows adaptability to new technological advances.

Developing model equations for a FGMOS device and enabling the model to be simulated creates a problem because of the nature of the floating node.

The contact poly control gate couples capacitively with the floating gate and therefore modulates the channel current. If there is charge on the floating gate this will further modulate the channel current.

The essential requirement is for the FGMOS is to transfer charge through the oxide on to the floating gate. The charging and discharging are based on the classical principles of Fowler-Nordheim Tunnelling [14] and Impact–Ionised Hot Electron Injection(IHEI) also known as Channel Hot Electron Injection[15,16,17]. Although these techniques for charging and discharging are well documented they have only been applied to specific structures [18]. However the characterization of FGMOSFETs is also heavily dependent on the fabrication process and geometries [30].

3.2. Charging and Discharging of a Floating Gate

In order to transfer charge to the floating gate it is necessary move the electrons through the oxide.

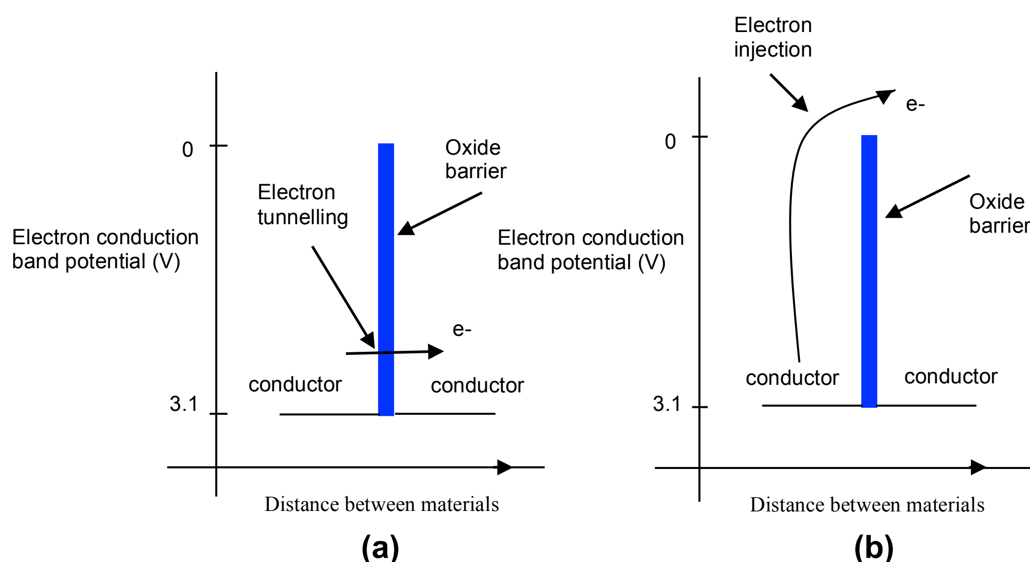


Fig.3.2.1. (a) Electron tunnelling through band potential
(b) Electron injection over band potential

Electron tunnelling is a quantum mechanical process and is the main mechanism for consideration for the modelling of a floating gate device. The equations to be used have been well defined by Fowler-Nordheim and relate to the electric field that is applied across the oxide.

For the floating gate device the structure for consideration consists of the polysilicon gate – gate oxide – heavily doped region of silicon. Electrons are tunnelled from the FG to the doped region. The potential difference lowers the oxide barrier and electrons enter the oxide conduction band, and are then swept across the oxide and into the doped silicon by the high oxide field. Empirically equations have been found

for the gate current during tunnelling with varying degrees of accuracy. A general formulation is shown in equation (3.2.1.)[8] .

$$\boldsymbol{I_g} = \boldsymbol{I_{to}}.\boldsymbol{e}^{-\frac{V_f}{V_{ox}}} \quad \ldots \ldots \quad (3.2.1)$$

where, I_g = gate current equating to tunnel current for this work, I_{Tun}

V_{ox} = oxide voltage, i.e. (tunnelling voltage – floating gate voltage).

V_f = constant dependent on oxide thickness,

for modern technology ≈ 368.04(V)

I_{to} = pre-exponential tunnel current per unit area

This is the initial equation used for analysis and simulation [4].

Accurate characterisation of a FG device has historically proved difficult due to the isolated FG. It was therefore necessary to create a model to take into account this isolation and to calculate the charge stored on the FG when a tunnelling voltage is applied. With the model introduced in this work an EKV nMOSFET long channel device has been adapted and used. The model is adaptable and parameters can adjust to other transistor models. Also it has the ability for parameters to be adapted for evolving devices operating on the same principles. As such it is thought that a degree of rigour has been obtained.

3.3. Floating Gate model Analysis

Tunnelling Current

If Fowler-Nordheim tunnelling [154 is assumed to change the charge on the floating gate, the tunnelling current that flows will depend on voltage across the oxide and the oxide thickness. There may also be other effects such as capacitor coupling and device geometries.

$$I_{Tun} = A.exp\left[\frac{B}{(V_{Tun} - V_{fg})}\right] \quad \text{if } V_{Tun} > V_{fg} \quad \text{else } 0 \quad \ldots\ldots \quad (3.3.1)$$

Where "A" = I_{to} and "B" = V_f are constants referred to in eq.(3.2.1)

The simulation carried out was to set the value of "W" the pulse width and V_{Tun} the pulse magnitude and so inject charge on to the floating gate. This is the same as extracting electrons from the floating gate by tunnelling. The simulation would be carried out at the subthreshold level and post threshold level. Tunnel voltage pulses would be applied of 50μs width and changes in floating gate monitored and the effects on the device characteristics evaluated

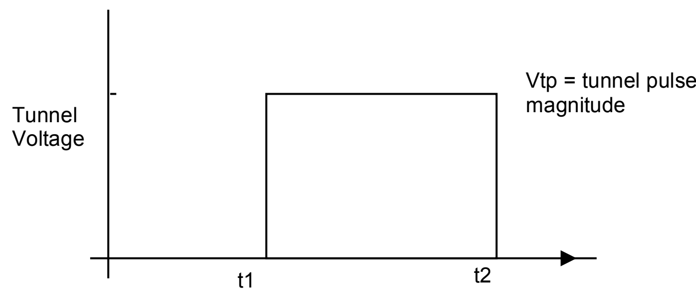


Fig.3.3.1 Applied Tunnel Pulse

For the pulse shown in Fi.3.3.1 the tunnel current will be:-

$$I_{Tun} = A.exp\left[\frac{B}{V_{tp} - V_{fg}}\right] \quad \text{for } \ t_1 \leq \ \text{time} \ \leq \ t_2 \quad \ldots\ldots \quad (3.3.2)$$

$$\text{Also we have:-} \quad I_{Tun} = \frac{dQ_{fg}}{dt}$$

$$\text{and} \therefore \quad Q_{fg} = \int_{t_1}^{t_2} A.exp.\left[\frac{B}{(V_{tp} - V_{fg})}\right].dt \quad \ldots\ldots \quad (3.3.3)$$

For initial approximation it was assumed that V_{tp} (8 – 12V) >> V_{fg} (0.1 – 1.0V) and that V_{fg} is only a weak function of time and therefore:-

$$Q_{fg} \approx A.exp.\left[\frac{B}{(V_{tp} - V_{fg})}\right].(t_2 - t_1) \quad \dots\dots \quad (3.3.4)$$

Total accumulated charge can then be calculated for small increments of time and evaluating V_{fg} after each pulse.

“A” and “B” are Fowler-Nordheim coefficients and are highly dependent on the thickness of the oxide and the Si/SiO_2 barrier, for 40Å oxide these are taken from C. Diorio et al.[29], and are :- A = 9.35 x 10^8 (A) and B = -368.04 (V^{-1})

In order to check the value of “B” we can replace $A(t_2 - t_1)$ by “D” giving:-

$$Q_{fg} \approx D.exp\left[\frac{B}{V_{tp} - V_{fg}}\right] \quad \dots\dots \quad (3.3.5)$$

$$\text{or} \quad ln(Q_{fg}) \approx ln(D) + \frac{B}{(V_{tp} - V_{fg})} \quad \dots\dots \quad (3.3.6)$$

From plotting $ln(Q_{fg})$ against $\frac{1}{(V_{tp} - V_{fg})}$, "B" equals the slope.

Further in the sub-threshold saturation region we have:-

$$I_s = I_0.exp\left[\frac{K.V_g - V_s}{Vt}\right] \quad \dots\dots \quad (3.3.7)$$

Where:- $K = \frac{C_{ox}}{C_{ox} + C_d}$, $I_0 =$ the pre exponent current,

and $V_t =$ the Thermal Voltage $\approx$ 26mV at 300K

$$\text{and for} \quad V_s = 0 \quad : \quad I_s = I_0.exp\left[\frac{K.V_g}{Vt}\right] \quad \dots\dots \quad (3.3.8)$$

$$\text{or} \quad I_s = I_0.exp\left[\frac{K(Q_{fg} + C_c.V_c)}{C_T.Vt}\right] \quad \dots\dots \quad (3.3.9)$$

$$\text{where} \quad C_T = C_{fg} + C_c \quad \dots\dots \quad (3.3.10)$$

$$\therefore \quad I_s = I_0.exp\left[\frac{Q_{fg}}{Q_T}\right].exp\left[\frac{K_2.V_c}{Vt}\right] \quad \dots\dots \quad (3.3.11)$$

$$\text{where} \quad Q_T = \frac{C_T.Vt}{K} \quad \text{and} \quad K_2 = \frac{K.V_c}{C_T} \quad \dots\dots \quad (3.3.12)$$

Hence, writing $$I_s = W.I_0.exp\left[\frac{K_2.V_c}{Vt}\right] \quad \dots\dots \quad (3.3.13)$$

Where "W" is the weight factor for the floating gate and is given by:-

$$W = exp\left[\frac{Q_{fg}}{Q_T}\right] \quad \dots\dots \quad (3.3.14)$$

From the above we can evaluate "K" and "I_0" from equation (3.3.8.) as we have:-

$$\ln(I_s) = ln(I_0) + \frac{K.V_{fg}}{Vt} \quad \dots\dots \quad (3.3.15)$$

Therefore plotting $\ln(I_s)$ against $V_{fg:}$ as in Fig.3.3.2.

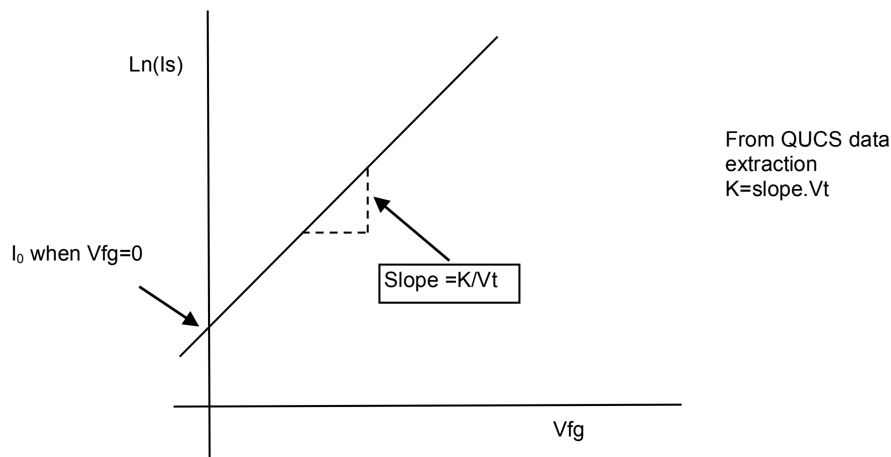


Fig.3.3.2. Plot of $\ln(I_s)$ against V_{fg}

We can use the data extraction features from QUCS to find K and I_0.

3.4. Chapter Summary

Chapter 3 covers the physical structures and principles of operation of floating gate devices. Special emphasis has been paid to the transfer of charge through the insulating oxide onto the floating gate. The principle of Fowler-Nordheim tunnelling has been shown through the band potential and the classic Fowler-Nordheim formula given.

Using the Fowler-Nordheim equation an extensive analysis was carried out for charge transfer onto the floating gate for a tunnelled pulse.

Chapter 4.

Model and Analysis of Floating Gate nMOSFET

4.1. Equivalent Circuit Model

The long channel nMOSFET was the basis of the model. To this was added the capacitive elements associated with the extra control electrode and the coupling capacitor effect of the FG with the bulk semiconductor, and the overlap capacitors associated with the source and drain, as shown in Fig.4.1.1. The dashed lines indicate the modification made in order to take into account the tunnelling terminal and it's associated capacitance.

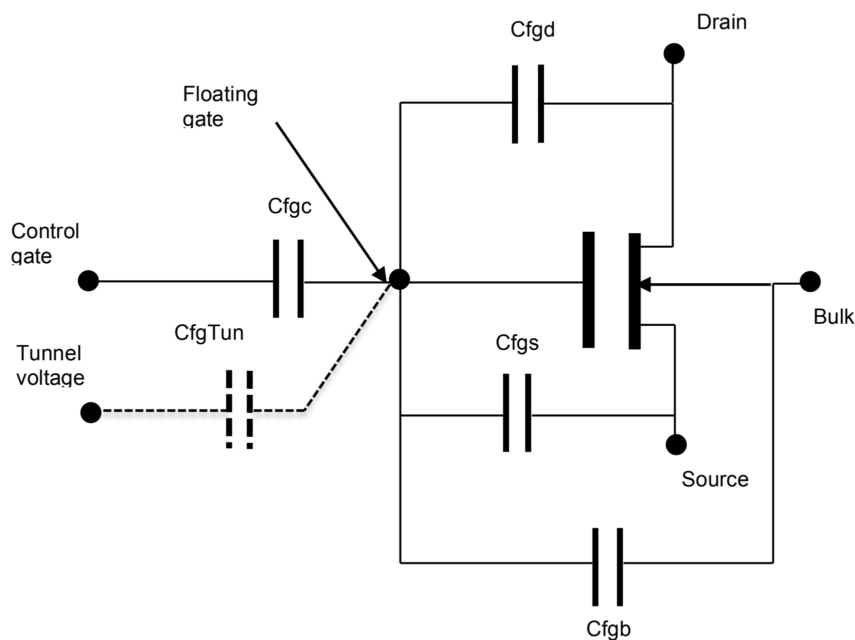


Fig.4.1.1. Equivalent circuit of FGMOSFET

For charge neutrality and utilising the superposition principle we have:-

$$Q_{fg} = Q_{fgc} + Q_{fgd} + Q_{fgs} + Q_{fgb} + Q_{fgTun} \quad \dots\dots \quad (4.1.1)$$

and using superposition we have:-

$$\text{where} \quad V_1 = \frac{C_{fgc}}{C_T}.V_{fgc}$$

$$V_2 = \frac{C_{fgd}}{C_T}.V_{fgd}$$

$$V_3 = \frac{C_{fgs}}{C_T}.V_{fgs}$$

$$V_4 = \frac{C_{fgb}}{C_T}.V_{fgb}$$

$$V_5 = \frac{C_{fgT}}{C_T}.V_{fgTun}$$

$$V_6 = \frac{Q_{fg}}{C_T}$$

Where:- V_1, V_2, V_3, V_4, V_5 and V_6 are the voltages at each node and C_T is the total capacitance.

superimposing:-

$$V_{fg} = V_1 + V_2 + V_3 + V_4 + V_5 + V_6 \quad \dots\dots \quad (4.1.2)$$

and therefore:- $V_{fg} = \frac{C_{fgc}}{C_T}.V_{fgc} + \frac{C_{fgd}}{C_T}.V_{fgd} + \frac{C_{fgs}}{C_T}.V_{fgs} + \frac{C_{fgb}}{C_T}.V_{fgb} +$

$$\frac{C_{fgT}}{C_T}.V_{fgTun} + \frac{Q_{fg}}{C_T} \quad \dots\dots \quad (4.1.3)$$

4.2. Floating Node Analysis Solution

The major problem with a FGMOS is the fact there is no electrical connection with the FG, only through capacitor coupling, which means that simulators cannot cope with charge transfer. In order to overcome this, it was decided to incorporate large parallel resistances with the capacitive elements. The resistance values chosen were such that the time constant of the RC circuit formed were extremely large compared with any duration of simulation: Typically the time constant was set to 10000s

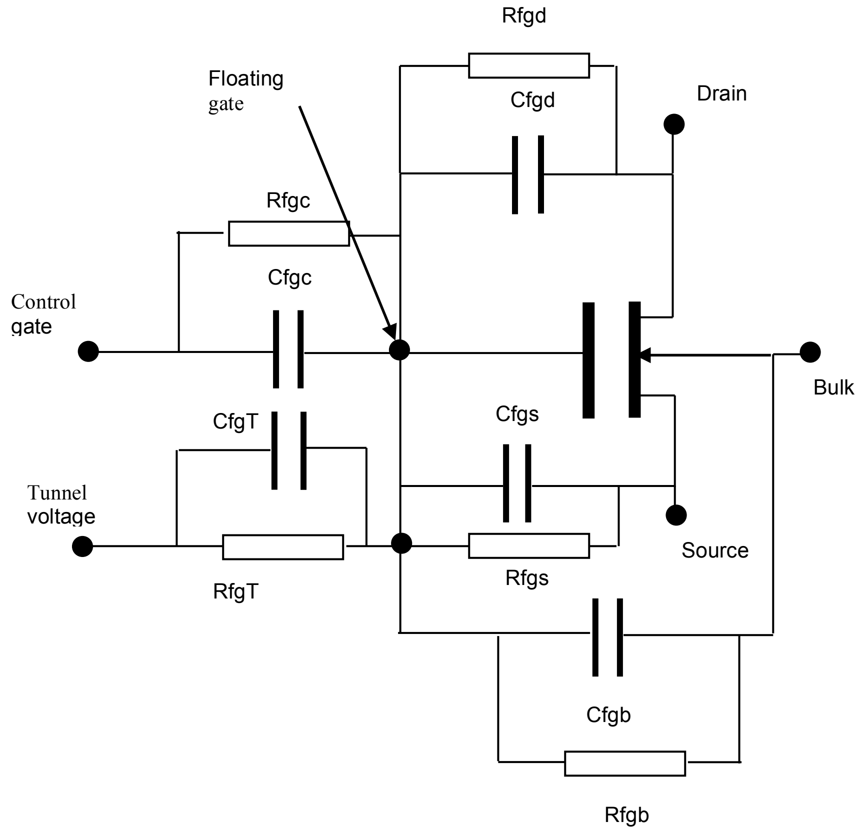


Fig.4.2.1. Equivalent circuit of FGMOSFET for analysis

Also to simplify analysis all the time constants are made equal. This can be done as all time constants will be such that they do not effect the relative short duration of the simulations

$R_{fgC}C_{fgC} = R_{fgD}C_{fgD} = R_{fgS}C_{fgS} = R_{fgB}C_{fgB} = R_{fgT}C_{fgT}$

DC node equation gives:-

$$\frac{(V_{fg} - V_d)}{R_{fgd}} + \frac{(V_{fg} - V_s)}{R_{fgs}} + \frac{(V_{fg} - V_b)}{R_{fgb}} + \frac{(V_{fg} - V_c)}{R_{fgc}} + \frac{(V_{fg} - V_{Tun})}{R_{fgT}} = 0 \quad \dots\dots \quad (4.2.1)$$

re-arranging eq. (4.2.1.)

$$V_{fg}\left[\frac{1}{R_{fgd}}+\frac{1}{R_{fs}}+\frac{1}{R_{fgb}}+\frac{1}{R_{fgc}}+\frac{1}{R_{fgT}}\right]$$

$$=\frac{V_d}{R_{fgd}}+\frac{V_s}{R_{fgs}}+\frac{V_b}{R_{fgb}}+\frac{V_c}{R_{fgc}}+\frac{V_{Tun}}{R_{fgT}} \quad \ldots. \quad (4.2.2)$$

or

$$V_{fg}=\frac{\left[\frac{V_d}{R_{fgd}}+\frac{V_s}{R_{fgs}}+\frac{V_b}{R_{fgb}}+\frac{V_c}{R_{fgc}}+\frac{V_{Tun}}{R_{fgT}}\right]}{\left[\frac{1}{R_{fgd}}+\frac{1}{R_{fgs}}+\frac{1}{R_{fgb}}+\frac{1}{R_{fgc}}+\frac{1}{R_{fgT}}\right]} \quad \ldots\ldots \quad (4.2.3)$$

For the time associated with simulation, and indeed practical applications the Time Constants, τ, are assumed to be very large and can be considered equal. This was achieved by selecting extremely large resistor values.

$\tau = R_{fgd} . C_{fgd} = R_{fgs} . C_{fgs} = R_{fgb} . C_{fgb} = R_{fgc} . C_{fgc} = R_{fgT} . C_{fgT}$ …… (4.2.4)

then

$$V_{fg}=\frac{\left[\frac{C_{fgd}.V_d}{\tau}+\frac{C_{fgs}.V_s}{\tau}+\frac{C_{fgb}.V_b}{\tau}+\frac{C_{fgc}.V_c}{\tau}+\frac{C_{fgT}.V_{Tun}}{\tau}\right]}{\left[\frac{C_{fgd}}{\tau}+\frac{C_{fgs}}{\tau}+\frac{C_{fgb}}{\tau}+\frac{C_{fgc}}{\tau}+\frac{C_{fgT}}{\tau}\right]} \quad \ldots\ldots \quad (4.2.5)$$

or

$$V_{fg}=\frac{\left[C_{fgd}.V_d+C_{fgs}.V_s+C_{fgb}.V_b+C_{fgc}.V_c+C_{fgT}.V_{Tun}\right]}{C_T} \quad \ldots\ldots \quad (4.2.6)$$

where

$$C_T=C_{fgd}+C_{fgs}+C_{fgb}+C_{fgc}+C_{fgT} \quad \ldots\ldots \quad (4.2.7)$$

Note that if $V_s = V_b \rightarrow 0$

$$V_{fg} = \frac{[C_{fgd}.V_d + C_{fgc}.V_c + C_{fgT}.V_{Tun}]}{C_T} \quad \ldots\ldots \quad (4.2.8)$$

Also, provided that $C_{fgc} >> (C_{fgd} + C_{fgT})$, which from the design point of view is true, then:-

$$V_{fg} \to \frac{C_{fgc}.V_c}{C_{fgc}} \to V_c \quad \ldots\ldots \quad (4.2.9)$$

This indicates that before a tunnelling voltage is applied and there is no charge on the Floating Gate, and that the transistor is effectively controlled by the control gate voltage. However once a charge has been accumulated on the floating gate this becomes the dominant controlling voltage.

4.3. Analysis for transient solution.

Assuming $Q_{fg} \to 0$ and C_{fgd}, C_{fgs} and $C_{fgb} \to 0$

Then

$$\frac{(V_{fg} - V_c)}{R_{fgc}} + C_{fgC}.\frac{d(V_{fg} - V_c)}{dt} + \frac{(V_{fg} - V_{Tun})}{R_{fgT}} + C_{fgTun}.\frac{d(V_{fg} - V_{Tun})}{dt}$$

$$= I_{Tc} \quad \ldots\ldots \quad (4.3.1)$$

Where I_{Tc} is the tunnel current

or

$$(C_{fgc} + C_{fgT}).\frac{dV_{fg}}{dt} + V_{fg}.\left(\frac{1}{R_{fgc}} + \frac{1}{R_{fgT}}\right)$$

$$= I_{Tc} + \frac{V_c}{R_{fgc}} + \frac{V_{Tun}}{R_{fgT}} + C_{fgc}.\frac{dV_c}{dt} + C_{fgT}.\frac{dV_{Tun}}{dt} \quad \ldots\ldots \quad (4.3.2)$$

This is a complex equation that may have no analytic solution and may need to be iteratively solved.

4.4. Steady State Solution.

For the steady state solution the following are assumed:-

(i) $V_{Tun} \rightarrow 0$ and $\therefore \frac{dV_{Tun}}{dt} \rightarrow 0$

(ii) $V_C =$ a constant value and $\therefore \frac{dV_C}{dt} \rightarrow 0$

(iii) $I_{Tc} = 0$

Then from equation (4.3.2.):-

$$\left(C_{fgc} + C_{fgT}\right).\frac{dV_{fg}}{dt} + V_{fg}.\left(\frac{1}{R_{fgc}} + \frac{1}{R_{fgT}}\right) = \frac{V_c}{R_{fgc}} \quad \dots\dots \quad (4.4.1)$$

putting $C_{fgc} + C_{fgT} = C_T$

then

$$C_T.\frac{dV_{fg}}{dt} + V_{fg}.\left(\frac{1}{R_{fgc}} + \frac{1}{R_{fgT}}\right) = \frac{V_c}{R_{fgc}} \quad \dots\dots \quad (4.4.2)$$

equation (4.4.2.) can be expressed in the general form:-

$$\frac{dV_{fg}}{dt} + \alpha.V_{fg} = \beta \quad \dots\dots \quad (4.4.3)$$

$$\text{where} \quad \alpha = \frac{1}{C_T}.\left(\frac{1}{R_{fgc}} + \frac{1}{R_{fgT}}\right)$$

$$\text{and} \quad \beta = \frac{V_c}{R_{fgc}.C_T}$$

$$\text{hence} \quad \frac{dV_{fg}}{\left(\beta - \alpha.V_{fg}\right)} = dt \quad \dots\dots \quad (4.4.4)$$

$$\text{this is a standard integral form} \rightarrow \int \frac{dx}{X} = \frac{1}{b}.ln|X| \quad \text{where } X = a + bx$$

integrating this standard form gives:-

$$\int \frac{1}{\left(\beta - \alpha.V_{fg}\right)} dV_{fg} = \int dt. \quad \dots\dots \quad (4.4.5)$$

and

$$t = \frac{1}{\beta}.\left[\frac{1}{\left(-\frac{\alpha}{\beta}\right)}.\ln\left|1-\frac{\alpha}{\beta}.V_{fg}\right|\right]$$

$$t = -\frac{1}{\alpha}.\ln\left(1-\frac{\alpha}{\beta}.V_{fg}\right)$$

hence

$$-\alpha t = \ln\left(1-\frac{\alpha}{\beta}.V_{fg}\right)$$

or

$$e^{-\alpha t} = 1-\frac{\alpha}{\beta}.V_{fg}$$

and therefore

$$V_{fg} = \frac{\beta}{\alpha}.(1-e^{-\alpha t})$$

substituting in the values for α and β we get:-

$$\frac{\beta}{\alpha} \rightarrow \frac{\frac{V_C}{R_{fgC}.C_T}}{\frac{1}{C_T}.\left[\frac{1}{R_{fgC}}+\frac{1}{R_{fgT}}\right]} = \frac{V_C.R_{fgT}}{\left(R_{fgT}+R_{fgC}\right)}$$

giving:-

$$V_{fg} = \frac{V_C.R_{fgT}}{\left(R_{fgT}+R_{fgc}\right)}.\left[1-e^{-\frac{1}{C_T}.\left(\frac{1}{R_{fgT}}+\frac{1}{R_{fgc}}\right)}\right] \quad \ldots \ldots. \quad (4.4.6)$$

$$\text{if} \quad \ldots\ldots\ldots\ldots\ldots. \quad \frac{1}{R_x} = \frac{1}{R_{fgT}} = \frac{1}{R_{fgc}}$$

then the Time Constant, τ, for eq.(4.4.6) = $C_T.R_X$

and if

$$C_T.R_X \rightarrow \infty$$

and

$$V_{fg} \rightarrow V_c \quad \ldots\ldots \quad (4.4.7)$$

This takes us back to the solution obtained for the DC node equations that is to be expected as the Tunnelling voltage pulse has been removed.

4.5. Chapter Summary

Chapter 4 shows the development of the created floating gate model. This basically consists of a number of capacitances associated with the floating gate and the integrated terminals of the n-type enhancement MOSFET. Analysis of this model has been carried out using the superposition principle to establish the voltage on the floating gate. This shows the relationship of the voltage to the charge stored on the floating gate and the total equivalent circuit capacitance.

Total analysis has been enabled and carried out by adding extremely large resistances in parallel with the equivalent capacitances. The analysis has been shown for D.C. and transient voltages.

Chapter 5.

Floating Gate Characteristics

5.1. Theoretical Characteristics

The theoretical characteristics of a floating gate device are similar to a MOSFET and are determined by the following equations [10,20], that have been implemented in the QUCS EKVv2.6 model.

(i) Linear Region

$$I_S = I_0 . exp\left[\frac{KV_{fg} - V_s}{Vt}\right] . \left[1 - exp\left(\frac{V_{ds}}{Vt}\right)\right] \quad \ldots \ldots \quad (5.1.1)$$

$$\text{where} \quad \mathrm{K} = \frac{C_{ox}}{C_{ox} + C_d} \quad \text{and} \quad Vt = \text{thermal voltage } (\approx 26\text{mV at } 300 \text{ Kelvin})$$

(ii) Saturation Region

$$I_S = I_0 . exp\left[\frac{KV_{fg} - V_s}{Vt}\right] \quad \ldots \ldots \quad (5.1.2)$$

(iii) Cut off.

$$I_s \rightarrow 0 \quad \ldots \ldots \quad (5.1.3)$$

The Linear and Saturation Regions are shown in Fig.5.1.(a) and (b) . The schematic utilises the QUCS software and a Floating Gate device that has been developed. For this simulation no voltage is applied to the floating gate terminal so the channel formation is controlled entirely by the 1 Volt applied to the control terminal.

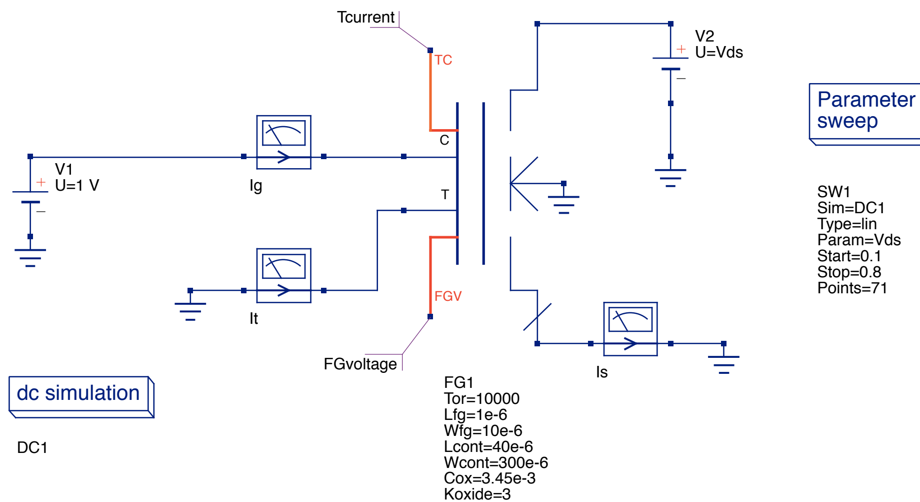


Fig.5.1.1.(a) QUCS Schematic used to obtain Floating Gate MOS Characteristic for Linear and Saturation Regions for Is v Vds

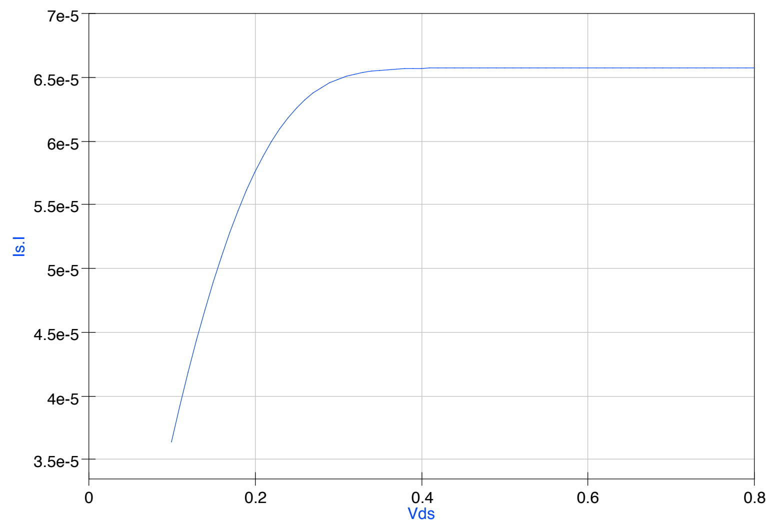


Fig.5.1.1.(b) Linear and Saturation Characteristic for schematic shown in Fig.5.1.1.(a) Is v Vds.

For Fig. 5.1.1.(b) a constant gate voltage, V_{gs} = 1V, is applied, which is above the threshold voltage. The device operates in the linear region until V_{ds} reaches 0.3 – 0.4 when it starts to enter the saturation region, where excess negative charges are pulled towards the drain and reduces the channel area at the drain. This gradually limits the current and makes it more independent of increase in V_{ds}.

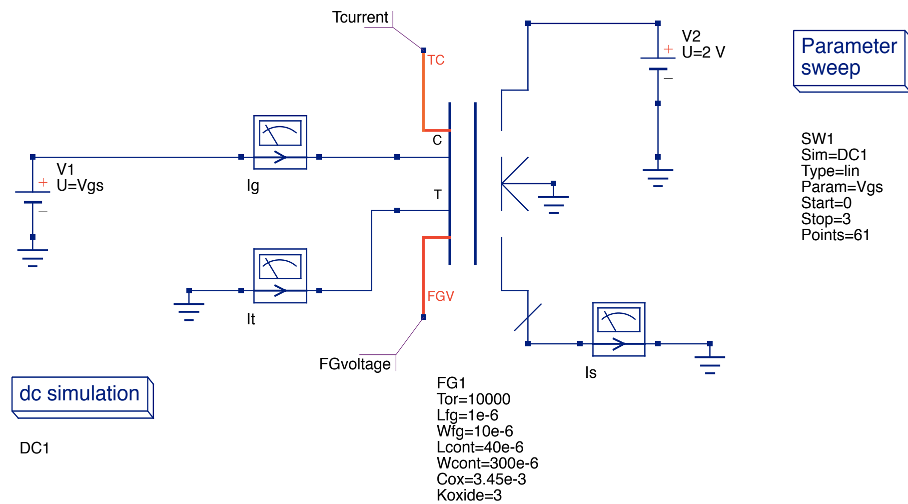


Fig.5.1.2.(a) QUCS Schematic used to obtain Floating Gate MOS Linear and Saturation Characteristic, Is v Vgs.

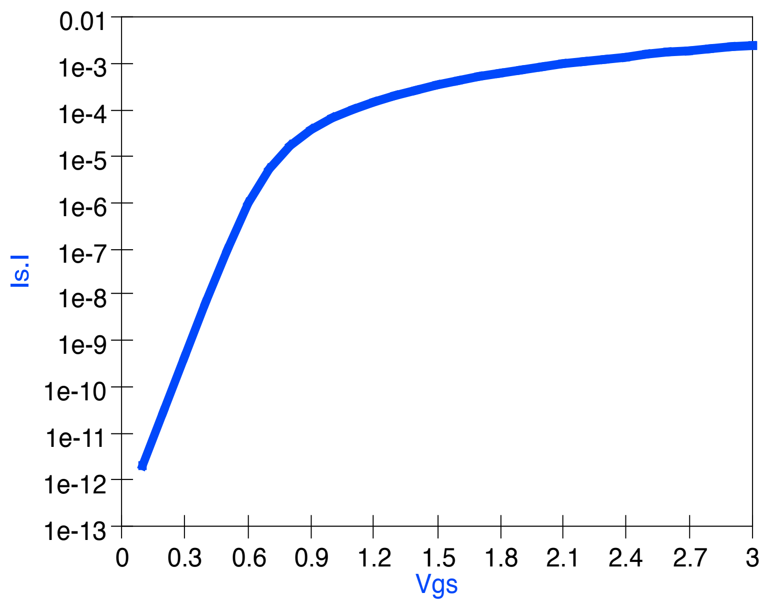


Fig.5.1.2.(b) Linear and Saturation characteristic for schematic shown in Fig.5.1.2.(a), Is v Vgs

For the schematic shown in Fig.5.1.2.(a) the drain-source voltage is set at 2V and the gate-source voltage is sweep from 0.1 V – 3 V. Initially the source current shows weak inversion(subthreshold). Below the threshold voltage (approx..4V_t) the mobile charge carriers do not disappear abruptly but reduce slowly due to the

capacitive voltage between the gate – source and source – bulk, and current transport by diffusion is important.

Above the threshold voltage the square law region is entered.

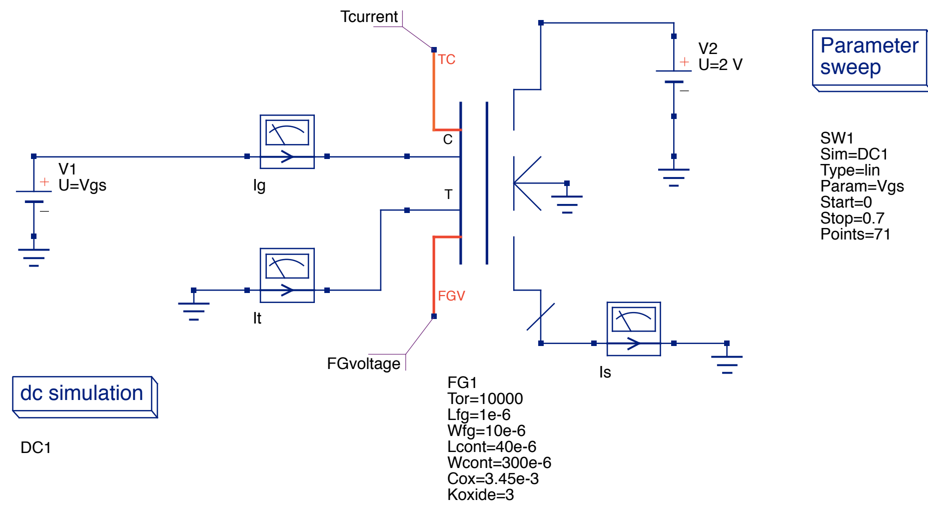


Fig.5.1.3.(a) QUCS Schematic used to obtain Floating Gate MOS characteristic response in subthreshold region.

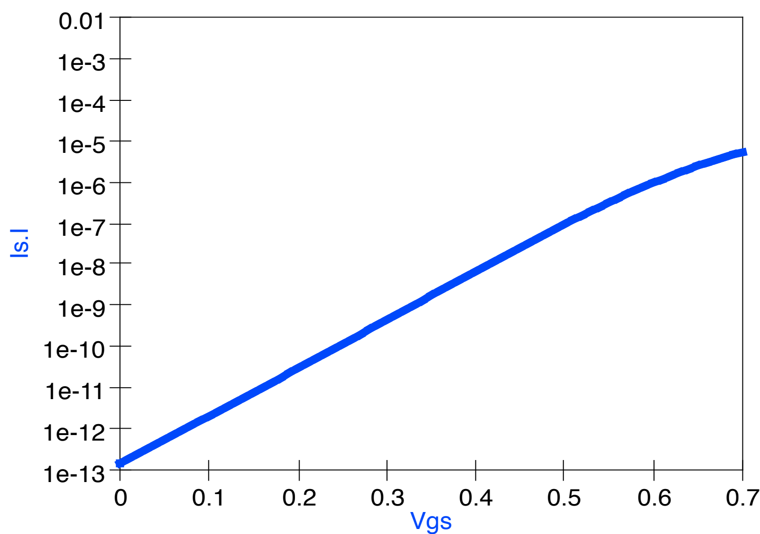


Fig.5.1.3.(b) Subthreshold characteristic for schematic shown in Fig.5.1.3.(a), I_s v V_{gs}

For the response shown in Fig.5.3.1.(b). it can be seen that below the threshold voltage in weak inversion that a current still flows between drain and source due mainly to surface charge. This continues even when V_{gs} is 0V.

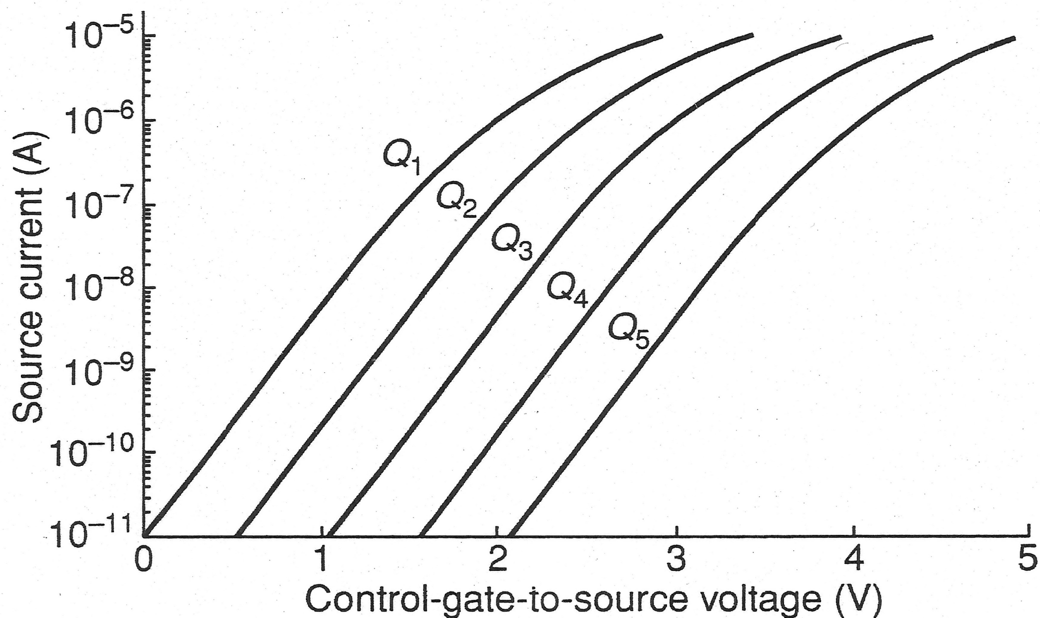


Fig.5.1.4. Shift of V v I characteristic as charge is accumulated on Floating Gate [5].

Fig.5.1.4. shows the target effect that is required for a floating gate device. Through applying high voltage pulses to the floating gate terminal Fowler-Nordheim charging takes place through the oxide layer and charges accumulate on the floating gate, so effectively shifting the threshold voltage.

5.2. Chapter Summary

Chapter 5 considers the overall characteristics that are expected for a floating gate n-type enhancement MOSFET. Simulations have been carried out for the device in the linear and saturation regions. The shift in the characteristic has been shown for the different levels of charge transferred on to floating gate through charge

tunnelling. This indicates the change in the characteristic that the simulation model would be expected to achieve.

Chapter 6.

QUCS Software

6.1. QUCS software package.

The acronym QUCS stands for Quite Universal Circuit Simulator. It is an open source circuit simulator and has been developing since 2004 when initially a team of scientists and engineers decided to take part in the MOS-AK Verilog-A standardisation initiative. The software was to be developed using GNU/Linux under General Public License. It is available for most operating systems including GNU/Linux, Windows®, Solaris®, NetBSD, FreeBSD and MacOS®. The simulator has developed rapidly since this time and previously reported details of the simulators capabilities can be found from ref[2,3,6,10].

As with most simulators, circuits are represented by textual netlists and/or schematic diagrams. A simulation engine then carries out the circuit simulation on the basis of these representations and according to the analysis required e.g. DC, AC or transient. Further, results are stored and can be displayed by a post simulation processing system both in tabular and graphic format. Again, as with all simulators, individual components are represented by a mathematical model defining the components physical operation. The complete architectural structure is shown in Fig.1.1. The use of subcircuits is also a feature of modern simulators and enables a hierarchical structures for the building of more complicated circuits. With the release of QUCS 0.0.12 a new modelling component was introduced called the EDD. This enables QUCS to formulate device current as a function of voltage and also device charge to be formulated as a function of current and voltage.

The software library contains a large number of models for compact semiconductor devices and it has been the intention of this research to develop a compact model of a floating gate device so that it sits inside the software library and can then be incorporated as an integrated part of circuit design. The software is fully integrated, providing circuit simulation and analysis routines, with advanced device and circuit modelling tools. It also provides a graphical environment for circuit schematic drawing, or netlist preparation, and simulation control, as shown in Fig.6.1.1.

The software consists of a suite of stand alone programmes that are interactive through a graphical user interface, GUI. For the purpose of this work the GUI enables schematics to be created, simulations to be setup and run, and results to be displayed in graphical and tabular form.

For the schematic implementation, data can be taken from component symbols, numerical values, algebraic equation blocks, user defined subcircuits, library components and non-linear equation defined devices along with simulation directive icons as shown in Fig.6.1.2. The underlined terms being indicative of the work to be carried out by this research for floating gate devices. The simulation package overcomes one of the most important deficiencies of SPICE and that is the lack of subroutine parameters that can be passed as component values to the circuitry within the subcircuit, and an inability to calculate component values, or other quantities, using variables and algebraic equations attached to a subcircuit.

QUCS software is proving extremely important in the design of semiconductor devices and incorporates a large number of physical processes defined by algebraic equations[6], reference Appendix 2.

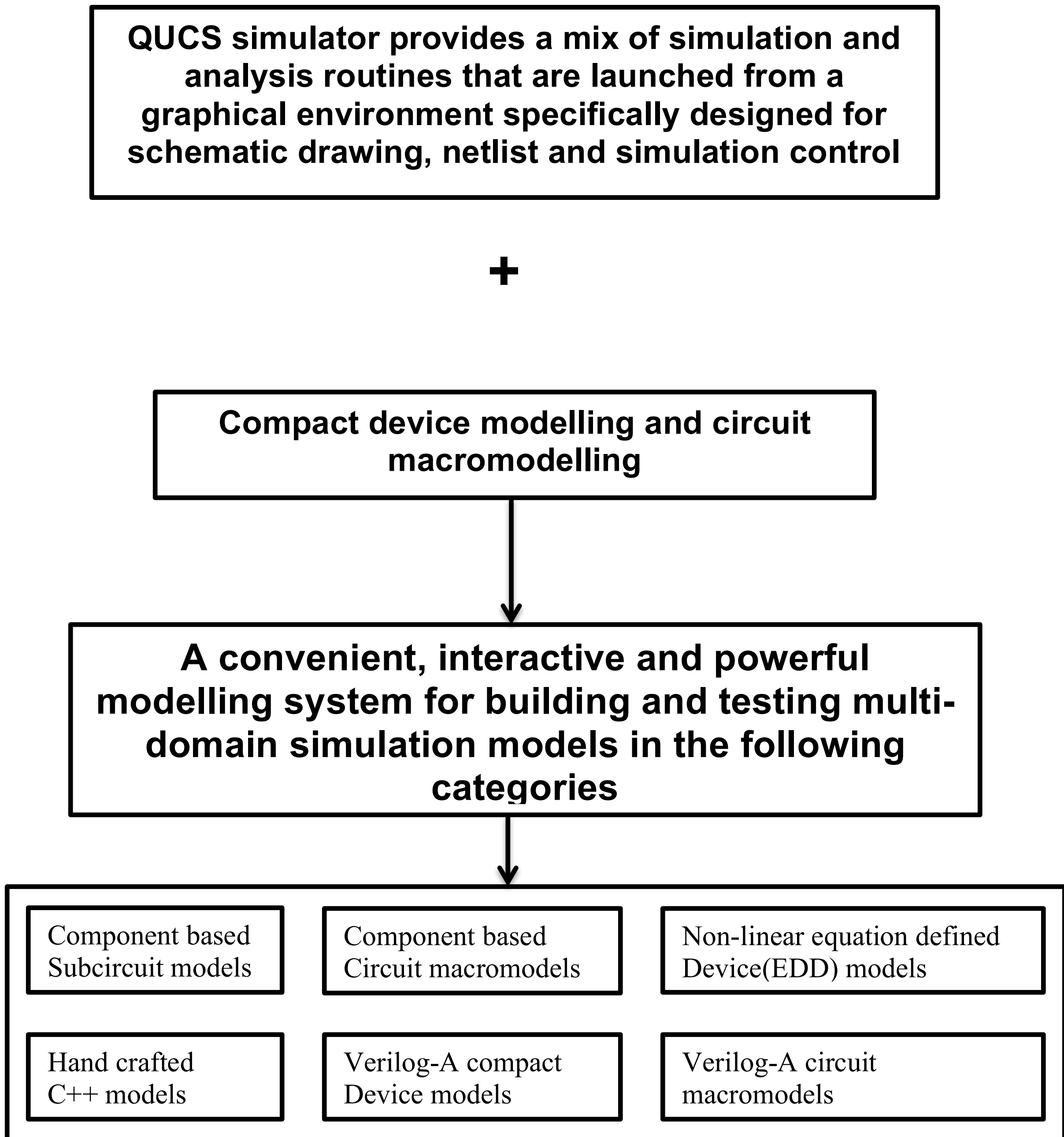


Fig.6.1.1. Chart for implementation of circuit simulation within QUCS