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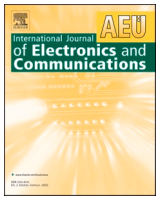

On-Chip Terahertz antenna array based on amalgamation of metasurface-inspired and artificial magnetic conductor technologies for next generation of wireless electronic devices

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ABSTRACT

The paper presents a feasibility study on an innovative terahertz (THz) on-chip antenna array designed to reliably meet the high-performance connectivity requirements for next generation of wireless devices to enable bandwidth intensive applications, superfast fast streaming, bulk data exchange between internet of things (IoT) devices/smartphones and the development of holographic video conferencing. The significantly smaller wavelength of the THz-band and metasurface-inspired and artificial magnetic conductor (AMC) technologies are exploited here to realize an on-chip antenna. Several experimental on-chip antenna arrays of various matrix sizes were investigated for application at millimeter-wave/Terahertz RF front-end transceivers. The technique proposed here is shown to enhance the antennas impedance bandwidth, gain and radiation efficiency. Purely for experimental purposes a 2 × 24 radiation element array was fabricated. It exhibits an average measured gain of 20.36 dBi and radiation efficiency of 37.5% across 0.3–0.314 THz. For proof of the concept purposes a THz receiver incorporating the proposed on-chip antenna was modelled. The results show that with the proposed antenna array a THz receiver can provide a gain of 25 dB when the antenna is directly matched to low-noise amplifier stage.

1. Introduction

To run bandwidth intensive applications or exchange huge amount of databetween devices such as digital cameras/camcorders and laptops or smartphones, the next generation of wireless devices will need to operate at significantly higher data-rates and connect seamlessly. This is only possible at the Terahertz (THz) band (0.1–10 THz), which is the key enabling technology to unleash the very large bandwidths necessary for Terabit per second (Tb/s) transmission. Moreover, this technology will alleviate the spectrum scarcity problem and promote the realization of high-definition holographic video conferencing and ultra-high speed data dissemination in data centers. In fact, in 2019 Apple Inc. filed a patent US11099072B2 to embed THz technology on board a smartphone. This will entail the development of a THz system-on-chip (SoC).

The need for system-on-chip devices for various consumer electronics has increased significantly with the evolution of wireless technology. This has been made possible with the advancement of very large-scale integration (VSLI) technology that enables integration of various functional modules of a complete system on a single integrated circuit (IC) board; however, the antenna remains the largest component outside of the IC because its dimensions are a function of the operating wavelength. Integration of the antenna and other functional modules of a system on the same chip is highly desirable to realize a compact and economical solution. The significantly smaller wavelength provided by the THz-band is exploited here to realize on-chip antennas.

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Integrated circuit technology has advanced tremendously over the last two decades [1] resulting in integration of billions of transistors in a few square millimeters [2]. This has resulted in the development of multiband and multi-standard wireless communication transceivers [3,4] that are composed of (i) a digital baseband unit for signal processing, (ii) a mixed-signal unit for signal conditioning, (iii) RF front-end unit for modulating/demodulating the baseband signal, and (iv) antenna for transmitting/receiving the modulated carrier signal. Conventionally, wireless communication systems have been constructed by cascading these units in either a linear or lateral architecture. These architectures permit individual units to benefit from the latest technological developments. For instance, the use of power amplifiers (PA) which are based on III–V compound semiconductor technology can offer characteristics of high gain and excellent noise-figure at high frequencies; the use of complementary metal-oxide semiconductor (CMOS) technology for digital circuitry applications can offer the benefit of ultra-low power consumption; and the use of low-loss dielectric substrates for antenna implementation. However, as discussed in [1,5], implementation of a transceiver based on a linear architecture has the disadvantage of requiring a significantly larger chip area that thereby inhibits miniaturization. Reducing the size of the transceiver is one of the major impetuses in wireless technology. Lateral architecture, on the other hand, enables miniaturization that is conducive for implementing system-in-package (SiP). Nevertheless, even with these approaches, the antenna is implemented outside the package because its dimensions correlate with the wavelength of the operating signal [6]. In addition, integrating the various transceiver module technologies especially at higher frequencies is a great challenge. Because of the latest advances in silicon technologies, on-chip integration of digital baseband and RF front-end has made possible the realization of system-on-chip (SoC) [7,8]. As a result, the use of millimeter-waves (mm-Wave) and terahertz bands are becoming increasingly attractive for various personal wireless devices. Besides the availability of a generous bandwidth at mm-Wave and THz-bands, this region of the electromagnetic spectrum benefits from significantly smaller wavelengths, which allows for the design of miniature antennas [9–16]. This attribute makes the implementation of on-chip antennas an attractive proposition for applications at these bands.

The standard CMOS process provides a suitable platform for integrating the mm-Wave antenna on a chip, which offer the advantages of a high level of integration, robustness due to no external bonding wires, low fabrication cost and high yield for mass production. However, there are many challenges to overcome for implementing on-chip antennas in particular the low gain, constraints in the antenna configuration, and inaccurate characterization of on-chip antenna as probe-based measurements are easily influenced by coupling and interference effects from the integrated circuits and the probe itself. Examples of on-chip antennas recently reported in literature include a dual-band on-chip meander-line monopole antenna which was fabricated on 65-nm bulk CMOS chip [17]. It exhibits a measured gain of −10 dBi at 28 GHz over a bandwidth of 5.3%, and 0 dBi at 60 GHz over a bandwidth of 5.9%. Radiation efficiency of 45% and 30% are reported at 28 GHz and 60 GHz, respectively. The surface area of the antenna is 0.25×0.3 mm^2. Reported in [18] is a terahertz on-chip antenna with chip-integrated dielectric resonator (DR). It uses a comb-shaped dipole antenna that is implemented on a silicon substrate using 65-nm CMOS technology. The fabricated antenna is reported to provide a peak gain of 8.6 dBi and a maximum radiation efficiency of 44% at 295 GHz. In [19], a double-folded dipole antenna was fabricated using 130-nm SiGe BiCMOS technology. It was implemented using localized backside etching (LBE) and integrated with the transceivers. Arranging the LBE areas around the radiating element is shown to effectively attenuate substrate surface waves and ensure mechanical stability and reliability. Results show the antenna has a 5 dBi gain at 170 GHz. In [20], an octagonal shorted annular ring (OSAR) antenna array is reported that is based on 130-nm SiGe BiCMOS technology. The antenna consists of an annular ring patch with an array of shorted pins to create a cavity which is necessary to enhance the gain and reduce surface waves. The 2×1 OSAR antenna array, which is implemented on a die area of 550×1100 μm^2, has −10 dB impedance bandwidth of 17 GHz, peak gain of 4.1 dBi and radiation efficiency of 38 % at 320 GHz.

The research work presented in this paper provides the design of an innovative subwavelength antenna for on-chip integration. The proposed antenna combines metasurface (MTS)-inspired and artificial magnetic conductor (AMC) technologies. MTS is realized here by constructing a periodic arrangement dielectric unit-cells on a thin conductive layer on top of a dielectric host. The unit-cells are engineered to interact with the impinging electromagnetic waves in a specific way to modify the dispersion characteristics of surface [15–22]. Implementation of AMC was originally reported in [23–25] using grounding pins. Because the grounding pins complicate the fabrication of AMC surfaces, Yang et al. in [23] devised an AMC surface without the use of ground pins. In this paper AMC is implemented on a dielectric medium of a specific thickness that mimics the characteristics of an artificial magnetic conductor. On-chip antenna arrays of various sizes are investigated. The large array size is shown to exhibit characteristics of wide impedance bandwidth, high-gain, and high radiation efficiency. The proposed on-chip antenna arrays, which were constructed on a 35 μm thick silicon wafer, are shown to be viable for applications in mm-Waves and THz integrated circuits.

The paper is organized as follows. Section II discusses the pros and cons of on-chip antennas. Section III presents the advances in on-chip antennas and the principles behind the proposed THz antenna. Section IV describes the design of the proposed on-chip antenna. Section V presents the simulation results of a THz receiver incorporating the proposed on-chip antenna. The performance of the proposed on-chip antenna array is compared with previously reported on-chip antennas in Section VI. Finally, the paper is concluded in Section VII.

2. Advantages and challenges of on-chip antennas

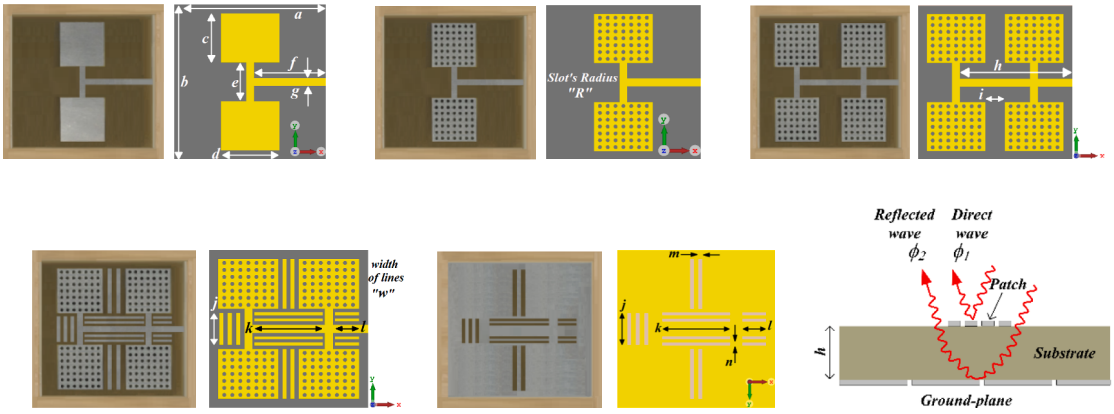
A) Maximizing On-Chip Power Transfer.

Antennas are essential components in wireless systems. Their function is to interface the receiver/transmitter modules to the free-space propagating medium. To maximize the antenna's transmission power, it is vital to optimize its radiation efficiency. To accomplish this the antenna needs to be properly impedance matched with the transmitter/receiver module and the free space environment. Designing a matching circuit involves transforming complex impedances from or to typically 50 Ω. In the case of a receiver module, it's necessary to realize optimum impedance matching between the low-noise amplifier (LNA) and receive antenna; in the case of a transmitter module, matching is required between the power amplifier (PA) and the transmit antenna [26].

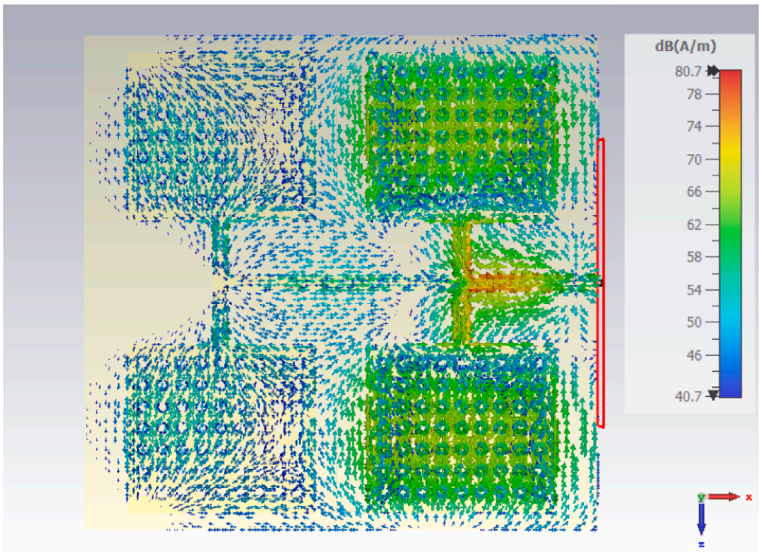
In the case of high frequency systems operating at mm-Waves, the transceiver IC is connected to the antenna feed point using bond-wires. Because the bonding-wires cannot be accurately characterized especially at high frequencies this can severely affect the matching circuit and therefore compromise the efficiency of the antenna. The solution is to eliminate the uncertainty of bonding-wires. The strategy to achieve is to implement the antenna on the chip itself, which eliminates the need for a matching network. Hence, space is saved as the IC can be directly conjugately matched with the antenna.

B) On-Chip Substrate.

Antennas can be implemented on standard silicon substrates however such substrates are highly lossy due to the low substrate resistivity. In addition, the excitation of RF energy at the antenna is confined within the silicon substrate by its high dielectric constant. This is a major drawback of current on-chip antenna implementations. The high dielectric constant restricts the energy to radiate efficiently into the free-



(d) (e) (f)



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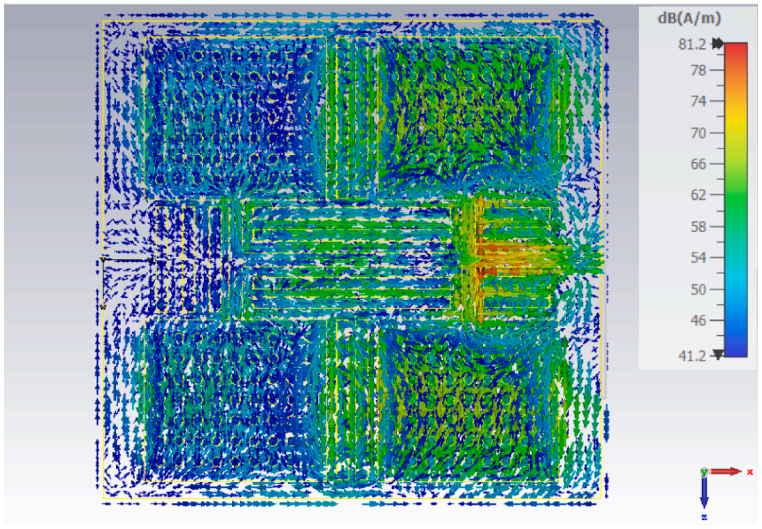
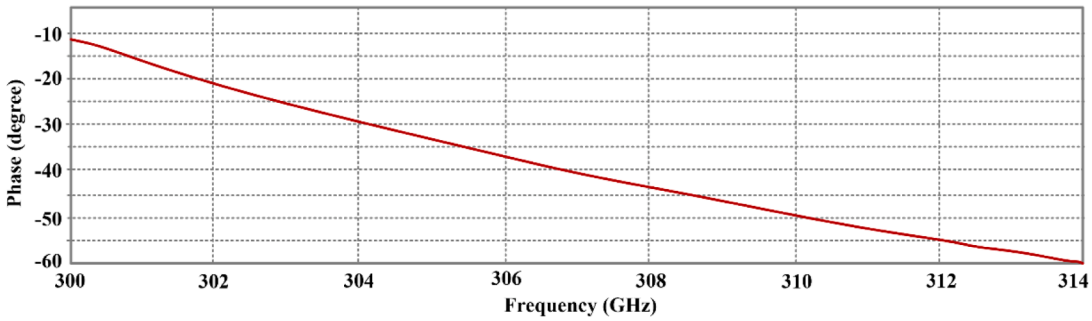


(h)

Fig. 1. Layouts and fabricated prototype of the proposed on-chip antennas. (a) 2 × 1 array antennas, (b) 2 × 1 on-chip MTS antenna array, c) 2 × 2 on-chip MTS antenna array, (d) 2 × 2 on-chip MTS antenna array with AMC ground-plane and decoupling open-ended microstrip-lines, (e) AMC ground-plane for "d", (f) cross-section of patch antenna, (g) Surface current density of the 2 × 2 on-chip MTS antenna array with no AMC ground-plane and no decoupling open-ended microstrip-lines, (h) Surface current density of the 2 × 2 on-chip MTS antenna array with decoupling elements and ground-plane slots, (i) phase response at the input port of the 2 × 2 on-chip MTS antenna array with decoupling elements and ground-plane slots, (j) optimized 2 × 24 on-chip MTS-AMC antenna array, and (k) AMC ground-plane for "f".



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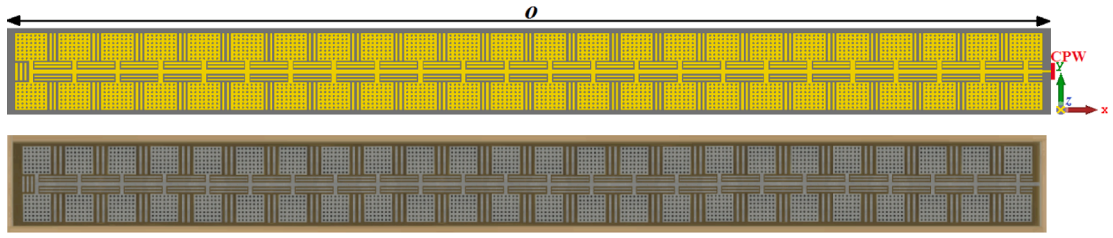

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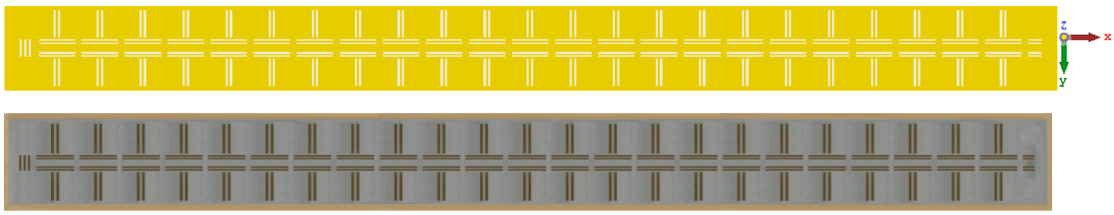


(k)

Fig. 1. (*continued*).

space medium. In [9] the 77 GHz dipole antenna that is implemented on a silicon layer radiates with an efficiency of less than 5%. Moreover, substrates with high dielectric constants and low resistivity dissipate most of the power as heat, which can be detrimental to the overall performance of the on-chip system. The other factor affecting the performance of antennas is surface waves, which are created in thick high dielectric constant substrates. It is therefore important to limit the antenna footprint when fabricated on silicon substrate. One technique to neutralize surface waves is to use a multilayer substrate where silicon dioxide (SiO_2) layer is deposited on a silicon layer. The antenna is constructed on the surface of the SiO_2 layer which has a ground-plane on its underside. The purpose of the ground-plane is to act as a shield and to reflect the radiated energy from the antenna in the upward direction. This stops the radiated energy from being absorbed into the silicon layer. With existing semiconductor technology, the thickness of the SiO_2 layer is limited to about 15 μm. Because of the proximity of the antenna to the ground-plane, electric current is induced in the ground-plane, which is dissipated as heat. Microstrip antennas exhibit a similar problem at frequencies under 100 GHz. This is because by locating the ground-plane at the bottom of the substrate causes unwanted EM coupling with the IC modules. The solution to prevent this from happening is to excite the antenna through a coplanar waveguide. Alternatively, the antenna can be implemented under the silicon layer, however, this would introduce additional complexity in the form of through-silicon-vias needed to connect the antenna to the IC.

C) Characterization of On-Chip Antennas.

In practice, it is likely to observe discrepancies in the performance of the fabricated on-chip antenna with the predicted simulation analysis. This can be attributed to various factors including inaccurate simulation models, fabrication tolerances, post fabrication processing of the silicon wafer, and unwanted electromagnetic coupling with other transceiver modules on the wafer. These inconsistencies can have an impact on the antenna's characterizing parameters such as the impedance bandwidth, gain, and radiation characteristics.

Antennas are conventionally characterized by their performance metrics such as gain, radiation efficiency, and radiation patterns. The general approach is to locate a known transmitter from the antenna under test (AUT) at a given distance in an anechoic chamber. The magnitude of the transmitter output is a known quantity, as is the loss of cabling. Similarly, the sensitivity of the receiver attached to the AUT is also known. The path-loss over the distance between the two antennas can then be calculated. With this setup, the magnitude of the signal power measured at the receiver is used to determine the gain of the AUT. Antenna radiation pattern can be determined by placing the AUT on a rotating platform and measuring the magnitude of the received signal at increments as the platform is rotated. This approach is not recommended for on-chip antennas for several reasons namely: (i) the fragility of the silicon wafer which can be easily damaged; (ii) the tips of the wafer probes used to excite the antenna are delicate and can be easily damaged during measurement; (iii) the large probe-arm can affect the measured results; (iv) the probes need to be placed accurately on the bond pads using a microscope which may block the movement of the antenna during the test procedure; and (v) the wafer probes have to be calibrated. To circumvent these issues, several pioneering on-chip antenna characterization methods have been proposed in [27–30].

3. Advances in on-chip antennas

The success of on-chip antennas has led to their application in the emerging technology of THz, a frequency band that lies between the

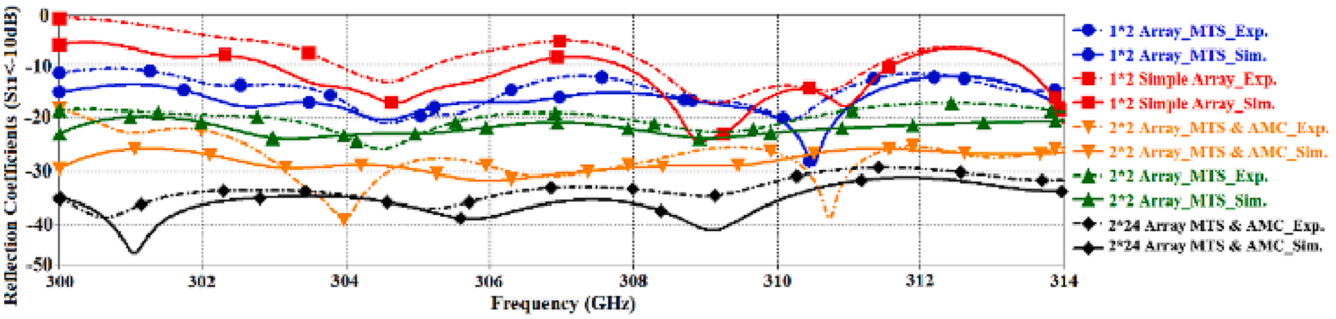


Fig. 2. Reflection-coefficient responses of the on-chip antenna array for different conditions.

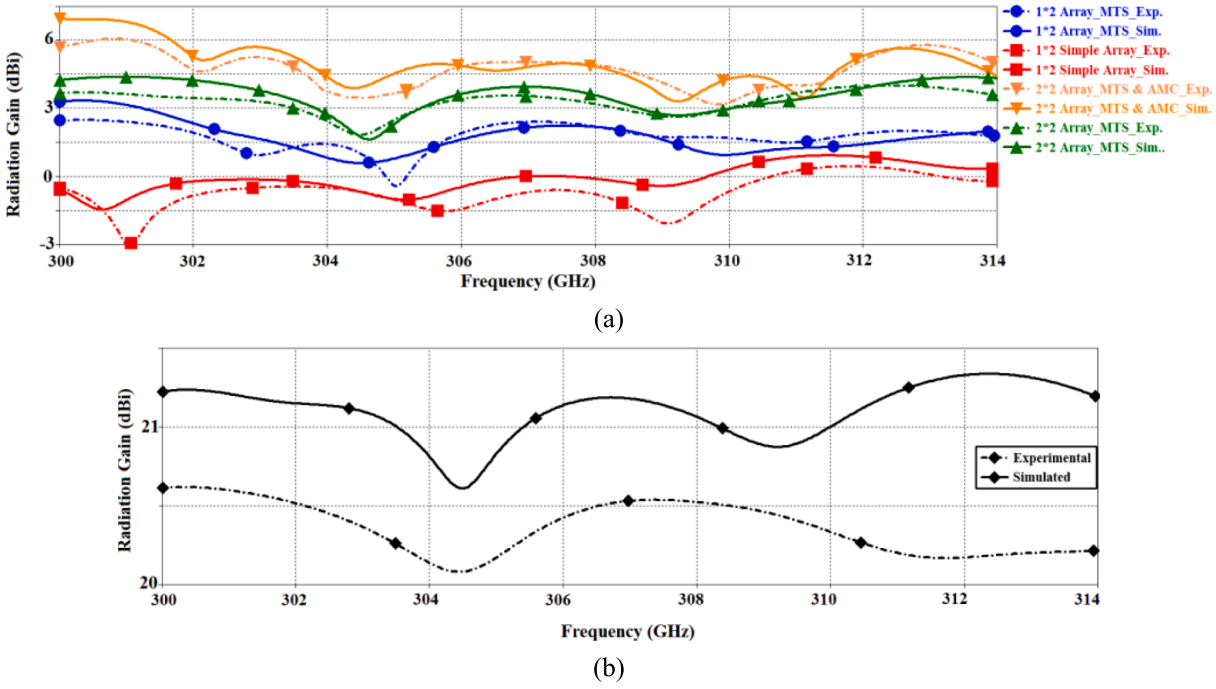


Fig. 3. Radiation gain of the (a) 2 × 1 and 2 × 2 on-chip antenna arrays for different cases, and (b) optimized 2 × 24 on-chip MTM-AMC antenna array.

microwave and infrared domain (0.1 THz to 10 THz). The shorter wavelength of THz wave provides higher resolution of images and therefore greater detail of targets can be obtained. Unlike optical and infrared bands, THz waves can penetrate obscuring materials such as clothing, wood and dust, with relatively little loss. THz imaging and sensing have potential for various applications as reported in [31,32]. This section summarizes the impetus of on-chip antennas for THz applications.

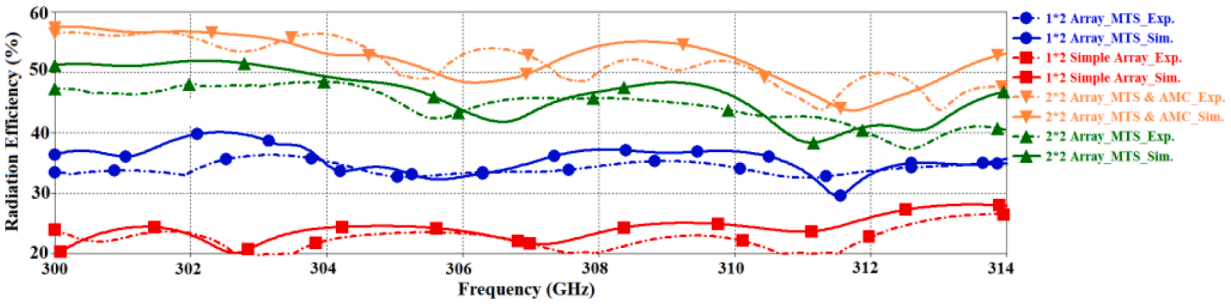
A) Terahertz On-Chip Antennas.

Recent advances made in silicon technology and its lower cost makes it a rival to III-V compound semiconductor technologies [33–35]. The design of on-chip THz antennas is accompanied by numerous challenges, such as fabrication of nano-scale structures, low radiation efficiency, and issues of characterizing the antenna as described above. The antenna design proposed in this paper is aimed for on-chip implementation for operation across 0.3–0.314 THz. This antenna is based on innovative techniques based on MTS and AMC technologies that promote miniaturization and which make on-chip THz antennas a feasible prospect.

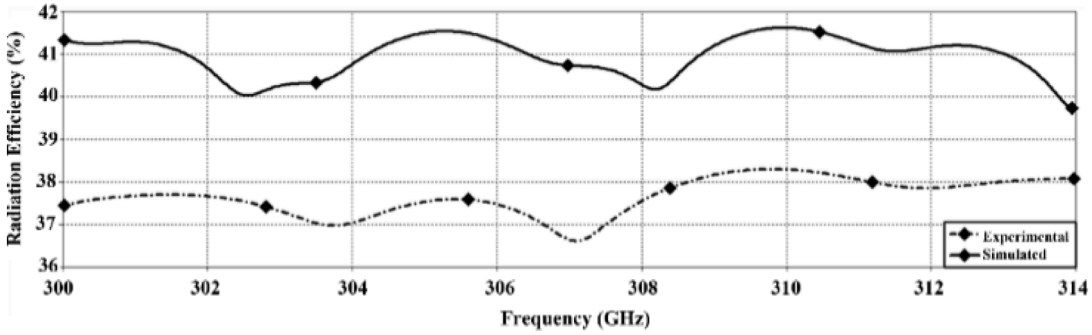
B) Principles Behind the Proposed THz On-Chip Antenna Design.

The initial antenna design proposed here for on-chip applications is a simple 2 × 1 array that is based on a standard square patch shown in Fig. 1(a). Ground-plane (GND) is employed here to prevent backfire radiation from the antenna, and the slots in the ground-plane inhibit surface-wave excitation. In the second iteration of the design process, the patches are converted to metasurfaces. This is achieved by incorporating a periodic array of subwavelength circular dielectric slots on the patches to manipulate its EM response [25]. Hence, with this technique, we can engineer the dispersion characteristics of the antenna. The distribution of individual slots is instrumental in determining the response of the surface. This characteristic differentiates the metasurfaces from frequency selective surfaces (FSS). In fact, the resonant elements constituting FSS are of the order of the operating wavelength and the elements are periodically spaced by λ/2 gap. The periodic array of dielectric slots in the patch antenna essentially results in a slow wave structure. This is because the slots effectively reduce the phase velocity of the waves propagating over it. As the antenna dimensions are a function of the phase velocity, by reducing the phase velocity the antenna size can be reduced without compromising the frequency range over which it operates. This property is used here to miniaturize the on-chip antenna.

On-chip mm-Wave antennas are afflicted by the ground image currents, which are induced by lossy substrate on which the antenna is



(a)



(b)

Fig. 4. Radiation efficiency of the (a) 2 × 1 and 2 × 2 on-chip antenna array for various scenarios, and (b) optimized 2 × 24 on-chip MTM-AMC antenna array.

Table 1
Structural parameter dimensions.

Parameter	*a*	*b*	*c*	*d*	*e*	*f*
Value (μm)	417	434	142	158	104	196
Parameter	*g*	*h*	*i*	*j*	*K*	*l*
Value (μm)	23	313	50	92	200	67
Parameter	*m*	*n*	*R*	*o*	*Substrate thickness*	
Value (μm)	11	10	4	5021	35	

Table 2
Average Impedance Matching Values for the Different Arrays.

On-chip antennas	Simulated impedance match (S_{11}) in dB	Measured impedance match (S_{11}) in dB
2 × 1 simple array	−9.1	−7.4
2 × 1 on-chip array based on MTS	−15.4	−14
2 × 2 on-chip array based on MTS	−22.3	−20.5
2 × 2 on-chip array based on MTS-AMC	−28.1	−24.6
2 × 24 on-chip array based on MTS-AMC	−35.4	−31.4

constructed and the presence of ground-plane below the chip. This has a negative impact on the antenna's gain and radiation efficiency. We have shown here that by defecting the ground-plane with rectangular slots is an effective technique to mitigate the adverse effects of image current. RF waves impinging on the antenna's surface are reflected into free-space and some EM-waves penetrated through the gaps on the array into the substrate and are reflected at the ground-plane with a phase shift of π. The direct reflected and ground reflected EM-waves can interfere destructively to degrade the antenna properties. However, by using an on-chip antenna substrate of appropriate thickness constructive

Table 3
Average Antenna Gain Values for Different Cases.

On-chip antennas	Simulated gain (dBi)	Measured gain (dBi)
2 × 1 simple array	0.36	−0.72
2 × 1 on-chip array based on MTS	1.44	1.68
2 × 2 on-chip array based on MTS	3.84	3.36
2 × 2 on-chip array based on MTS-AMC	5.28	4.57
2 × 24 on-chip array based on MTS-AMC	22.10	20.36

Table 4
Average Radiation Efficiency Values for the Different Arrays.

On-chip antennas	Simulated eff. (%)	Measured eff. (%)
2 × 1 simple array	24.5	21
2 × 1 on-chip array based on MTS	35	53
2 × 2 on-chip array based on MTS	46	45
2 × 2 on-chip array based on MTS-AMC	53	53
2 × 24 on-chip array based on MTS-AMC	41	37.5

interference results when the direct and reflected EM-waves combine and thereby boosting the antenna's gain and efficiency performance [35]. The results presented in the next section confirm this result.

4. Proposed on-chip antenna designs

The antenna array based on square patches, shown in Fig. 1(a) was manufactured on the 35-μ m silicon dioxide substrate with a dielectric constant of$\varepsilon_r = 4$, resistivity of 10 Ω.cm, and tan$\delta = 0.001$. Characteristics of the antenna arrays were analyzed first using 3D full-wave electromagnetic simulation tool, namely CST Microwave Studio. The performance of the various array sizes is systematically discussed in this section.

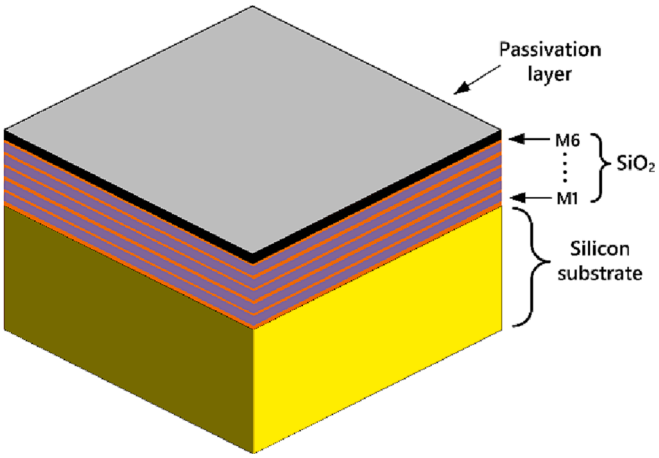


Fig. 5. Silicon based CMOS stack-up.

A) 2 × 1 On-Chip Antenna Array.

Fig. 1(a) shows a simple 2 × 1 on-chip antenna array comprising standard square patches. The measured reflection-coefficient results of this array in Fig. 2 show it to have $|S_{11}| \leq -10$ dB over 300–314 GHz. The average gain and radiation efficiency of this antenna measured, shown in Figs. 3 and 4, are −0.95 dBi and 21%, respectively.

B) 2 × 1 MTS-based On-Chip antenna array

The patch antennas of the 2 × 1 on-chip antenna array, shown in Fig. 1(b), are perforated with an arrangement of circular slots that transform the patch into an MTS structure. The dimensions and periodicity of the circular slots fabricated on the patch are of subwavelength at the frequency of operation. These characteristics define the metasurface and should not be confused with frequency selective surfaces where the periodicity of the unit-cells are of the order of λ/2 at the operating frequency and where the unit-cells are not of sub-wavelength dimensions [36,37]. The slots were optimized using CST Microwave Studio to realize the best radiation characteristics. Dimensions of the optimized on-chip antenna are given in Table I.

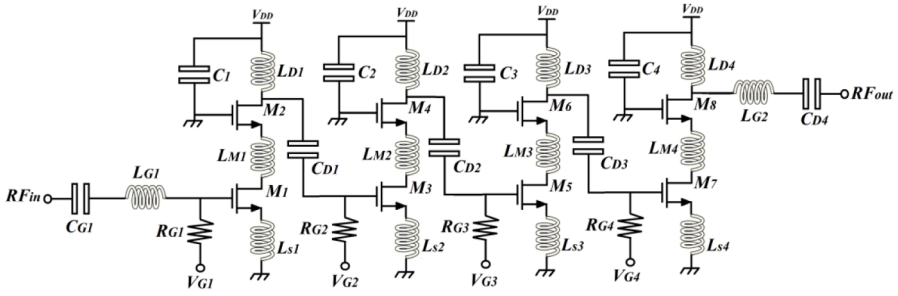
Figs. 2 through 4 show a comparison of the MTS array with the original 2 × 1 array. The array with MTS exhibits significantly improved results. Across 300 GHz to 314 GHz, the average measured reflection-coefficient (S_{11}) of the MTS array is −14 dB compared to −7.4 dB for the 2 × 1 original patch array, which is an improvement of 6.6 dB. Compared to the original 2 × 1 array, the MTS array shows improvement in the measured gain and radiation efficiency of 2.4 dBi and 32%, respectively. These results demonstrate the effectiveness of MTS to increase the effective aperture area of the antenna. With the proposed technique, the dimensions of the antenna array remain unaffected.

C) 2 × 2 MTS-based On-chip antenna array

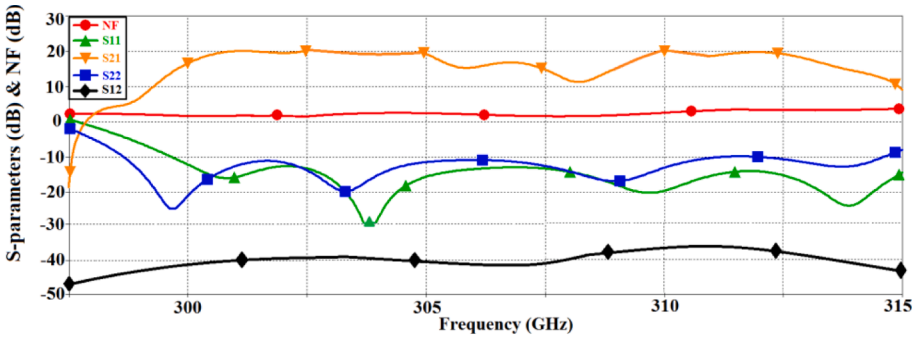
A 2 × 2 metasurface antenna array, which is shown in Fig. 1(c), was fabricated on the same substrate and footprint size as the 2 × 1 array. The dimensions of the four patches are identical. Dimensions of the other structural parameters are given in Table 1. Fig. 2 shows the 2 × 2 antenna operates across the same frequency range as the 2 × 1 array from 300 GHz to 314 GHz. Across this frequency range its average measured reflection-coefficient is better than −20 dB. Figs. 3 and 4 show

Table 5
Component Values of the 4-Stage THz LNA.

Parameters	Values
C_{G1}	110 *fF*
L_G	480 *pH*
R_{G1}, …,R_{G4}	20 *kΩ*
C_1, …,C_4	3.2 *pF*
L_{D1}, L_{D3}	280 *pH*
L_{D2}, L_{D4}	265 *pH*
L_{M1}, …,L_{M4}	58 *pH*
L_{s1}, …,L_{s4}	110 *pH*
C_{D1}, …,C_{D3}	42 *fF*
C_{D4}	39 *fF*



(a)



(b)

Fig. 6. (a) Schematic of the THz LNA integrated circuit, and (b) S-parameters and Noise Figure.

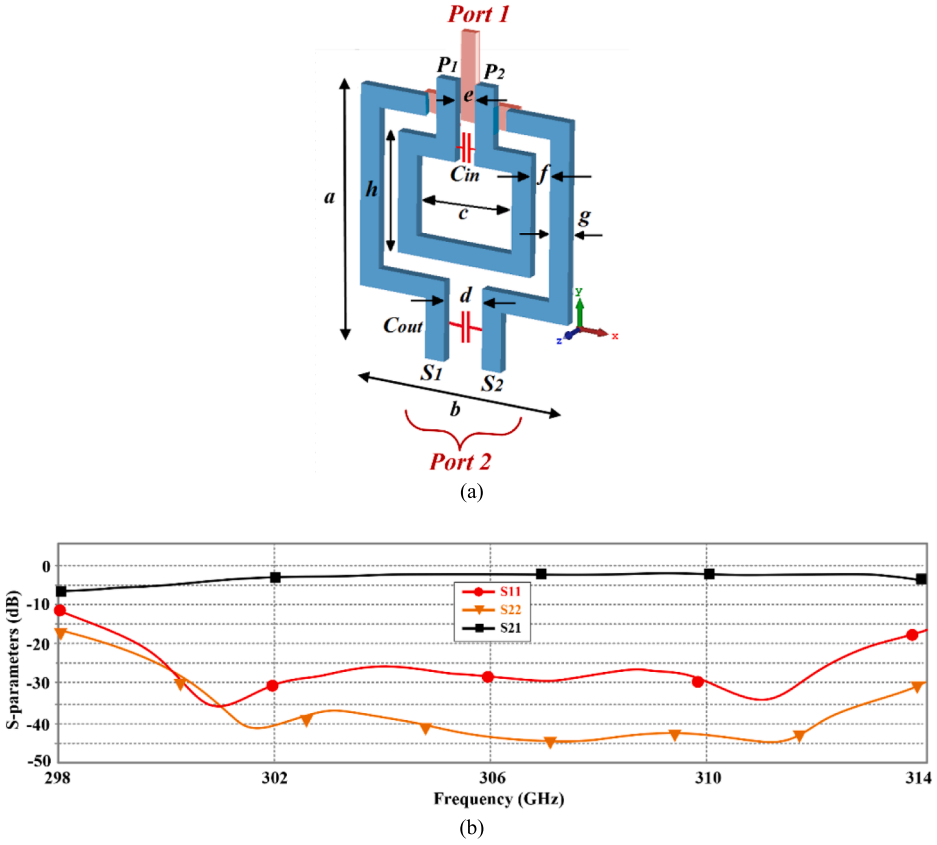


Fig. 7. (a) Model of the 0.31-THz on-chip balun, and (b) *S*-parameters ($Z_0 = 50\ \Omega$).

Table 6
Structural Prameters of the On-Chip Balun.

Parameter	*a*	*b*	*c*	*d*
Value (μm)	0.95	0.76	0.3	0.12
Parameter	*e*	*f*	*g*	*h*
Value (μm)	0.06	0.06	0.08	0.48
Parameter	*Cin*	*Cout*		
Value (fF)	120	300		

its average gain and radiation efficiency over this frequency span are 3.36 dBi and 45%, respectively.

D) 2 × 2 MTS-AMC based On-Chip Antenna Array with Ground-Plane Slots.

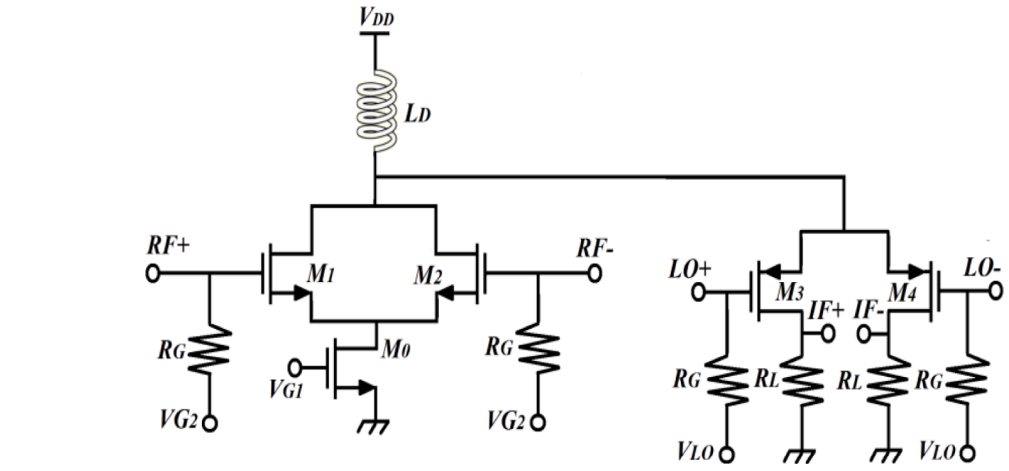
Miniaturization of antenna array requires reduction in the gap between the adjacent antenna elements. Unfortunately, this leads to strong unwanted mutual EM coupling between the elements that results in reduction in the antenna gain, operating bandwidth, and radiation efficiency. Mutual coupling was suppressed here by suppressing the surface currents interactions. This was achieved by inserting microstrip resonant elements between the radiating patches of the 2 × 2 MTS array, as shown in Fig. 1(d). Mutual coupling between the radiators due to current flow over the ground-plane was mitigated by defecting the ground-plane with rectangular slots. The slots were located under the resonant elements, as shown in Fig. 1(e). With this configuration a pseudo cavity is formed between the ground-plane and the partially conductive top layer to create an AMC structure. The impinging waves penetrate through the gap between the radiating elements and into the substrate layer where the waves undergo internal reflection and subsequently escape through the gaps on the top conductive layer, as illustrated in Fig. 1(f). The substrate thickness introduces phase shifts between the surface reflected waves and the ground reflected waves. Resonance condition is established when the phase difference is zero [25], i.e.,

$$\varphi_2 - \varphi_1 = 2\varphi_T - \frac{2\pi}{\lambda}2h - \pi = 2N\pi, \quad N = 0, 1, 2\cdots \tag{1}$$

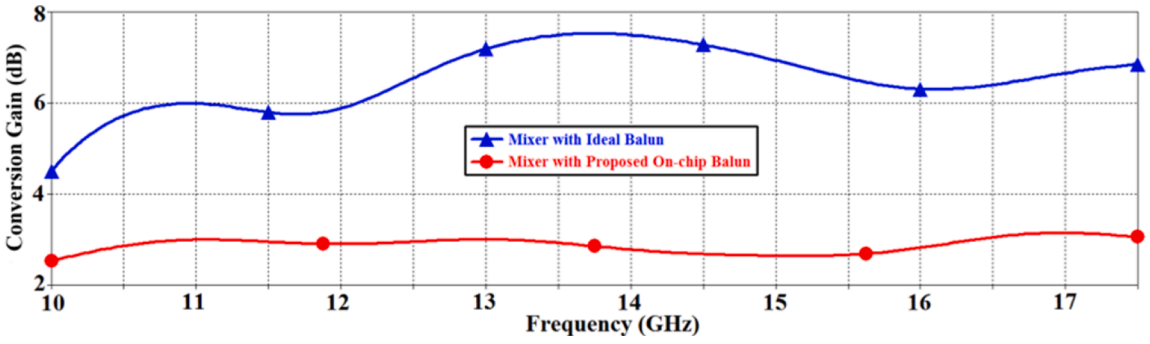
The structure then behaves like a perfect magnetic conductor (at normal incidence) since it reflects normal incident waves with zero phase shift. In this study the zero phase shift is established at the center frequency of the antenna's operational band. Fig. 1(g) shows the surface current density over the 2 × 2 on-chip MTS antenna array with no AMC ground-plane and no microstrip resonant elements between the patches. The figure shows the instant in time when the two antennas nearest the input feedline are excited. It is evident the surface current couples with the other two patches farthest away from the input port. Fig. 1(h) shows the surface current density over the 2 × 2 on-chip MTS antenna array with AMC ground-plane and decoupling microstrip resonant elements. It is evident from this the decoupling elements significantly suppress the surface currents interacting with the other patches. Fig. 1(i) shows the phase response at the input port of the 2 × 2 on-chip MTS antenna array with decoupling elements and ground-plane slots. It is evident in Figs. 2 to 4 the MTS array with decouping elements and ground-plane slots can significantly improve the reflection-coefficient measured to be better than −24 dB, achieve gain of 4.57 dBi, and efficiency of 53% across 0.3 THz to 0.314 THz. Compared to the 2 × 2 MTS array, this is an improvement in gain of 1.15 dBi and efficiency of 8%.

E) 2 × 24 Element MTS-AMC On-Chip Antenna Array.

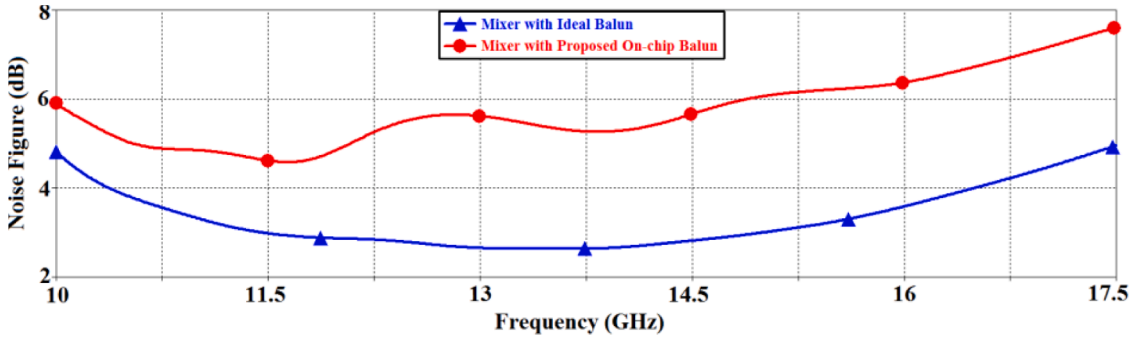
In practice the size of the array is limited by the available on-chip



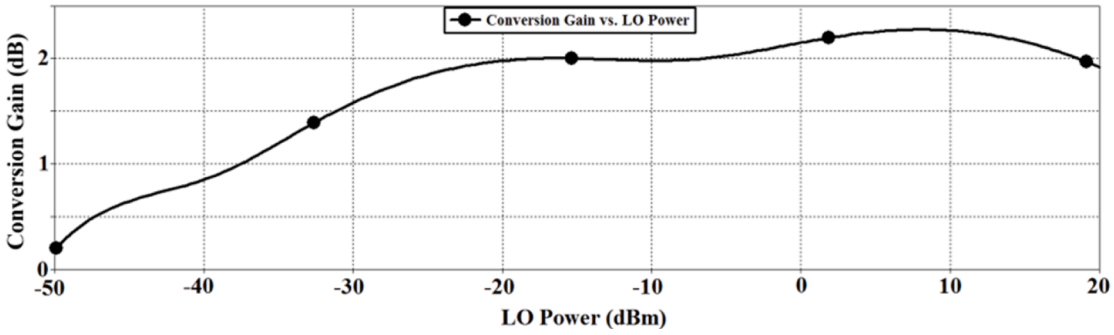
(a)



(b)



(c)



(d)

Fig. 8. (a) Schematic of the folded Gilbert-cell mixer fabricated using 40-nm CMOS technology, (b) conversion gain, (c) NF of the interstage-matched mixer, and (d) conversion gain of mixer with balun as a function of LO power.

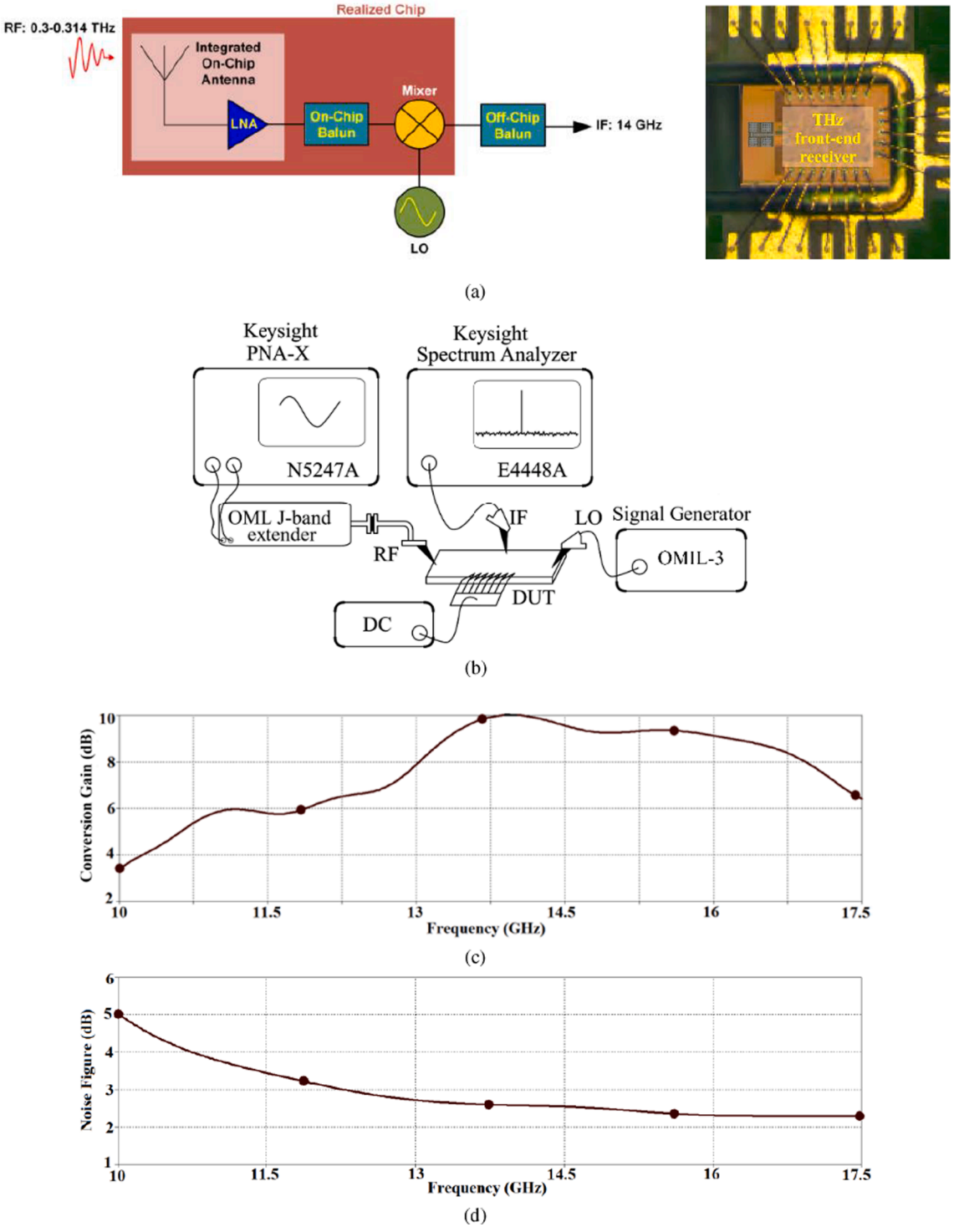


Fig. 9. (a) The proposed CMOS based 0.31-THz front-end receiver with an integrated on-chip antenna, (b) measurement set-up for the RF front-end receiver excluding the integrated antenna, (c) receiver conversion gain excluding the integrated antenna, and (d) receiver NF excluding the integrated antenna.

area. A 2 × 24 linear array of MTS-AMC was designed and fabricated purely for experimental purposes. Its layout and fabrication are shown in Fig. 1(j), and its ground-plane in Fig. 1(k). From Figs. 2 to 4 it is evident from the measured results the antenna has an average reflection-coefficient that is better than −31 dB, gain and radiation efficiency of 20.36 dBi and 37.5%, respectively, across 0.3 to 0.314 THz. For comparison purposes, the results of the on-chip antenna's salient parameters are given in Tables 2 to 4.

5. Simulation Based Model of a THz Front-End Receiver Integrated With the Proposed On-Chip Antenna

In this section, the active components constituting the front-end of a 0.31 THz receiver were first individually modelled and then integrated with the proposed antenna for the purpose of proof of concept. The 2 × 2 MTM-AMC antenna array was fabricated on the same CMOS chip as the front-end receiver. The 40-nm CMOS stack process of TSMS consisted of several SiO_2 layers interleaved with metal layers (M1-M6), as illustrated

Table 7
Performance of the THz Integrated Antenna.

Module	Performance
On-chip Antenna (2 × 2 MTS-AMC)	Gain: 5.10 dBi BW: 300–314 GHz
Low Noise Amplifier	Average gain: 17 dB BW: 300–315 GHz Noise Figure < 3 dB Input Power (1 dB): 30 dBm
On-Chip Balun (transformer)	Average insertion-loss: 3 dB
Mixer	Ave. conversion gain: 2.8 dB Average noise figure: 5.5 dB RF-IF isolation > 50 dB LO-IF isolation > 45 dB Total Chain Gain: 25 dB (Mixer de-embedded)
Receiver (On-chip Antenna + THz front-end)	Total average chain gain: 7.5 dB (Mixer embedded) Average noise figure < 3 dB Input Power (1 dB): −30 dBm Power Consumption: 12.6 dBm

in Fig. 5. The antenna was fabricated on the top metal layer. The metal layers under the antenna structure were filled with SiO_2. Metal layer M1 on the silicon substrate was used as the ground plane.

A. THz Low-Noise Amplifier.

The low-noise amplifier (LNA) in the THz on-chip receiver was modelled using the 40-nm CMOS process of TSMC's IC foundry. A cascode topology was chosen for this design as it offers an improved gain and isolation over a common emitter amplifier (CEA). A four-stage cascode configuration was realized, as shown in Fig. 6(a), to boost the amplifier gain. By sharing the bias current in the cascade arrangement, the overall efficiency of the amplifier can be improved. Interstage matching was necessary to optimize the power transfer. In fact, each load inductor L_D and decoupling capacitor C_D has been selected to provide conjugate matching between the adjacent amplifier stages. Intrastage inductors (L_m) were tuned to convert the source impedance to the maximum noise impedance [38]. The input/output impedance of the LNA is 50-Ω. DC power supply, bias voltage and ground-lines are distributed through a dense grid made of wide metal layers to reduce the effects of parasitic inductances/resistances, and to optimize parasitic capacitances. This was done to enhance the stability of the DC power to the circuit as well as shield the components.

LNA components values used are given in Table 5. The measured S-parameters and NF of the LNA are shown in Fig. 6(b). This LNA has a gain $|S_{21}|$ greater than 10 dB over a frequency range from 300 GHz to 315 GHz with a peak gain of 20 dB. Its input/output reflection-coefficients (i.e., $|S_{11}|$ and $|S_{22}|$) are better than −10 dB. NF of the amplifier is less than 3 dB over its operating frequency range. The power consumed by the amplifier is 8.2 mW from a supply voltage V_{DD} of 1.2 V. The LNA was integrated in the receiver and conjugately impedance matched to the proposed on-chip antenna.

B. Interstage Transformer.

Transformers implemented using planar geometry are unable to fully confine the magnetic field within the device. The finite resistivity experienced by the unconfined magnetic field in the substrate causes magnetic losses. In addition, ohmic loss results from thin metallization and parasitic loss due to the conducting coil of the transformer and substrate. However, due to the challenges in integrating three-dimensional structures (e.g., solenoid) in the standard CMOS process technologies, planar transformers are the preferred solutions. This is because they are easy to fabricate owing to their simple geometry and compatibility with CMOS foundry processes.

The simulation model of the on-chip transformer, shown in Fig. 7(a), transforms the signal from the LNA to a differential input to the mixer without needing a matching circuit. The transformer interleaves the primary (P_1 & P_2) and secondary (S_1 & S_2) coils to establish impedance transformation from single to differential with an enhancement in DC isolation and bandwidth. The geometry of the transformer was optimized with the 3D full-wave EM solver by CST Microwave Studio. The transformer has a footprint of 1.1 × 1.4 mm^2. The optimized structural parameters of the on-chip transformer are given in Table 6. Capacitors at the input/output were used for matching purposes. The values of C_{in} and

Table 8
Comparison of the Proposed On-Chip Antenna With Others Reported in Literature.

Refs.	Antenna Type	Frequency Band (GHz)	Gain (dBi)	Efficiency (%)	Resistivity (Ω.cm)	Process Technology
[39]	Bowtie-slot	90–105	Max. −1.78	–	50	0.13-μm BiCMOS
[40]	Differential-fed circularly polarized	50–70	Max. −3.2	–	50	0.18-μm
[41]	Ring-shaped monopole	50–70	Max. 0.02	Max. 35	12.5	CMOS 0.18-μm
[42]	Circular open-loop	57–67	Max. −4.4	–	–	CMOS 0.18-μm
[43]	Loop antenna	65–69	Max. 8	Max. 96.7	1000	CMOS 0.18-μm
[44]	AMC squared slot	15–66	Max. 2	–	–	CMOS 0.09-μm
[45]	Monopole	45–70	Max. 4.9	–	10	Silicon CMOS
[46]	Dipole antenna	95–102	Max. 4.8	–	10	Bi-CMOS
[47]	Tab monopole	45–75	Max. 0.1	Max. 42	10	Silicon CMOS
[48]	Transmitter/receiver modules	218–246	Ave. 8.5	–	–	130-nm SiGe HBT
[49]	MTM – DR	>450	Max. 4.5	Max. 45.7	10	Standard CMOS
[50]	Monopole antenna	~300	Max. 1.7	–	–	InP 50-μm
[51]	Patch Fed DRA	330–355	Max. 7.9	Max. 74	–	0.18-μm SiGe
[52]	On-chip 3D (Yagi concept)	320–360	Max. 10	Max. 80	10	0.13-μm SiGe
[53]	Half-Mode Cavity Fed DRA	125–140	Max. 7.5	Max. 46	–	0.18-μm CMOS
[54]	Slot Fed Stacked DRA	125–135	Max. 4.7	Max. 43	–	0.18-μm CMOS
[55]	DRA	120–140	Max. 2.7	Max. 43	–	0.18-μm CMOS
This work	2 × 1 MTS	300–314	Ave. 1.52 Max. 3.3	Ave. 21 Max. 37	10	Silicon layer
This work	2 × 2 MTS	300–314	Ave. 3.7 Max. 4.1	Ave. 45 Max. 47.7	10	Silicon layer
This work	2 × 2 MTS-AMC	300–314	Ave. 4.58 Max. 6.16	Ave. 53 Max. 56.9	10	Silicon layer
This work	2 × 24 MTS-AMC	300–314	Ave. 20.36 Max. 20.6	Ave. 37.5 Max. 41.7	10	Silicon layer

C_{out} are 120 fF and 300 fF, respectively. The *S*-parameters of the transformer in Fig. 7(b) show that its insertion-loss varies between −7 dB and −2 dB over the operating frequency band from 300 GHz to 314 GHz.

C. Down-Converting Mixer.

The equivalent model of the symmetrical Gilbert-cell mixer, shown in Fig. 8(a), was used here to reduce the phase/amplitude imbalance in the differential RF input signal, and to mitigate the common-mode noise. This mixer employs balanced transconductance stages M_1 and M_2, and two switching transistors M_3 and M_4. The voltage V_{G1} at the base of transistor M_0 is used to activate and deactivate the mixer. The input RF stage is based on source-coupled pair of transistors M_1 and M_2. The output current of the transconductance stage via inductance L_D that acts as a choke forcing the RF signal of M_1 and M_2 to fold into the source terminals of the p-channel transistors M_3 and M_4. The inductance and Q-factor of the inductor are 250 pH and 20 pH, respectively. The mixer uses inductance L_D to balance the RF transconductor and to direct the RF signal to the switching transistors. The LO signal is applied to the gates of M_3 and M_4, which act as switches and convert the signal frequency to IF of 14 GHz. The load resistors R_L convert the output IF current to voltage. The load resistors drop the DC voltage; however, this has negligible effect on the function of the mixer. This is because the mixer transistors function in the switching mode that require a low DC voltage across their drain–source terminals. The component values of the mixer are $L_D = 240$ pH and $R_L = 700\ \Omega$. The mixer design was modelled using the 40-nm CMOS technology. By down-converting the THz signal to the microwave band allows the on-chip antenna to be tested easily with no need for specialized equipment.

The measured conversion gain and NF performance of the mixer for interstage matching conditions with an ideal and the proposed balun are shown in Fig. 8(b) and (c), respectively. With an ideal balun, the mixer exhibits as expected a high conversion gain that varies between 4.5 dB and 7.7 dB. However, the conversion gain of the mixer with the on-chip balun in Fig. 8(b) varies between 2.6 dB and 3.2 dB. The conversion gain in both cases is positive and maintained in the IF operating frequency range. The NF of the mixer with the ideal balun shown in Fig. 8(c) varies from 2.7 dB to 5 dB, and for the non-ideal case varies between 4.7 dB and 7.7 dB. We can reduce the noise by using an amplifier with higher gain. Fig. 8(d) shows the optimum conversion gain possible of the mixer with the proposed balun. The gain of 2.3 dB is obtained when driven by a LO with RF signal power of around 8 dBm.

D. Performance of the THz Receiver with On-Chip Antenna.

Block diagram of the RF front-end receiver with the on-chip antenna in Fig. 9(a) was modelled using the 40-nm CMOS technology by TSMC. Fig. 9(b) shows the setup used to measure the front-end receiver excluding the antenna. LO signal generator is OMIL-03 Terahertz series that has a built-in IMPATT source and frequency reference synthesizer. A 20 dB attenuator is recommended with the LO to regulate the power. The RF signal from Keysight PNA-X N5247A can be extended to the required frequency band with an OML J-band VNA extender. The Keysight spectrum analyzer E4448A can be used to measure the IF signal. To accurately determine the power from the receiver it's necessary to subtract the losses introduced by the probe and cables. The results show that at the input frequency of 0.314 THz, the receiver's conversion gain in Fig. 9(c) varies from 3.5 dB to 10 dB. The peak conversion gain is at 14 GHz. NF in Fig. 9(d) varies from 2.3 dB to 5 dB. At 14 GHz NF is 2.5 dB. The performance parameters of the THz front-end receiver are shown in Table 7.

6. Discussion

The performance of the proposed MTS-AMC based on-chip antenna array is compared in Table 8 with other mm-Wave and THz antennas reported in the literature. The 2 × 24 MTM-AMC array exhibits gain and radiation efficiency comparable to other arrays cited in the table. However, unlike other on-chip antennas, which are multi-layered structures requiring complex fabrication processes, the proposed technique has the advantage of being less complex as it can be fabricated on the single layer of silicon. This makes it cost-effective, especially for mass production. As expected, the experimental 2 × 24 array exhibits significantly higher average gain of 20.36 dBi but this is at the expense of the radiation efficiency of 37.5%. Also, its large footprint is prohibitive for on-chip applications. The main purpose of this experimental study was to demonstrate the effectiveness of combining MTS and AMC in the implementation of on-chip antennas.

7. Conclusions

In this work, we have demonstrated for the first time the effectiveness of combining the MTS and AMC technologies to enhance the performance of THz on-chip antennas in terms of impedance matching, gain and radiation efficiency. This was achieved without compromising the antenna's footprint. The MTS property was achieved by incorporating periodic array of subwavelength circular dielectric slots on the patch antennas. The AMC surface was realized by using an appropriate substrate thickness so that the directly radiated and ground-plane reflected electromagnetic-waves interfere constructively. Moreover, the isolation between the adjacent radiators was mitigated by suppressing the surface currents. This was accomplished by inserting microstrip resonant structures between the radiating patches and by defecting the ground-plane with rectangular slots. Several antenna arrays of different matrix sizes were fabricated on silicon substrate and their performance measured. For experimental purposes the 2 × 2 antenna array based on MTS-AMC technologies was integrated with a THz on-chip receiver that was designed to operate between 0.3 and 0.314 THz. Measured results show that the proposed on-chip antenna is a viable alternative for on-chip integration in mm-Wave and THz RF front-end transceivers of wireless devices.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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Declaration

All of the figures, materials, and data within the manuscript are original and owned by authors.

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