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Modelling and simulation of Zener diode noise in the time domain

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Abstract

This paper presents a new time domain Zener diode compact model for transient noise simulation. SPICE2 and SPIC3 use piece-wise linear time dependent sources for generating complex waveforms. This approach is not practical when applied to randomly generated noise. Today, through on-going improvements to freely available circuit simulation tools, SPICE noise generation has moved to a new level. Ngspice, for example, computes white Gaussian noise 'on-the-fly' as transient simulation progresses. The proposed model has a simple behavioural structure that supports time domain shot, flicker, and thermal noise. The physical properties of the proposed model are introduced in the second section. This is followed by an evaluation of model performance in the third and fourth sections, including static d.c, dynamic charge, and transient noise characterisation. Finally, the fifth section summarises the conclusions of the research.

KEYWORDS

compact device modelling, flicker and thermal noise, Ngspice, shot, transient simulation, Verilog-A, Zener diode

1 | INTRODUCTION

The SPICE[1,2] diode model is a core element in Zener and avalanche breakdown diode modelling. It has a number of limitations however, including poor reverse bias leakage current accuracy, a common series resistance for both the high current forward and reverse bias regions of operation, limited control of the slope of the Zener or avalanche breakdown regions and no mechanism for setting temperature variation of the Zener or avalanche breakdown voltage. Since the SPICE Zener diode model was first released a series of publications have reported improvements to its simulated d.c. characteristics. In 1981 Laha and Smart[3] introduced a breakdown mechanism modelled as the sum of exponential terms. This extension was added to the original SPICE 2 diode model. To ensure numerical stability a new limiting algorithm was implemented and merged with the SPICE simulator code. The 1988 paper by Piotrowski[4] reported a reverse diode model that improved modelling of low leakage currents. Piotrowski also added a series resistance in the Zener or avalanche breakdown regions improving model performance at high diode currents. Of particular interest is the paper by Deveney[5] that presents a temperature dependent macro-model for Zener and avalanche diodes. For a high percentage of the Zener diode applications at d.c. or low frequency analogue signal processing, for example, voltage stabilisers and wave shaping circuits, the improved Zener diode models have acceptable functionality and accuracy. Moreover, it

is common practice for device manufacturers to characterise SPICE models for their products. There is at least one application area where the existing Zener diode models are inappropriate. This is time domain noise simulation. Early versions of SPICE did not implement a simple method for time domain noise generation but relied on piece-wise linear sources for complex signal waveform construction. Such an approach is not very practical for noise because it is very inflexible and potentially error prone. Today this situation has changed through on-going improvements to freely available circuit simulation tools, including Ngspice,[6] Xyce,[7] and Qucs-S.[8] These tools support time domain noise generation as a transient simulation progresses. The omission of a simple method for time domain noise generation was a serious limitation because Zener diodes are often a central component in the design of low cost noise generator circuits for test equipment, particularly analogue dithering signal generation for A/D dynamic range analysis, spectrum analyser calibration, and communications receiver performance testing under fading and EMI conditions. Zener diode transient noise simulation adds an important tool to the available circuit design and analysis repertoire. This paper presents a new Zener diode compact model that accounts for frequency band limited shot and flicker noise, and resister thermal noise in the time domain. In addition, it also simulates more accurately dynamic stored charge in the reverse and forward bias regions of device operation. The physical properties of the proposed model are introduced in Section 2. The final part of this section provides details of a SPICE behavioural subcircuit based on the physical attributes of the proposed compact model. This has a simple structure and is mainly built from equation-defined components that allow a high degree of design flexibility. An evaluation of the proposed Zener diode model performance is outlined in Sections 3 and 4, including static d.c. dynamic charge, and transient domain noise characterisation. The model performance evaluation is centred on the properties of a typical 3.9 volt Zener diode with a 'soft' current/voltage characteristic in the reverse bias region. Finally, Section 5 summarises the main conclusion of this research.

2 | A ZENER DIODE COMPACT MODEL FOR TRANSIENT AND TIME DOMAIN NOISE SIMULATION

The schematic symbol and non-linear equivalent circuit for the proposed Zener diode model are drawn in Figure 1. The model consists of three parallel electrical networks. These represent (1) the forward biased device, (2) the reverse biased device, and (3) Zener effects. In Figure 1 the three networks, inside dotted boxes, f, r and z, are connected at the diode anode and cathode terminals, Pa and Pk, implying that terminal currents are the sum of the three branch currents. Moreover, outside their designated region of bias operation the f, r and z circuits continue to be active but do not contribute significantly to device current. The model equivalent circuit is implemented with nonlinear equation defined current sources, nonlinear capacitors and resistors, rather than the mixture of diodes, voltage sources and passive components found in SPICE macro-models. The behavioural modelling approach is particularly important because it simplifies model conversion from SPICE to Verilog-A or Modelica, and other hardware description languages. The new model also implements time domain thermal, shot and flicker noise. Sources of noise are indicated in Figure 1 by the shaded RMS current generator symbols. For devices with *Vzener* less than roughly five volts the Zener effect dominates. Zener diodes are normally characterised by negative *Vzener* temperature coefficients. Avalanche breakdown is the dominant mechanism in higher voltage Zener diodes. Such devices are often characterised by positive *Vzener* temperature coefficients.

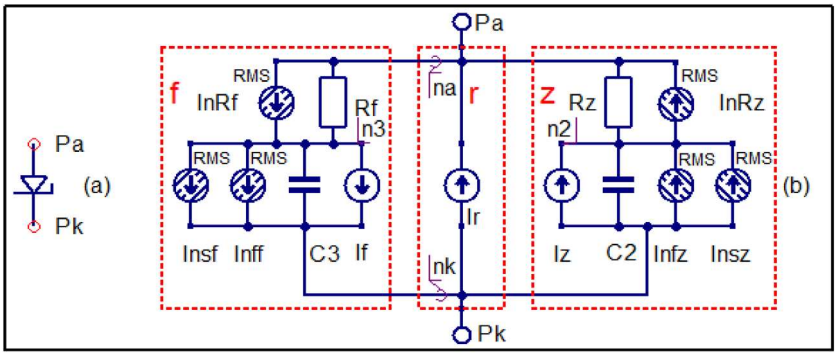

FIGURE 1 Zener diode compact device model: (A) schematic symbol, (B) non-linear equivalent circuit.

2.1 | The non-linear d.c. model

The d.c characteristics of the Zener diode model are determined by *Rf*, *If*, *Ir*, *Rz* and *Iz*. These are given by Equations (1)–(5)

$$IRf = \frac{v(na,n3)}{RfInt} \tag{1}$$

$$If = IsfT2 \cdot \left(\exp\left(\frac{V(n3,nk)}{Nf \cdot VTH}\right) - 1.0\right) \tag{2}$$

$$Ir = IsrT2 \cdot \left(\exp\left(\frac{V(nk,na)}{Nr \cdot VTH}\right) - 1.0\right) \tag{3}$$

$$IRz = \frac{v(n2,na)}{RzInt} \tag{4}$$

$$Iz = IszT2 \cdot \left(\exp\left(\frac{-[V(nk,n2) + VzenerInt]}{Nz \cdot VTH}\right) - 1.0\right) \tag{5}$$

where *V* (*nxxx*, *nyyy*) is the voltage between nodes nxxx and nyyy. Variables *RfInt*, *IsfT*2, *VTH*, *RzInt*, *IszInt* and *VzenerInt* are defined in Figure 2. The remaining undefined quantities are either intermediate equations, numerical constants or parameters. Model equations and constants are listed in Figure 2, where *P_Q* is the Verilog-A name for the charge of an electron and *P_K* is the Verilog-A name for Boltzmann's constant. Model parameters are listed in Table 1. The non-linear d.c. model has similar functionality to Zener diode macro-models. However, its structure is simpler. One notable difference is the inclusion of the Zener diode knee voltage *VzenerInt* in Equation (5) rather than being implemented as a separate independent voltage source in branch z. This reduces the number of internal model nodes by one, slightly improving computational efficiency.

2.2 | The transient dynamic charge model

The dynamic charge characteristics of the proposed Zener diode model are determined by the properties of capacitors *C*2 and *C*3. These are defined by currents *IC*2 and *IC*3 given by Equations (6) and (7), where $ICx = \frac{d}{dt}(Qx)$ and *Qx* is the charge stored by capacitor *x*. *C*3 models both depletion and diffusion capacitance from roughly—*Vzener* volts to the forward bias region of operation. *C*2 adds an additional capacitance in the Zener or avalanche regions of operation. As a first approximation *C*2 dynamic charge, *QC*2, is set to be proportional to the diode d.c. current. Depletion and forward bias diffusion capacitances are modelled with non-linear equation-defined charge, *QC*3. Separate transit time parameters *Tt* and *Ttz* provide an additional degree of freedom when fitting simulation output data to device capacitance measurements.

$$IC2 = \frac{d}{dt}\{QC2\} = \frac{d}{dt}\{(Ttz \cdot Ir) + (Ttz \cdot Iz)\} \tag{6}$$

$$\begin{aligned} IC3 = {} & \frac{d}{dt}\{QC3\} = (Fcp > V(n2,nk)) \\ & ? \frac{d}{dt}\left\{\left(Cj0 \cdot \frac{VjT2}{1-M}\right) \cdot \left(1 - \left[1 - \frac{V(n2,nk)}{VjT2}\right]^{1-M}\right) + Tt.Iz\right\} \\ & : \frac{d}{dt}\left\{Cj0 \cdot \left[F1 + \frac{1}{F2} \cdot \left(F3 \cdot (V(n2,nk) - Fcp) + \frac{M}{2 \cdot Vj} \cdot \{V(n2,nk) \cdot V(n2,nk) - Fcp \cdot Fcp\}\right)\right] + Tt \cdot If\right\} \end{aligned} \tag{7}$$

where undefined variables and constants are given in Figure 2 or listed in Table 1.

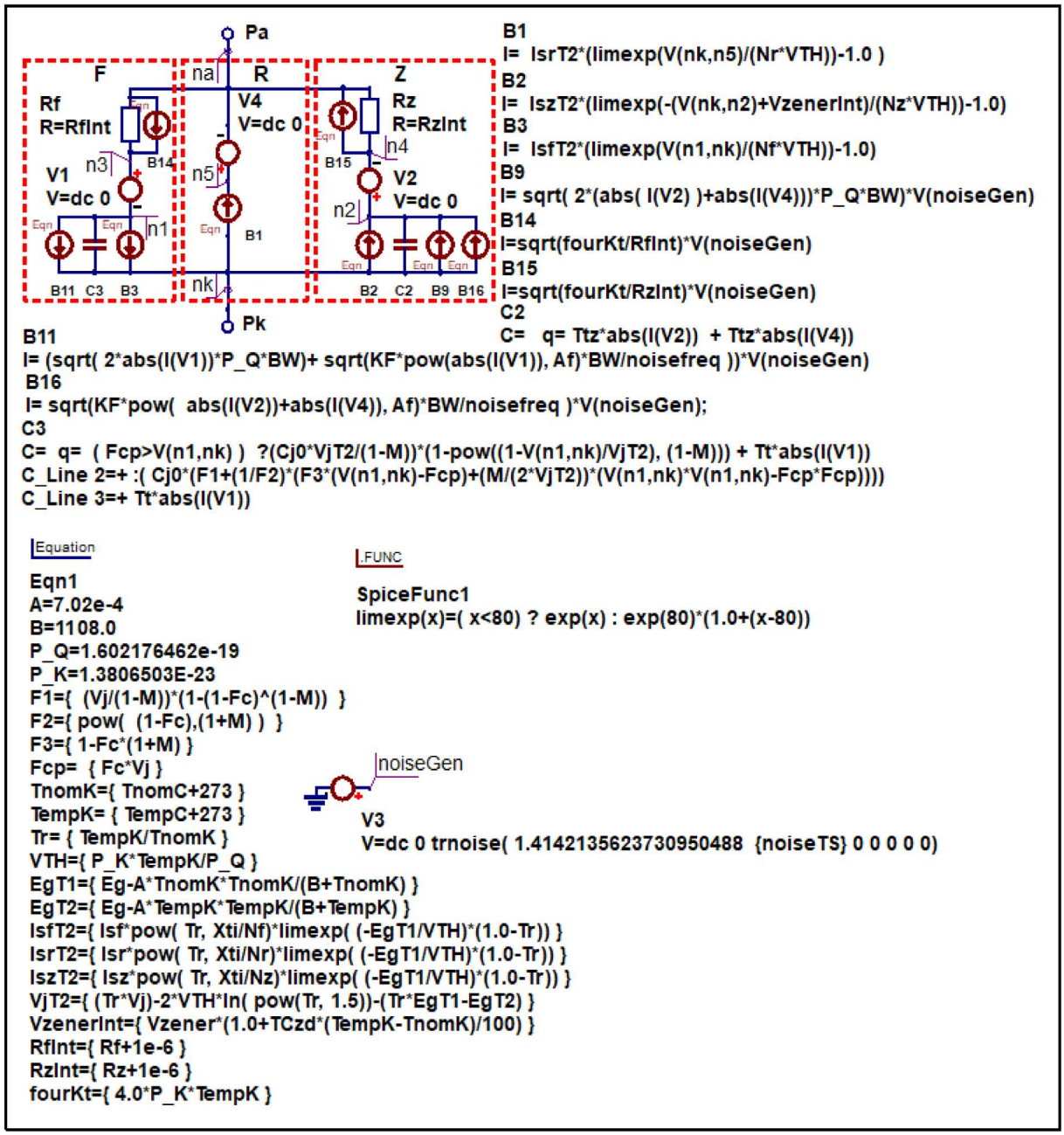

FIGURE 2 Qucs-S/Ngspice Zener diode behavioural model: subcircuit schematic drawing; intermediate equations and limexp function definition.

2.3 | The transient noise model

Shot, flicker and resistive thermal noise are observed in Zener diodes.[9–11] The time domain transient noise characteristics of the Zener diode compact model are determined by the properties of current noise sources *Insz*, *Infz*, *Insf*, *Inff*, *InRz* and *InRf*. These are represented by the RMS values given by Equations (8)–(13)

$$Insz = \sqrt{2 \cdot (Iz + Ir) \cdot P\_K \cdot BW} \tag{8}$$

$$Infz = \sqrt{KF \cdot (Iz + Ir)^{Af} \cdot \frac{BW}{\text{noisefrequency}}} \tag{9}$$

TABLE 1 Zener diode parameters.

Name	Description	Unit	Default
Nf	Forward bias emission coefficient		1.1
Isf	Forward bias saturation current	A	6.6e-15
Nr	Reverse bias emission coefficient		10.3
Isr	Reverse bias saturation current	A	1.02e-9
Nz	Zener/avalanche region emission coefficient		0.8
Isz	Zener/avalanche region saturation current	A	2.97e-13
Eg	Band gap	eV	1.11 for Si
Xti	Isf, Isr, Isz temperature coefficient		3.0
M	Grading coefficient		0.488
Fc	Coefficient for depletion capacitance		0.995
Vj	Junction potential	V	0.675
Cj0	Zero bias junction capacitance	F	176e-12
Tt	Forward bias transit time	s	8.13e-9
Ttz	Zener/avalanche region transit time	s	8.13e-9
Rf	Forward bias series resistance	Ω	0.001
Rz	Zener/avalanche region series resistance	Ω	0.001
Vzener	Zener diode voltage at TempC	V	3.9
noiseTS	Noise generator break point time step	s	200e-6
Tczd	Zener diode temperature coefficient	%	−0.09
BW	Noise band width	Hz	1e6
Af	Flicker noise exponent		1
Kf	Flicker nose coefficient		3.2043e-18
noiseFreq	Flicker noise simulation frequency	Hz	100
TnomC	Parameter measurement temperature	Celsius	27
TempC	Device temperature	Celsius	27

$$Insf = \sqrt{2 \cdot |If| \cdot P\_K \cdot BW} \tag{10}$$

$$Inff = \sqrt{KF \cdot |If|^{Af} \cdot \frac{BW}{\text{noisefrequency}}} \tag{11}$$

$$InRf = \sqrt{\frac{fourKt \cdot BW}{RfInt}} \tag{12}$$

$$InRz = \sqrt{\frac{fourKt \cdot BW}{RzInt}} \tag{13}$$

where undefined variables and constants are given in Figure 2 or listed in Table 1.

2.4 | Building a Zener diode SPICE behavioural model

The schematic of a Qucs-S/Ngspice behavioural subcircuit for the proposed Zener diode model is presented in Figure 2. This has a similar structure to the compact model in Figure 1. Equations (1)–(13) are implemented with equation-

defined B current sources, non-linear charge defined capacitors and resistors. Voltage sources $V1$, $V2$ and $V4$ act as current probes in the f, r and z circuit branches. The Ngspice subcircuit netlist is listed in Appendix A.

3 | EVALUATION OF THE PROPOSED ZENER DIODE COMPACT MODEL

3.1 | Static d.c. characteristics

The test circuit drawn in Figure 3 introduces a simple analogue test bench for simulating Zener diode d.c. characteristics and comparing output data with device measurements. The comparison technique employed is essentially an overlay process where simulated data is plotted on top of measured data and the model parameters varied, by parameter 'tuning' or optimization, to give a best 'fit' between the two data sets[12]; in the forward bias region ($Vzdz \geq 0.4$ V) parameters Nf, Isf and Rf, in the reverse bias region (Vzd from roughly 0.4 V to $-Vzener$) parameters Nr, Isr, and in the Zener region, ($Vzd \leq -Vzener$), parameters Nz, Isz and Rz. At high diode d.c currents Rf and Rz act as current limiting components in the forward and reverse bias regions, respectively. At low diode currents Rf and Rz have little effect on d.c. performance. In this study Rf and Rz are both set at a 1 m Ω nominal value.

3.2 | Dynamic charge characteristics

Capacitance modelling in conventional Zener diode macro-models is normally restricted to depletion capacitance. This is not surprising because a high proportion of Zener diode applications are at d.c. or low signal frequencies where capacitance plays a minimum role. At RF, or indeed where fast switching transients need to be investigated, the effects caused by capacitance are likely to strongly influence simulation accuracy. Compared to conventional Zener diode macro-models the proposed Zener diode model includes two additional capacitance contributions; the first is forward bias diffusion capacitance and the second a reverse bias Zener capacitance. The plot of measured capacitance in Figure 4 suggests that capacitance increases with increasing diode current in the Zener effect region. $C3$ accounts for forward bias diffusion and depletion capacitance. $C2$ accounts for the extra capacitance in the Zener region of operation. To demonstrate the advantages that equation-defined behavioural compact modelling offers the proposed Zener

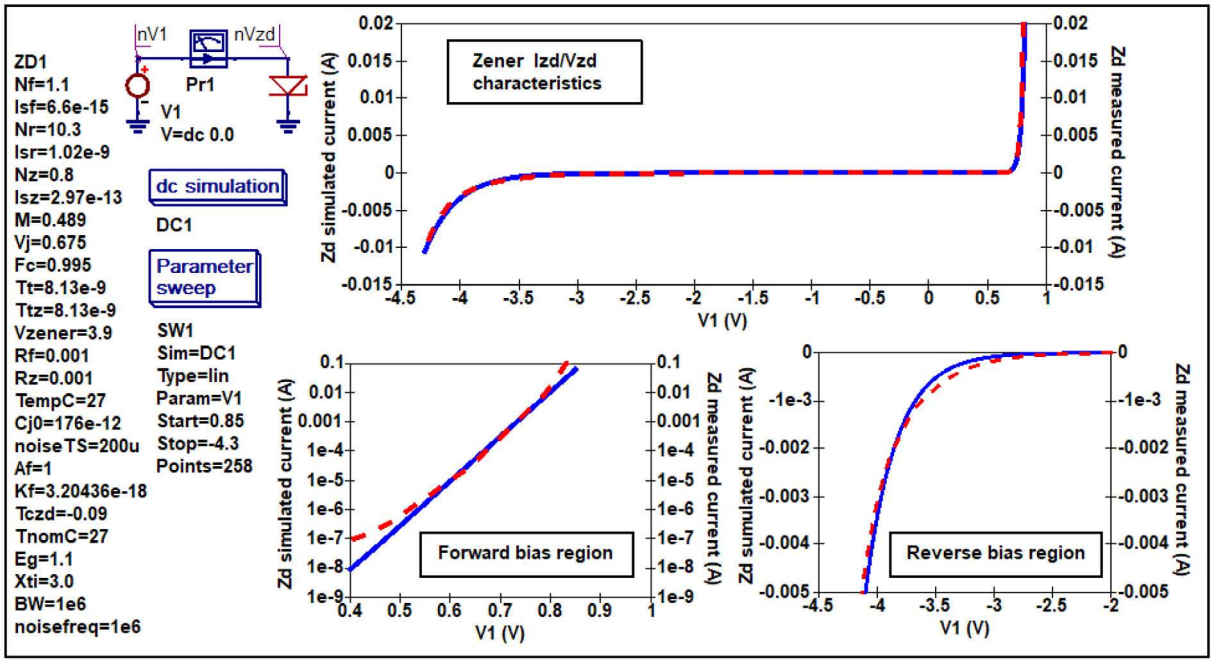

FIGURE 3 Qucs-S/Ngspice Zener diode d.c. test bench: simulated data; solid lines, measured data; dashed curves. Zener diode model parameters: default set listed in Table 1.

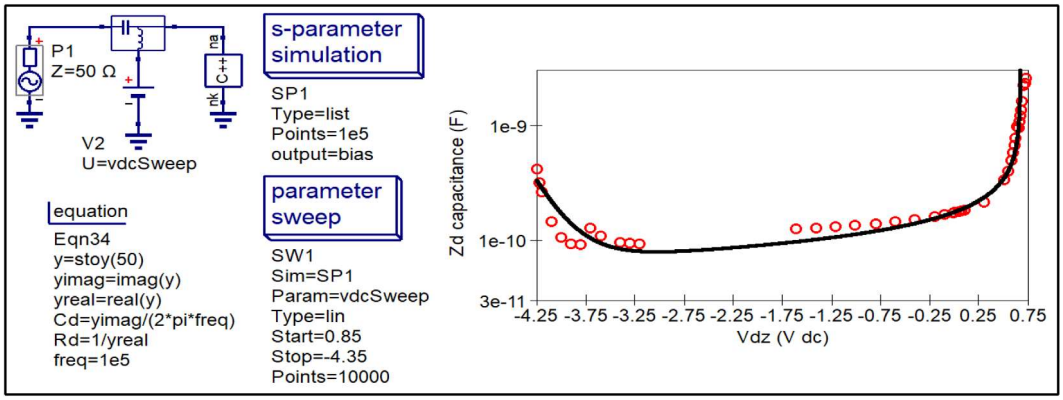

FIGURE 4 Zener diode capacitance test bench: simulated data; solid line, measured date; circles. Zener diode model parameters: default set listed in Table 1.

diode model has been translated to a Verilog-A module, compiled to C++, and its capacitive characteristics extracted from Y-parameters obtained with QucsStudio S-parameter simulation. The Verilog-A module code is listed in Appendix B. In most instances the Ngspice statements listed in Appendix A translate directly to their equivalent Verilog-A module[13] code. However, there are two exceptions; firstly time domain noise features are not currently implemented in Verilog-A and secondly SPICE voltage sources *V*1, *V*2 and *V*4, that act as current probes, are replaced by resisters *RfInt*, *RzInt* and *RS*, again acting as current sensing elements.

3.3 | Transient domain noise characteristics

Recent releases of the open source circuit simulator Ngspice include voltage and current sources that generate white Gaussian noise. These sources output noise constructed by a random number data stream processed by the Box Muller transform.[14] The sequence of generated values has random amplitude, but equidistant time intervals of width *noisTS*. Adding time domain noise to model components injects random fluctuating signals on top of d.c. voltages and currents. Figure 2 illustrates how time domain noise is implemented. Independent voltage source *V*3 outputs noise voltage *V* (*noiseGen*) with a 1 V RMS amplitude. Multiplying *Isnz*, *Infz*, *Insf*, *Inff*, *InRf* and *InRz* by *VnoiseGen* sets subcircuit current sources *B*9, *B*16, *B*11, *B*14 and *B*15 to the required frequency band limited shot and flicker noise, and thermal noise values. Placing time domain noise sources inside a model subcircuit minimises correlation between sources if more than one Zener diode is present in a transient simulation.

3.3.1 | Time domain noise calibration

The transient noise calibration test bench shown in Figure 5 illustrates how shot and flicker noise can be generated with the Ngspice *trnoise* noise source. In this study the initial purpose of the calibration test bench was to confirm the accuracy of simulated noise data prior to adding noise sources to the proposed compact model. In Figure 5 *trnoise* current source *I*1 generates noise voltage V (nG) across the 1 Ω load resistor. This voltage is probed by *Vprobe*2, outputting noise signals *V* (*ngen*) and RMS voltage *V* (*nrmsgen*). The *V* (*ngen*) and *V* (*nrmsgen*) waveforms are plotted against time in Figure 5. Probe *Vprobe* has been designed to remove the d.c. component from the differential input signal and to estimate the RMS value of the remaining noise. As time moves forward RMS voltage *V* (*nrmsgen*) converges to a steady state value (Figure C1; Appendix C) outlines the design of probe *Vprobe*. Noise voltage *V* (*nG*) has a Gaussian white noise spectrum with a value of 1 V RMS. Non-linear controlled current generator *B*1 generates frequency band limited shot and flicker noise. Probe *Vprobe*1 extracts the combined shot and flicker noise signal and its RMS value. By varying *Idc* and *noiseFreq* a calibration chart for the randomly generated noise can be constructed. Figure 6 illustrates this chart for *BW* = 1e6 Hz, a *noisefrequency* range of 1 Hz to 1e5 Hz, and a d.c. current range of 1–10 mA. Strong agreement between the theoretically calculated noise and the corresponding simulated data is supported by Figure 6, confirming the accuracy of the Ngspice generated time domain noise. Flicker noise is both a function of bias current and frequency.

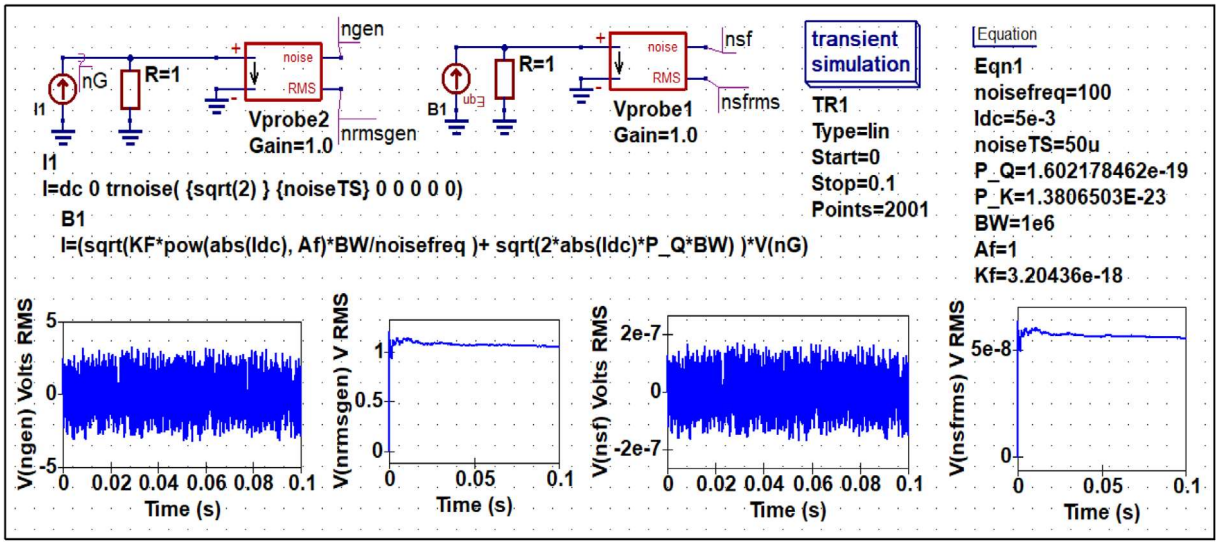

FIGURE 5 Transient noise calibration test bench with simulated noise waveforms and extracted RMS voltage curves.

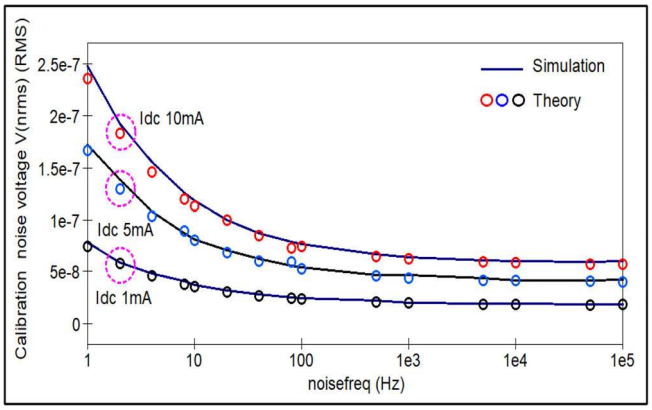

FIGURE 6 Ngspice noise calibration chart: Idc = 1, 5 and 10 mA, BW = 1e6 Hz, Af = 1 and Kf = 3.20436e-18.

At high frequencies flicker noise falls and shot noise normally becomes the dominant noise component. At low frequencies the reverse is true. At a given frequency flicker and shot noise have equal RMS values. This occurs at frequency *fseqf*, where

$$fseqf = \frac{Kf \cdot Idc^{(Af-1)}}{2 \cdot P\_Q} \tag{14}$$

For the case where *Af* is 1, this becomes

$$fseqf = \frac{Kf}{2 \cdot P\_Q} \tag{15}$$

The test example has *Kf* = 3.20436e-18, giving *fseqf* = 10 Hz. Hence, once parameter *Kf* is given a specific value, frequency *fseqf* is also fixed. However, the value of parameter *noisefrequency* attached to the model symbol, see Figure 3, is entirely under the control of 'users'. At high frequencies shot noise is normally the dominant noise component and the value chosen for *noisefrequency* is not likely to be critical. The reverse is true for low frequencies. As a first

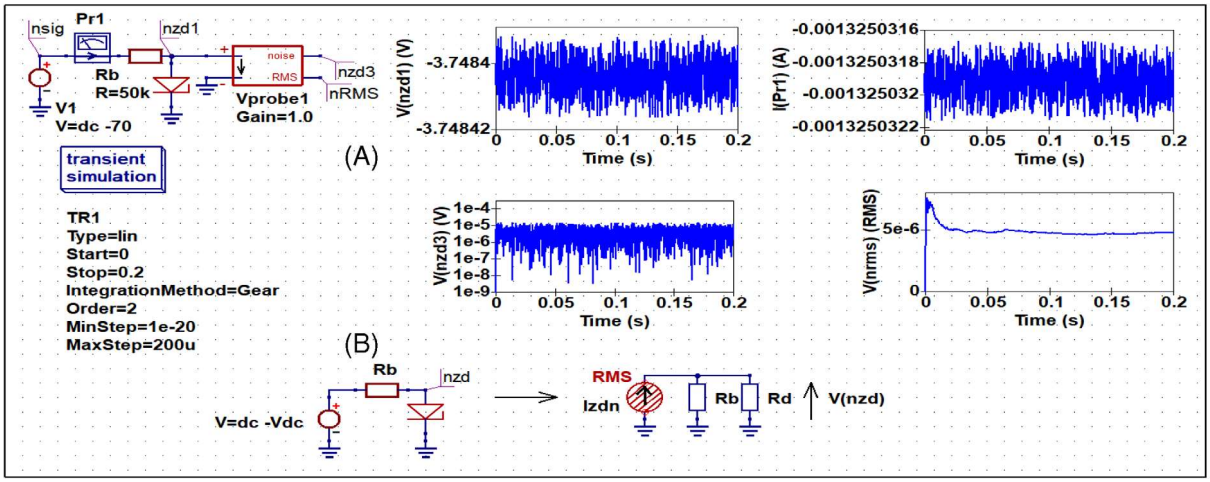

FIGURE 7 Zener diode transient simulation: (A) test bench and output data waveforms, (B) low frequency noise equivalent circuit. Zener diode model parameters: default set listed in Table 1.

approximation setting *noisefrequency* to a value near the start of the simulation frequency band width, should give acceptable flicker noise accuracy.

3.3.2 | Zener diode shot and flicker noise in the time domain

The noise plots shown in Figure 7A are typical for a Zener diode reversed biased with resistor Rb in series with d.c. voltage source $V1$. Waveforms $V\,(nzd1)$ and $I(Pr1)$ plotted against time clearly illustrate noise added to the d.c. bias signals Izd $= -1.325$ mA and Vzd $= -3.748$ V. The lower plots display noise voltage $V\,(nzd3)$ and its RMS value $V\,(nRMS)$. The test conditions correspond to a region on the reverse bias device characteristics where the Zener effect controls diode current. Figure 8 illustrates two sets of plots for (A) Zener diode noise voltage ($V\,(nRMS)$) against *noisefrequency* and (B) diode resistance Rd against d.c. bias voltage. Analysis of the low frequency noise equivalent circuit drawn in Figure 10B gives, to a first approximation, a value for the RMS noise voltage $V\,(nrms)$ as

$$V(nrms) = Izdn \cdot \frac{Rd}{1+\frac{Rd}{Rb}} \tag{16}$$

where Rd is the Zener diode resistance at a specified d.c. bias and

$$Izdn = \sqrt{2 \cdot |Izd| \cdot P\_K \cdot BW} + \sqrt{KF \cdot |Izd|^{Af} \cdot \frac{BW}{\text{noisefrequency}}} \tag{17}$$

Equation (16) indicates that when $Rb \gg Rd$

$$V(nrms) = Izdn \cdot Rd \tag{18}$$

Under practical bias conditions resistor Rd would normally be a few kilohms maximum and $V1$ no more than 10 or 20 V. However, to impose the condition $Rb \gg Rd$ the value of Rb must be set at a value much greater than a few kilohms and $V1$ increased to set the d.c. bias current. An estimate of the value of Rd can be found from the simulated values of $V\,(nrms)$, using

$$Rd = \frac{Rdm}{1 - \frac{Rdm}{Rd}} \tag{19}$$

$$Rdm = \frac{V(nrms)}{Izdn} \tag{20}$$

The graphs drawn in Figure 8 are particularly interesting because they highlight the bias condition for maximises noise generation. Although shot and flicker current noise RMS values are proportional to d.c. current, *Rd* decreases with increasing d.c. bias current. Hence, noise voltage output is highest when $Izdn \cdot Rd$ has its largest value. In the test example this occurs at voltages slightly higher than $-Vzener$, at around -3.7 V, at the onset of the Zener effect. For bias voltages greater than roughly -3.5 V the Zener effect ceases and the diode current drops to reverse bias leakage levels, reducing shot and flicker noise to a low value. The component models distributed with the SPICE circuit simulator were not designed for transient noise simulation. Essentially, in the time domain, they are noise free passive and active devices. However, during transient noise simulation they continue to function normally. Figure 9 shows a second test example where the Zener diode under test is connected as a load in the collector circuit of a pnp BJT. As the collector output resistance is very high this test circuit meets the required condition set by Equation (14), maximising output voltage noise generation. In this test circuit Zener diode d.c. bias current is set by the value of resistor *R*1.

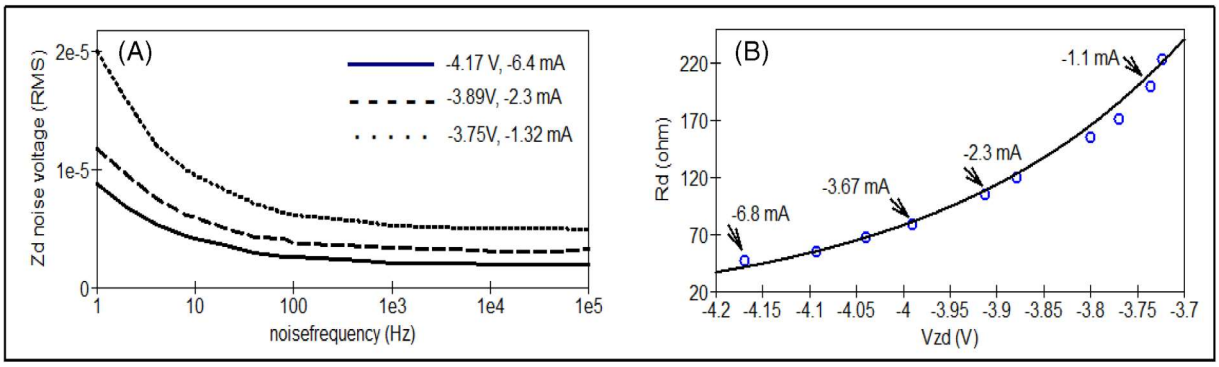

FIGURE 8 Zener effect bias region noise simulation: (A) RMS noise voltage plotted against *noisefrequency* for three bias points; (B) Zener diode resistance Rd plotted against bias voltage: data extracted from simulated Zener noise voltages, circles; data from Verilog-A S-parameter simulation Figure 4; solid line. Zener diode model parameters: default set listed in Table 1.

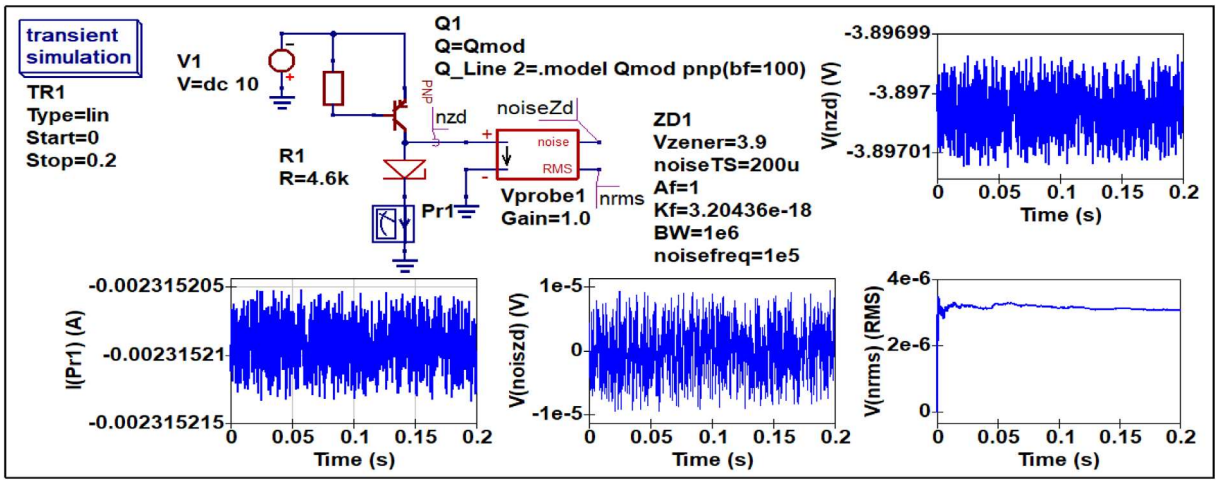

FIGURE 9 An alternative Zener diode transient simulation test bench that automatically satisfies the condition $Rb \gg Rd$ for maximising noise generation: d.c. bias conditions $Vzd = -3.9$ V and $Izd = -2.23$ mA.

4 | MODEL PERFORMANCE

Three of the most important metrics for estimating compact model performance are function, accuracy and simulation speed. This paper provides a solution to the problem of simulating Zener diode noise in the time domain while retaining the best d.c. features of existing Zener models. The proposed model is different to the classic SPICE single diode model, and the classic SPICE two diode subcircuit, in that it comprises an equation-defined subcircuit and its equivalent Verilog-A module. The compact model schematic drawn in Figure 2 suggests a more complex model than the classic SPICE models. However, to some extent this impression is influenced by the algebraic equations listed in the body of the compact model, for example, If the noise generators *B9*, *B16*, *B15*, *B11*, *B14* and *V3* are removed the compact model becomes very similar in size to the classic SPICE models. Three other schematic features are worth commenting on; firstly voltage generators *V1*, *V2* and *V4* are dummy current sensing components and play no part in physical modelling other than detecting current flow, secondly non-linear capacitor *C*1 adds diffusion capacitance in the reverse bias region of device operation, improving the accuracy of the transient response, and thirdly controlled generator *B1*, Figure 2, improves the accuracy of the reverse diode current, particularly in the d.c. bias region near to the nominal Zener voltage. This improvement is clearly shown in Figure 10, which suggests that the single diode SPICE model implements abrupt avalanche breakdown, the two diode subcircuit model has a better Izd/Vzd fit in the nominal Zener voltage region, whereas the proposed compact model predicts more accurately the softer *Izd/Vzd* d.c. characteristic observed with low voltage Zener effect devices. The Zener diode Izd/Vzd characteristic also confirm that the three models have d.c. bias values of −3.9 V at −2.36 mA. This agrees with the measured Zener data introduced in Figure 3.

The new compact model is an important innovation because it allows time domain noise to be investigated in circuits where a knowledge of noise effects are essential for accurate and reliable circuit design, for example, in low frequency noise generator analysis, noise propagation during power supply turn-on and noise levels in low noise circuits. Unfortunately, transient simulation of noise is a highly computational intensive process that implies long simulation times. In many instances however, a circuit may only include a small number of critical Zener diodes whose noise is a factor in circuit or system design. Moreover, non-critical Zener diodes can often be modelled with the Verilog-A module, which does not implement time domain noise, significantly reducing circuit transient simulation times. Since the adoption of the Verilog-A hardware description language[13] as an international modelling standard it has become the de-facto 'state-of-the-art' tool for simulation model development and model interchange between circuit simulators. As Verilog-A modules are compiled to C++ code and linked to a circuit simulator, their performance often approaches that achieved by hand crafted C++ device models. The test circuits shown in Figures 10 and 11 indicate the Verilog-A version of the new compact Zener diode by the symbol marked with C++. Close inspection of the Verilog-A code listed in Appendix B identifies a strong link between behavioural equation-defined modelling and Verilog-A variable

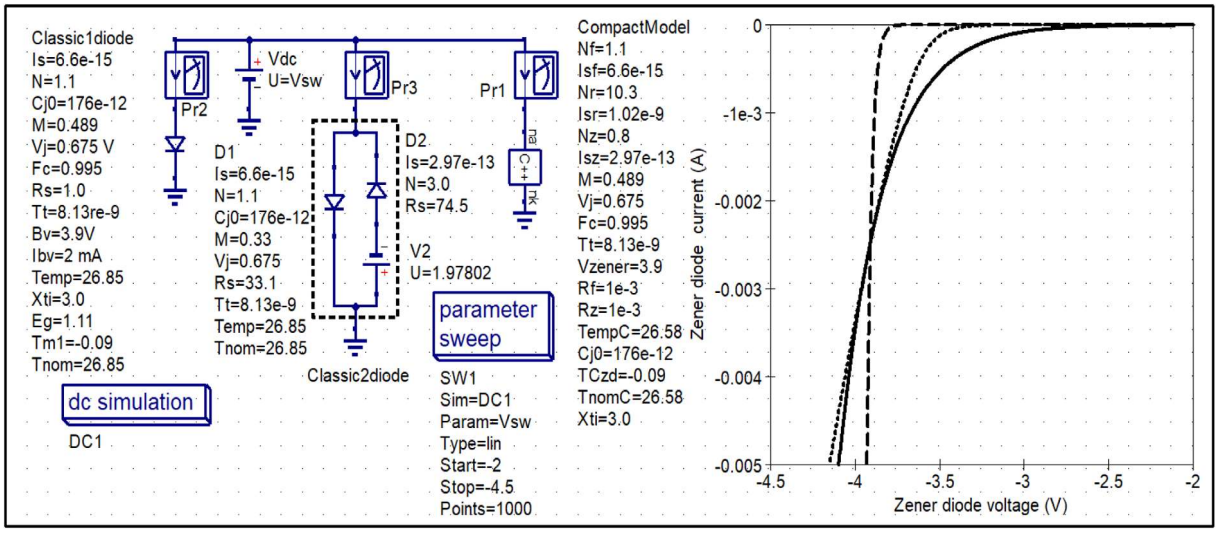

FIGURE 10 A 3.9 volt Zener diode d.c. test bench for comparing Zener diode models: (A) solid line—Verilog-A compact model; (B) dashed line—SPICE classic one diode model; (C) dotted line—SPICE two diode subcircuit.

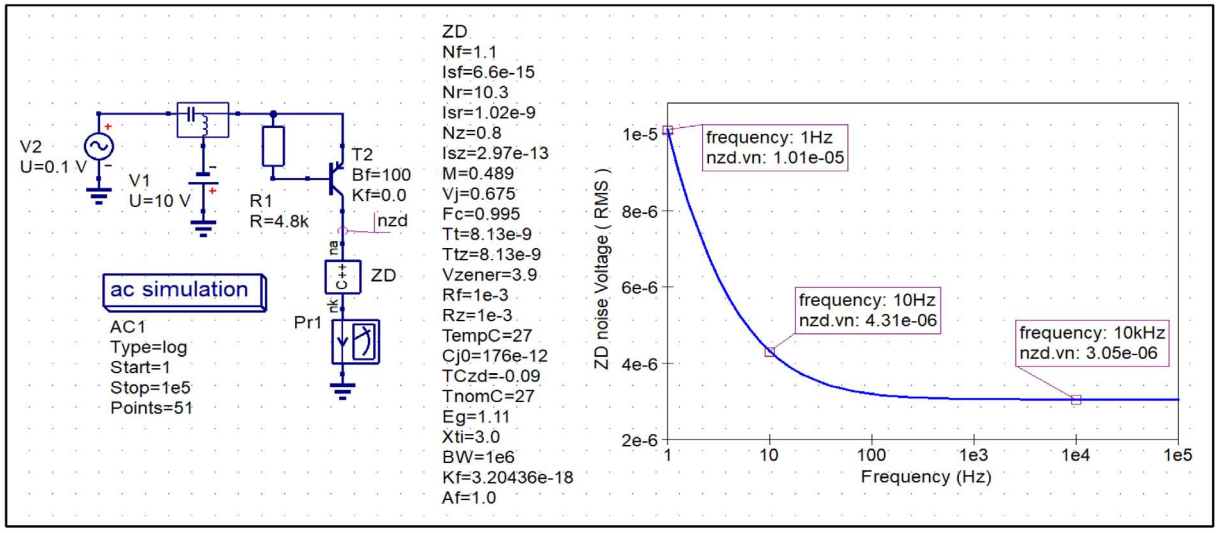

FIGURE 11 A Zener diode small signal AC noise test bench where the device under test *ZD* is the Verilog-A module listed in Appendix B and the RMS noise voltage plot is for d.c. bias conditions $Vzd = -3.89$ V and $Izd = -2.22$ mA.

assignment and current contribution statements, making synthesis of Verilog-A code from equation-defined subcircuit schematics a relatively straight forward process.

QucsStudio[15] Verilog-A supports shot and flicker noise as small signal a.c. frequency domain signals. To provide a cross check as to the accuracy of the transient simulation noise model, a.c. shot and flicker noise have been added to the Verilog-A version of the proposed compact Zener diode model, see Appendix B. Figure 11 introduces a small a.c. version of the transient noise test bench given in Figure 9, alongside a plot of the simulated Zener RMS noise voltage against frequency. In this test example BJT *T2* has parameter $Kf = 0.0$, effectively removing its flicker noise. The Verilog-A Zener noise model clearly gives good agreement with the time domain noise data reported in previous sections, providing a high degree of confidence in the transient simulation model accuracy.

The simulation speed of the new Zener model is best understood by considering model performance in the time domain where it is inherently a computationally intensive process with timing largely dependent on model parameter *noiseTS* and the transient simulation finish time *stop*. Decreasing parameter *noiseTS* computes a more detailed noise waveform but also increases the simulation run time. Transient noise simulation generates large amounts of output data and making parameter *noiseTS* very small becomes problematic on computers with limited RAM. Hence, a compromise between waveform detail and simulation times has to be made for each specific circuit under test. The type and complexity of individual Zener models also has an effect on simulation speed, for example, the SPICE single diode model has a lower simulation overhead than the SPICE two diode subcircuit. Even though the C++ compiled Verilog-A module is more complex than the SPICE classic Zener models, simulation tests without transient noise, suggest it simulates slightly faster than the SPICE single diode model and over twice as fast as the classic SPICE two diode subcircuit. These estimates are in line with the fact that the SPICE two diode subcircuit requires two diode models to be processed each time it is called during simulation. Moreover, the Verilog-A module is compiled to high speed C++ code which minimises model overhead.

5 | CONCLUSIONS

The Zener diode compact model introduced in this paper adds time domain noise simulation to the well-established small signal a.c noise features implemented in SPICE. The omission of a white noise generator from early versions of SPICE was a serious limitation, particularly because Zener diodes are often a central component in the design of low cost noise generators for test equipment and analogue RF applications. Today, this situation has changed through the on-going improvements in freely available circuit simulators. This paper introduces the physical attributes of the

proposed model and demonstrates its application in the testing of a low voltage, 'soft' current/voltage characteristic, Zener diode, The model structure is designed to support equation-defined behavioural model implementation that accounts for frequency band limited shot and flicker noise, and resistive thermal noise. White Gaussian noise generation is continually updated 'on-the-fly' as transient simulation progresses. Model evaluation tests indicate that maximum noise output occurs at bias conditions close to *Vzener* The proposed model is easily translated to Verilog-A, or indeed other similar hardware description languages. The simulation performance of the proposed model has been compared with measured and theoretical data. Good correlation was observed between simulation, theory and measurement. With its significantly improved performance the Verilog-A compact model is a strong candidate for use in d. c, a.c. and transient circuit simulation that excludes time domain noise. Similarly, the equation-defined compact model offers a new relatively simple solution for those situations where time domain Zener diode noise characterisation is an essential factor in accurate circuit performance analysis or electronic system design.

DATA AVAILABILITY STATEMENT

Data sharing not applicable to this article as no datasets were generated or analysed during the current study.

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APPENDIX A

NGSPICE ZENER DIODE SUBCIRCUIT CODE

```
* Qucs-S 0.0.24 ZDnoise.sch
.SUBCKT ZDRnoise na nk Nf=1.1 Isf=6.6e-15 Nr=10.3 Isr=1.02e-9 Nz=0.8 Isz=2.97e-13 M=0.489
+ Vj=0.675 Fc=0.995 Tt=8.13e-9 Ttz=8.13e-9 Vzener=3.9 Rf=0.001 Rz=0.001 TempC=27
+ Cj0=176e-12 noiseTS=200u Af=1 Kf=3.20436e-18 Tczd=-0.09 TnomC=27 Eg=1.1 Xti=3.0
+ BW=1e6 noisefreq=1e6
.FUNC limexp(x) = ( x
.PARAM A=7.02e-4
.PARAM B=1108.0
.PARAM P_Q=1.602176462e-19
.PARAM P_K=1.3806503E-23
.PARAM F1={(Vj/(1-M))*(1-(1-Fc)^(1-M))}
.PARAM F2={pow((1-Fc),(1+M))}
.PARAM F3={1-Fc*(1+M)}
.PARAM Fcp={Fc*Vj}
.PARAM TnomK={TnomC+273}
.PARAM TempK={TempC+273}
.PARAM Tr={TempK/TnomK}
.PARAM VTH={P_K*TempK/P_Q}
.PARAM EgT1={Eg-A*TnomK*TnomK/(B+TnomK)}
.PARAM EgT2={Eg-A*TempK*TempK/(B+TempK)}
.PARAM IsfT2={Isf*pow(Tr,Xti/Nf)*limexp((-EgT1/VTH)*(1.0-Tr))}
.PARAM IsrT2={Isr*pow(Tr,Xti/Nr)*limexp((-EgT1/VTH)*(1.0-Tr))}
.PARAM IszT2={Isz*pow(Tr,Xti/Nz)*limexp((-EgT1/VTH)*(1.0-Tr))}
.PARAM VjT2={(Tr*Vj)-2*VTH*ln(pow(Tr,1.5))-(Tr*EgT1-EgT2)}
.PARAM VzenerInt={Vzener*(1.0+TCzd*(TempK-TnomK)/100)}
.PARAM RfInt={Rf+1e-6}
.PARAM RzInt={Rz+1e-6}
.PARAM fourKt={4.0*P_K*TempK}
V1 n3 n1 dc 0
V2 n2 n4 dc 0
Rf n3 na {RFINT}
Rz n4 na {RZINT}
B3 n1 nk I = IsfT2*(limexp(V(n1,nk)/(Nf*VTH))-1.0)
B1 nk n5 I = IsrT2*(limexp(V(nk,n5)/(Nr*VTH))-1.0 )
B2 nk n2 I = IszT2*(limexp(-(V(nk,n2)+VzenerInt)/(Nz*VTH))-1.0)
V4 n5 na dc 0
C3 n1 nk q= ( Fcp>V(n1,nk) ) ?(Cj0*VjT2/(1-M))*(1-pow((1-V(n1,nk)/VjT2), (1-M))) + Tt*abs(I(V1))
+ :( Cj0*(F1+(1/F2)*(F3*(V(n1,nk)-Fcp)+(M/(2*VjT2))*(V(n1,nk)*V(n1,nk)-Fcp*Fcp))))
+ Tt*abs(I(V1))
C2 n2 nk q= Ttz*abs(I(V2)) + Ttz*abs(I(V4))
B14 na n3 I = sqrt(fourKt/RfInt)*V(noiseGen)
B15 n4 na I = sqrt(fourKt/RzInt)*V(noiseGen)
V3 noiseGen 0 dc 0 trnoise( 1.4142135623730950488 {noiseTS} 0 0 0 0 0)
B9 nk n2 I = sqrt( 2*(abs( I(V2) )+abs(I(V4)))*P_Q*BW)*V(noiseGen)
B16 nk n2 I = sqrt(KF*pow( abs(I(V2))+abs(I(V4)), Af)*BW/noisefreq )*V(noiseGen);
B11 n1 nk I = (sqrt( 2*abs(I(V1))*P_Q*BW)+ sqrt(KF*pow(abs(I(V1)), Af)*BW/noisefreq ))*V(noiseGen)
.ENDS
```

APPENDIX B

VERILOG-A ZENER DIODE MODULE

```
`include "disciplines.vams"
`include "constants.vams"
module ZDnoise(nk, na);
inout nk, na;
electrical n1, nk, na, n2, n5;
parameter real Nf=1.1; parameter real Isf=6.6e-15; parameter real Nr=10.3;
parameter real Isr=1.02e-9; parameter real Nz=0.8; parameter real Isz=2.97e-13;
parameter real M=0.489; parameter real Vj=0.675; parameter real Fc=0.995;
parameter real Tt=8.13e-9; parameter real Ttz=8.13e-9; parameter real Vzener=3.9;
parameter real Rf=1e-3; parameter real Rz=1e-3; parameter real TempC=27;
parameter real Cj0=176e-12; parameter real TCzd=-0.09; parameter real TnomC=27;
parameter real Eg=1.11; parameter real Xti=3.0; parameter real BW=1e6;
parameter real Kf=3.20436e-18; parameter real Af=1.0;
real A, B, P_Q, P_K, F1, F2, F3, Fcp, TnomK, TempK, Tr, Izd, Ifd, VzenerInt;
real VTH, EgT1, EgT2, IsfT2, IsrT2, IszT2, VjT2, RzInt, RfInt, Rs, fourKt;
analog begin
  A=7.02e-4; B=1108.0; P_Q=1.602176462e-19; P_K=1.3806503E-23;
  F1=(Vj/(1-M))*(1-pow(1-Fc,(1-M))); F2=pow((1-Fc),(1+M)); F3=1-Fc*(1+M); Fcp=Fc*Vj;
  TnomK=TnomC+273; TempK=TempC+273; Tr=TempK/TnomK; VTH=P_K*TempK/P_Q;
  EgT1=Eg-A*TnomK*TnomK/(B+TnomK); EgT2=Eg-A*TempK*TempK/(B+TempK);
  IsfT2=Isf*pow(Tr,Xti/Nf)*limexp((-EgT1/VTH)*(1.0-Tr));
  IsrT2=Isr*pow(Tr,Xti/Nr)*limexp((-EgT1/VTH)*(1.0-Tr));
  IszT2=Isz*pow(Tr,Xti/Nz)*limexp((-EgT1/VTH)*(1.0-Tr));
  VjT2=(Tr*Vj)-2*VTH*ln(pow(Tr,1.5))-(Tr*EgT1-EgT2);
  RzInt=Rz+1e-8; RfInt=Rf+1e-8; Rs=0.01;
  fourKt=4.0*P_K*TempK; VzenerInt= Vzener*(1.0+TCzd*(TempK-TnomK)/100);
  Izd = abs( V(n2,na)/RzInt) + abs(V(n5,na)/Rs ); Ifd = abs( V(na, n1)/RfInt);
  I(n1,nk) <+  IsfT2*(limexp(V(n1,nk)/(Nf*VTH))-1.0) ;
  I(nk,n5) <+  IsrT2*(limexp(V(nk,n5)/(Nr*VTH))-1.0 );
  I(n5,na) <+  V(n5,na)/Rs; I(n2,na)
  I(n2,na) <+  white_noise(fourKt/RzInt, "white");
  I(nk,n2) <+  IszT2*(limexp(-(V(nk,n2)+VzenerInt)/(Nz*VTH))-1.0);
  I(nk,n2) <+  white_noise(2.0*P_Q*Izd*BW,"white");
  I(nk, n2) <+  flicker_noise(Kf*pow( Izd, Af)*BW, 1.0, "flicker");
  I(n1,na) <+  V(n1,na)/RfInt;
  I(n1,nk) <+  white_noise(2.0*P_Q*Ifd*BW,"white");
  I(n1,nk) <+  flicker_noise(Kf*pow( Ifd, Af)*BW, 1.0, "flicker");
  I(n1,na) <+  white_noise(fourKt/RfInt, "white");
  I(nk,n2) <+  ddt( Ttz*Izd);
  I(n1,nk) <+  ( Fcp>V(n1,nk) ) ? ddt( (Cj0*VjT2/(1-M))*(1-pow((1-V(n1,nk)/VjT2), (1-M))) +Tt*V(n1,na)/RfInt)
                       : ddt( Cj0*(F1+(1/F2)*(F3*(V(n1,nk)-Fcp)+(M/(2*VjT2)) )*(V(n1,nk)*V(n1,nk)-
                       Fcp*Fcp)) + Tt*V(n1,na)/RfInt ) ;
  end
endmodule
```

APPENDIX C

TRANSIENT DOMAIN NOISE VOLTAGE PROBE

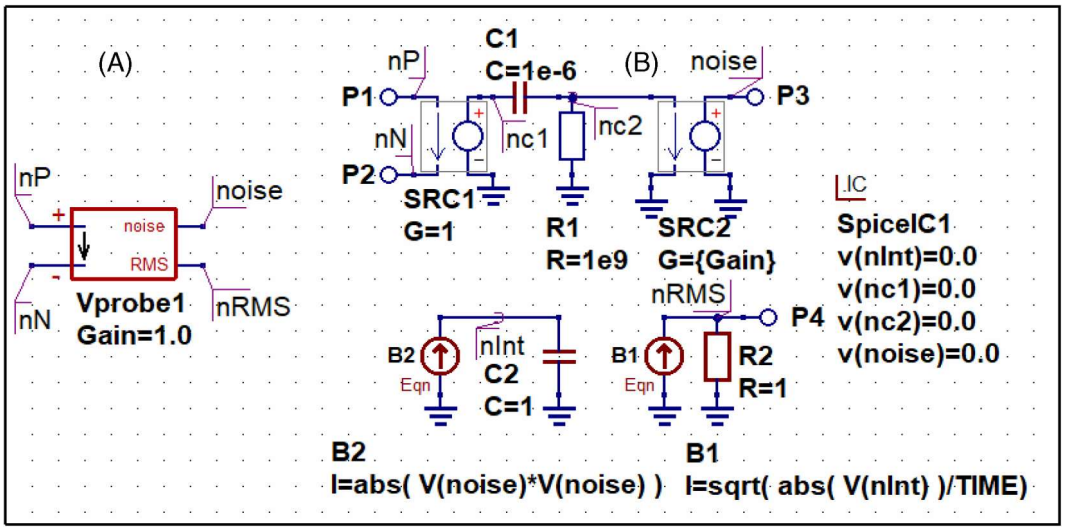

FIGURE C1 Differential voltage probe for transient noise simulation: (A) symbol, (B) subcircuit schematic.

AUTHOR BIOGRAPHY

Mike Brinson received a first class honours BSc degree in the Physics and Technology of Electronics from the United Kingdom Council for National Academic Awards in 1965, and a PhD in Solid State Physics from London University in 1968. Since 1968 Dr Brinson has held academic posts in Electronics and Computer Science. From 1997 till 2000 he was a visiting professor of Analogue Microelectronics at Hochschule, Breman, Germany. Currently, he is a professor at the Centre for Communication Technology Research, London Metropolitan University, United Kingdom. He is a Chartered Engineer (CEng) and a fellow of the Institution of Engineering and Technology (FIET), a Chartered Physicist (CPhys), and a member of the Institute of Physics (MInstP). Prof Brinson joined the Qucs project development team in 2006.