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RESEARCH ARTICLE

Compact macromodelling of operational amplifiers with equation defined devices

M.E. Brinson[a1] and S. Jahn[b]
[a]Department of Computing, Communications Technology and Mathematical Sciences, London Metropolitan University, UK, email: mbrin72043@yahoo.co.uk; [b] Fakultät IV-Elektrotechnik und Informatik, Fachgebiet Mikrowellentechnik, Technische Universität Berlin, Germany, email:Stefan@gruft.de.

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A new approach to the design of operational amplifier macromodels, based on a multi-terminal non-linear equation defined device, is presented. The concept of a compact macromodel is introduced and demonstrated by the design of a general purpose operational amplifier macromodel. The new macromodel models the principle operational amplifier characteristics, plus a number of features not normally found in previously published macromodels, including common-mode range, differential gain reduction during output voltage saturation, power-supply current sensing and temperature effects. The performance of the new macromodel has been tested using the Qucs circuit simulator and has been found to perform well in comparison to other published operational amplifier macromodels.

Keywords: operational amplifier macromodel; equation defined device; circuit simulation

1. Introduction

Operational amplifier macromodels have been widely employed in circuit simulation since they were first introduced to model devices at a behavioral level [3]. The development of SPICE macromodels is well documented in the scientific literature [2, 5,15] and because of the importance of this topic it continues to attract attention from researchers and device manufactures. A macromodel is a collection of linear and non-linear circuit simulation components combined together as a behavioral model, where the simulated electrical signals at the model input-output pins appear identical to the measured performance of a real device. In practice the majority of operational amplifier macromodels only model a number of the primary amplifier characteristics. Secondary properties are often ignored. For a macromodel developer one of the big challenges is to be able to construct a model which simulates as wide a range of physical circuit properties as possible, while minimising model complexity. With circuit simulators without equation defined components it is difficult to construct universal macromodels that allow component values to be calculated by a simulator, prior to the start of simulation or during simulation. Recent trends in circuit simulation and semiconductor device modelling indicate a growing movement towards standardisation of the Verilog-A hardware description language as a vehicle for semiconductor compact device specification and model interchange among commercial [10] and GNU circuit simulators

[1] Corresponding author. Email:mbrin72043@yahoo.co.uk

[11]. This paper presents a new approach to the design of operational amplifier macromodels and introduces the concept of a compact macromodel. A compact macromodel for a general purpose operational amplifier, centered on the well-known 741 operational amplifier, is described. This model comprises standard components, whose values are determined by numerical constants or symbolic equations, and non-linear equation defined devices (EDD) which are similar, but more advanced, to the SPICE 3 type B component [14]. The new macromodel has been implemented and tested using the Qucs circuit simulator [17]. Appendix 1 gives a brief description of the Qucs analogue capabilities and availability.

2. Compact macromodel description

Illustrated in Figure 1 is a compact macromodel for a general purpose operational amplifier. The term compact macromodel is introduced to indicate the similarity between the Verilog-A [1] specification of compact semiconductor device models and the approach adopted in this paper for the specification of operational amplifier macromodels. The proposed specification method is based on a set of equations which define the behavioural characteristics of the integrated circuit being modelled. Using these equations as a guide a compact macromodel can be constructed from (1) passive and active components with values expressed as numerical quantities or subcircuit parameters or algebraic equations, (2) multi-terminal non-linear equation defined devices (Appendix 2 outlines the properties of this novel component), and (3) linear controlled voltage and current sources that act as buffering blocks, current and voltage sensors or conversion elements. The model shown in Figure 1 illustrates all these features. In Figures 1(b) and 1(d) the compact macromodel equations are listed in a written syntax that has similar attributes to Verilog-A. Verilog-A is an analogue sub-set of the Verilog-AMS hardware description language. It has been specifically designed for modelling semiconductor device behaviour, replacing the more traditional C models. Compact macromodel equations consist of variables, numerical constants, operators, functions and an if-then-else construction similar to the C language ternary ?: statement. By employing schematic capture to construct a model diagram with embedded component equations the functional parts of a compact macromodel can be directly linked to a subcircuit symbol, ensuring that the macromodel development/simulation cycle becomes highly interactive, making experimentation with new model features very straightforward. Once fully tested compact macromodel equations can be easily converted to Verilog-A and translated to C, using for example, ADMS [16] prior to compilation and permanent inclusion in a simulator model library. A great advantage of this approach is that it allows fast prototyping of new macromodels without the need for a detailed understanding of a circuit simulators programming application interface [13]. However, some loss of simulation speed is likely due to the fact that compact macromodels are not converted into C code, compiled and linked with other parts of a simulator.

3 The operational amplifier compact macromodel specification

The compact macromodel shown in Figure 1 models a general purpose operational amplifier with the following characteristics:

- Input stage: Off-set voltage and current, bias current, differential input resistance

and capacitance.

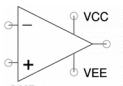
- Differential gain: Two pole response.
- Common-mode gain: Single zero response.
- Large signal properties: Slew rate limiting and common-mode range limiting.
- Output stage: resistance, output voltage limiting with reduced differential gain in saturation and current limiting.
- Power supply properties: Symmetrical and non-symmetrical power connections and power supply current sensing.
- Properties with temperature variation: Offset voltage and current, bias current, differential input resistance and maximum DC output current.

The parameter specifications and default values for the new compact macromodel subcircuit are listed in Table 1.

Table 1. Subcircuit parameters for a general purpose compact operational amplifier macromodel with typical UA741 values as default.

Name	Symbol	Description	Unit	Default
IB	I_B	Input bias current	A	80e-9
IB_TC	I_BTC	Input bias temp. coeff.	A $^oC^{-1}$	-1e-9
VOFF	V_{OFF}	Input offset voltage	V	7e-4
VOFF_TC	$V_{OFF}TC$	Input offset voltage temp. coeff.	V $^oC^{-1}$	1e-5
IOFF	I_{OFF}	Input offset current	A	1e-8
IOFF_TC	$I_{OFF}TC$	Input offset current temp. coeff.	A $^oC^{-1}$	-2e-10
RD	R_D	Differential input resistance	Ω	2e6
RD_TC	R_DTC	Differential input resistance temp. coeff.	$^oC^{-1}$	1.82e4
CD	C_D	Differential input capacitance	F	1.4e-12
AOL_0	*AOL0*	Differential gain at DC	dB	105
GBP	*GBP*	Differential unity gain frequency	Hz	1e6
FP2	*FP2*	Differential gain second pole frequency	Hz	3e6
CMRR_0	*CMRR0*	DC common-mode rejection ratio	dB	90
FCM	*FCM*	Common-mode gain zero frequency	Hz	200
CMR	*CMR*	Common-mode range voltage	V	12¥
PSRT	*PSRT*	Positive signal slew rate	Vs^{-1}	5e5
NSRT	*NSRT*	Negative signal slew rate	Vs^{-1}	5e5
RO	R_O	Output resistance	Ω	75
ILMAX	IL_{MAX}	Maximum DC output current	A	3.4e-2
ILMAX_TC	$IL_{MAX}TC$	Maximum DC output current temp. coeff.	A $^oC^{-1}$	-7.1e-5
VLIMP	*VLIMP*	Maximum positive output voltage	V	14¥
VLIMN	*VLIMN*	Maximum negative output voltage	V	-14¥
Tnom	*Tnom*	Circuit parameter measurement temperature	^oC	26.85
Temp	*Temp*	Circuit temperature	^oC	26.85
SFACT1	*SFACT1*	Current limit scale factor	V	0.85
SFACT2	*SFACT2*	Common-mode range scale factor	V	10¥
SFACT3	*SFACT3*	Differential voltage gain scale factor		-100
PWD	*PWD*	Power consumption	W	50e-3

¥ VCC = +15V and VEE = -15V




```
SUB1
GBP=1e6
PSRT=0.5e6
NSRT=0.5e6
CMRRDC=90.0
FCM=200
AOLDC=106.0
FP2=3e6
RO=75
CD=1.4e-12
RD=2e6
IOFF=20e-9
IB=80e-9
VOFF=0.7e-3
ILMAX=34e-3
VLIMP=14
VLIMN=-14
SFACT1=0.85
SFACT2=10
CMR=12
Temp=26.85
IB_TC=-1e-9
VOFF_TC=10e-6
Tnom=26.85
IOFF_TC=-200e-12
RD_TC=18.2e3
ILMAX_TC=-0.071e-3
SFACT3=-100
PWD=54e-3
```

Figure 1(a)

Equation

```
Eqn1
GCMRR0=1e6/CMRR_0
AOL_0=10^(AOLDC/20)
CMRR_0=10^(CMRRDC/20)
ILMAXT=ILMAX+ILMAX_TC*(T-TN)
VOFFT=VOFF+VOFF_TC*(T-TN)
RDT=RD+RD_TC*(T-TN)
IBT=IB+IB_TC*(T-TN)
IOFFT=IOFF+IOFF_TC*(T-TN)
T=Temp+273.15
TN=Tnom+273.15
CL_GAIN=SFACT1/ILMAXT
K1=1/(2*pi*GBP)
VT=vt(300)
CP1=K1
CP2=1/(2*pi*FP2)
CCMZ=1/(2*pi*1e6*FCM)
VOFFD2=VOFFT/2
IOFFD2=IOFFT/2
RD2=RDT/2
SLRTN=NSRT*K1
SLRTP=PSRT*K1
```

Figure1(b)

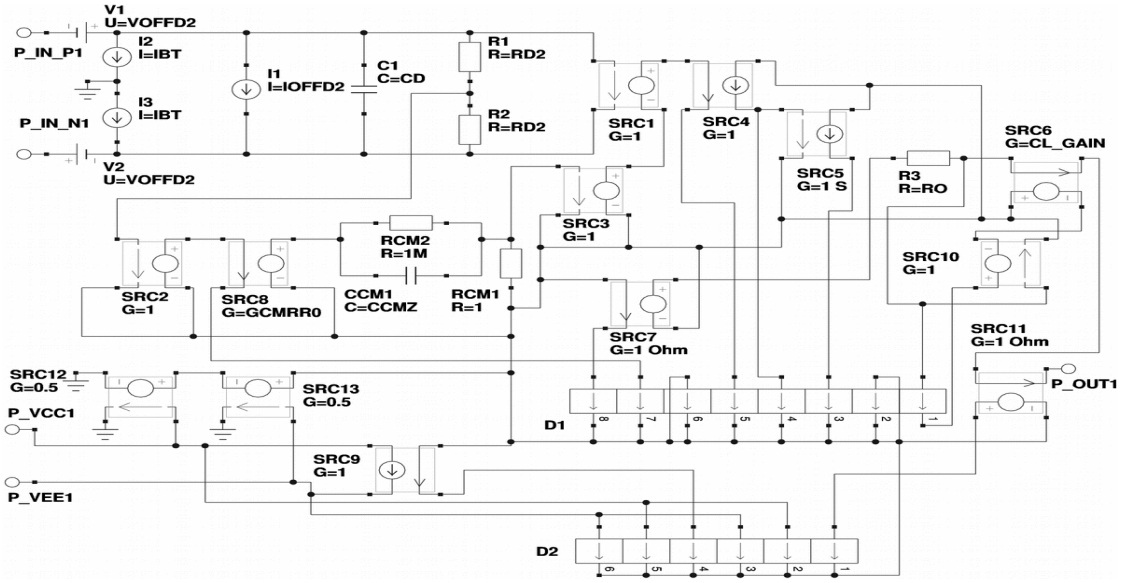
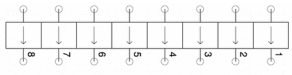
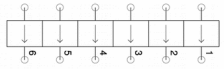


Figure1(c)





```
D1
Type=explicit
I1=(V1>0) ? 5e-16*(limexp(V1/VT)-1) : -5e-16*(limexp(-V1/VT)-1)
Q1=0
I2=0
Q2=0
I3=V3
Q3=CP2*V3
I4=(V4 > (VLIMP) ) ? V4/(AOL_0*limexp(SFACT3*( (V4/VLIMP)-1)) + 500)  :  (V4 < VLIMN)  ? V4/(AOL_0*limexp( SFACT3*((V4/VLIMN) - 1)) + 500) : V4/AOL_0
Q4=CP1*V4
I5=(V5 > SLRTP) ? SLRTP : (V5 < -SLRTN) ? -SLRTN : V5
Q5=0
I6=0
Q6=0
I7=CMR*tanh(V7/SFACT2)
Q7=0
I8=(V3 >= VLIMP) ? VLIMP : (V3 <= VLIMN) ? VLIMN: V3
Q8=0
```

```
D2
I1=0
I2=(V1 > 0) ? V1 : 0
I3=(V1 < 0) ? -V1 : 0
I4=PWD/((V5-V6)+1e-4)
I5=0
Q5=0
I6=0
Q6=0
```

Figure 1(d)

Figure 1. A compact macromodel for a general purpose operational amplifier: (a) subcircuit symbol and default UA741 parameters; (b) model equations; (c) model schematic; (d) EDD symbols and equations.

4. Input stage

The operation of the input stage of the macromodel shown in Figure 1 is determined by conventional electrical parameters; voltage offset (V_{OFF}), bias current (I_B), current offset (I_{OFF}), differential input resistance (R_D) and differential input capacitance (C_D). However, unlike many previously reported macromodels a number of these parameters are modelled as functions of circuit parameter measurement temperature (*Tnom*) and circuit temperature (*Temp*). Temperature dependence is represented as first order expressions given by equations (1)-(4).

$$VOFFT = V_{OFF} + V_{OFF}TC\ .(T - TN) \tag{1}$$

$$IBT = I_B + I_BTC.(T - TN) \tag{2}$$

$$IOFFT = I_{OFF} + I_{OFF}TC.(T - TN) \tag{3}$$

$$RDT = R_D + R_DTC.(T - TN) \tag{4}$$

Where, circuit temperature $T = Temp + 273.15$ K and circuit parameter measurement temperature $TN = Tnom + 273.15$ K. Figure 2 illustrates the effect of circuit temperature on the output voltage of a unity gain non-inverting amplifier with zero applied input voltage.

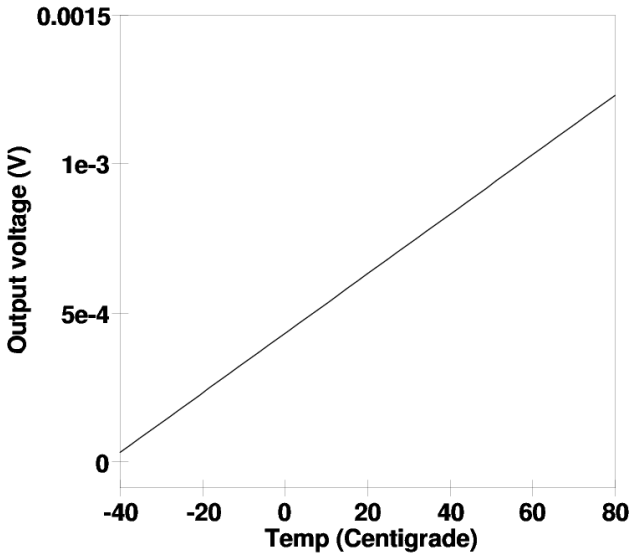


Figure 2. Output voltage against circuit temperature for a unity gain non-inverting amplifier with zero input voltage.

5. Common-mode characteristics

A high percentage of published operational amplifier macromodels model DC common-mode rejection ratio. A smaller percentage of these models also include AC common-mode effects. However, to the author's knowledge the majority of published macromodels make no attempt to model common-mode range. The new macromodel

illustrated in Figure 1 includes all three properties. Voltage controlled voltage source SRC2 senses the operational amplifier common-mode signal and applies the sensed voltage to branch 7 of EDD D1. The current flowing in this branch is set by equation (5).

$$I_7 = CMR \,.\tanh\left\{\frac{V_7}{SFACT\,2}\right\} \tag{5}$$

Where, *CMR* is the common-mode range and *SFACT2* is a scaling factor. Figure 3 gives a plot of I_7 as a function of V_7 for four values of *SFACT2*, clearly illustrating the limiting feature of the tanh function.

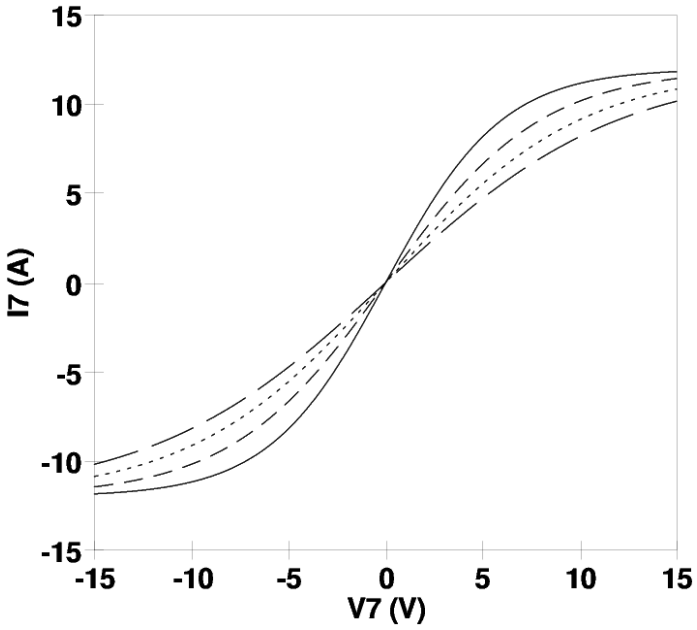


Figure 3. Plot of EDD D1 current I_7 against V_7 with *CMR* = 12 V: solid line *SFACT2* = 6 V; dash line *SFACT2* = 8 V; dot line *SFACT2* = 10 V; long dash line *SFACT2* = 12 V.

Figure 4(a) shows a typical set of output signals obtained from the simulation of a matched resistor CMRR test circuit [7]. At high input signal levels the simulated CMRR output signals show distortion effects due to common mode range limiting. This effect is often observed with actual amplifier CMRR measurements. Linear controlled source SRC8 converts current I_7 to a voltage. This voltage becomes the amplifier common-mode signal after being transformed by the voltage divider network CCM1, RCM2 and RCM1. Frequency dependent common-mode effects are modelled by the common-mode rejection ratio defined in equations (6)-(7).

$$C_{MRR}(\omega) = \frac{A_D(\omega)}{A_{CM}(\omega)} = \frac{CMRR0}{\left(1 + j\frac{\omega}{\omega_{Z1}}\right)} \tag{6}$$

$$A_D(\omega) = \frac{AOL0}{\left(1 + j\frac{\omega}{\omega_{P1}}\right).\left(1 + j\frac{\omega}{\omega_{P2}}\right)},$$
$$A_{CM}(\omega) = ACM0.\frac{\left(1 + j\frac{\omega}{\omega_{Z1}}\right)}{\left(1 + j\frac{\omega}{\omega_{P1}}\right).\left(1 + j\frac{\omega}{\omega_{P2}}\right)} \quad (7)$$

Where, *CMRR0* is the common-mode rejection ratio at DC, *AOL0* is the differential gain at DC, *ACM0* is common-mode gain at DC, ω_{Z1} is the angular frequency of a zero in the common-mode gain, and ω_{P1} and ω_{P2} are the angular frequencies of the two poles in the differential gain. The gain of controlled source SRC8 is *GCMRR0*=1e6/*CMRR0*, while capacitor *CCMZ*=1/(2.π.1e6.*FCM*) and the common-mode signal transfer function is given by equation (8).

$$V(SRC3) = \left(\frac{1}{CMRR0}\right).\left(\frac{1 + j\omega.1e6.CCMZ}{1 + j\omega.CCMZ}\right).V(SRC8) \quad (8)$$

Where, *V(SRC8)* is the voltage applied to the voltage divider network. The voltage divider network introduces a zero in the AC common-mode gain response at frequency *FCM*, and a pole at high frequencies well above the normal operating frequency range of the macromodel. For all practical purposes this pole can be ignored. Figure 4(b) shows the simulated AC CMRR for the default UA741 parameters.

Figure 4(a) Figure 4(b)

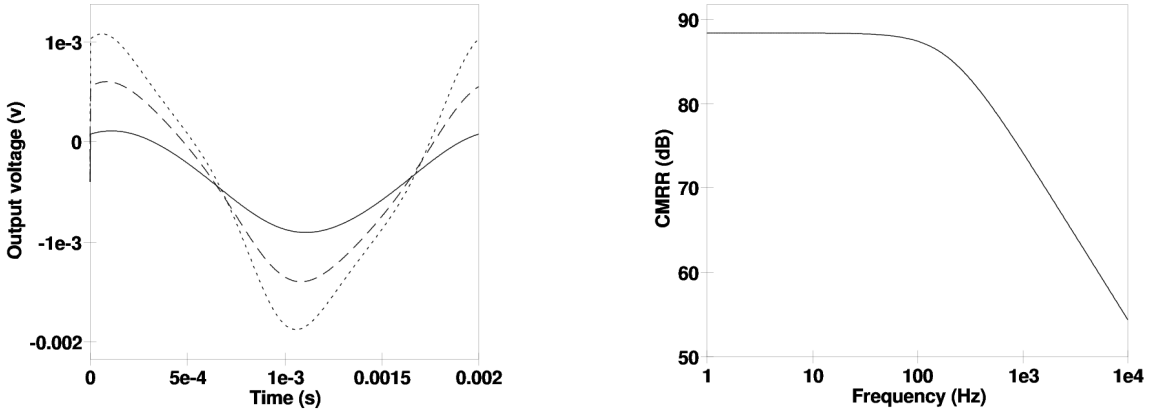


Figure 4. Plots of CMRR simulated results for a matched resistor test circuit (matched resistors = 10 kΩ, VCC = 15 V, VEE = -15 V): (a) transient output voltage against time for sinusoidal input signal with frequency = 500 Hz; solid line V_{in} = 5 V peak, dash line V_{in} = 10 V peak, dot line V_{in} = 15 V peak and (b) small signal AC CMRR against frequency.

6. Slew rate limiting

Voltage controlled sources SRC1 and SRC3 sense and add the input stage differential and the range limited and transformed common-mode voltage signals. The resulting voltage

is applied to branch 5 of EDD D1, yielding a slew rate limited current given by the if-then-else expression shown in equation (9).

$$I_5=\left(V_5>SLRTP\right)\ ?\ SLRTP\ :\ \left(V_5<SLRTN\right)\ ?\ -SLRTN\ :\ V_5 \tag{9}$$

Where, voltage *SLRTP=PSRT / (2.π.GBP)* V, voltage *SLRTN=NSRT / (2.π.GBP)* V and *GBP* is the differential gain bandwidth product in Hz. When V_5 is greater than *SLRTP* or smaller than *SLRTN,* I_5 is clamped, limiting the magnitude of the current that charges differential amplifier capacitor CP1. Current controlled current source SRC4 senses current I_5 and applies it as current I_4 to the first stage of the macromodel differential amplifier, branch 4 of EDD D1. Figure 5 shows the effect of slew rate limiting on a 10k Hz sinusoidal signal.

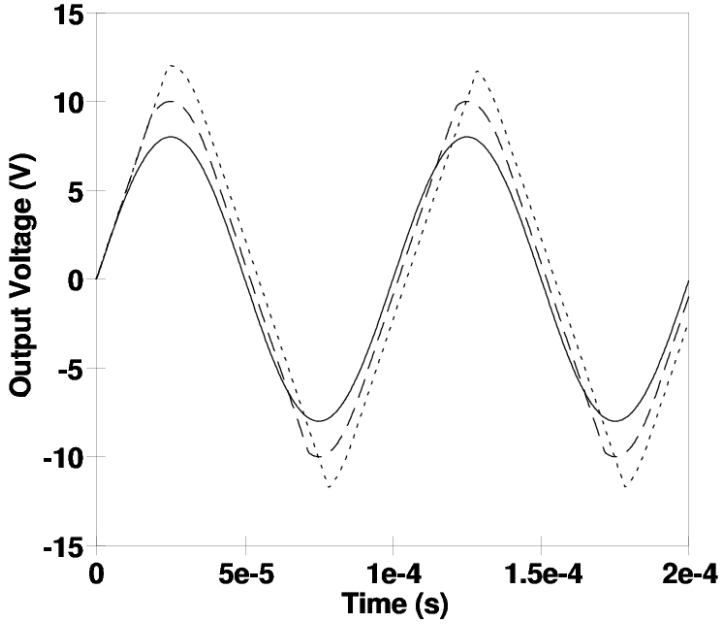


Figure 5. Unity gain non-inverting amplifier slew rate limited output voltage against time: sinusoidal input signal frequency = 10 kHz; solid line V_{in} = 8 V peak, dash line V_{in} = 10 V peak, and dot line V_{in} = 12 V peak.

7. The differential amplifier

Branches 4 and 3 of EDD D1 model a conventional differential amplifier with a high DC gain and a two pole frequency response. Under non-saturated output conditions controlled current source SRC4 sets branch current I_4 to the value given in equation (10).

$$I_4=\frac{V_4}{AOL0} \tag{10}$$

Where, *AOL0* is the DC differential gain. The frequency of the dominant pole in the differential gain response determines the value of stored charge Q_4. This is done indirectly by setting Q_4=*CP1*.V_4, where capacitor *CP1=1 / (2.π.GBP)*. Branch voltage V_4 is sensed by voltage controlled current source SRC5. The resulting current sets branch current I_3 to the value given in equation (11).

$$I_3 = V_3 \tag{11}$$

The frequency of the second pole in the differential gain response determines the value of stored charge Q_3. Again, this is done indirectly by setting Q_3=*CP2*.V_3, where capacitor *CP2=1 / (2.π.FP2*) and *FP2* is the second pole frequency. This normally has a value much higher than the dominant pole frequency. Figure 6 shows the simulated open-loop small signal AC differential gain and phase characteristics for the default UA741 parameters. Current controlled voltage source SRC7 senses EDD D1 branch current I_8. This is magnitude limited with a value controlled by the if-then-else equation given in (12).

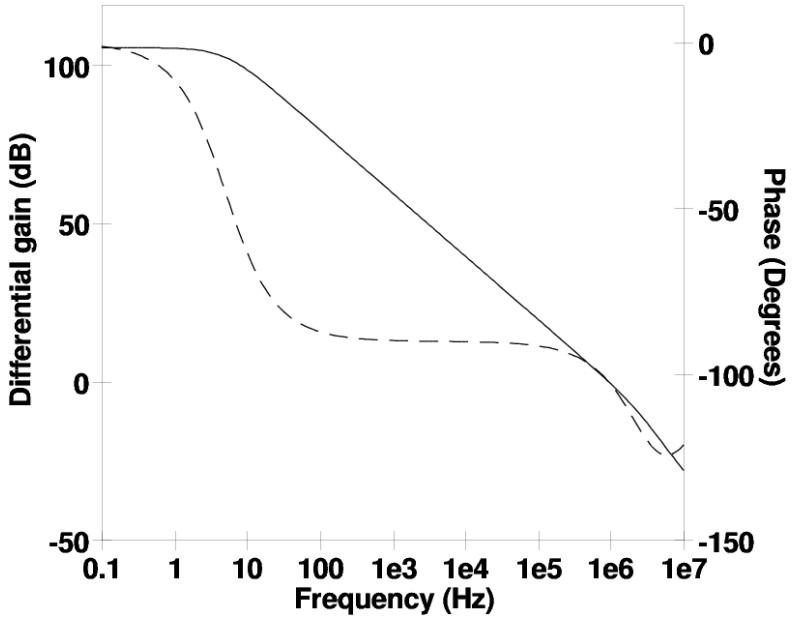


Figure 6. Plot of simulated open-loop AC small signal differential gain and phase against frequency: solid line = gain and dash line = phase.

$$I_8 = (V_3 \geq VLIMP)\ ?\ VLIMP : (V_3 \leq VLIMN)\ ?\ VLIMN : V_3 \tag{12}$$

Where, *VLIMP* is the amplifier positive voltage output limit, *VLIMN* is the negative voltage output limit and V_3 is the differential amplifier output voltage. Source SRC7 converts current I_8 to voltage and drives output resistance R_O. At signal levels where $VLIMN < V_3 < VLIMP$, $I_8 = V_3$. In the simulation of closed-loop non-inverting operational amplifier circuits an error can occur if the differential input signal increases significantly above or below zero volts. For example, the differential signal (V^+-V^-) can

reach around ±1 V when the macromodel output voltage becomes clamped and V_{in} peak is ±15 V AC (with *VLIMP* = 14 V, *VLIMN* = -14 V, VCC = 15 V and VEE = -15 V). For a real operational amplifier in this situation, it's differential gain is likely to become magnitude limited otherwise internally amplified voltages would rise or fall to values well above or below the power supply rail voltages. In the new compact macromodel the differential gain is reduced when the output voltage saturates at *VLIMP* and *VLIMN*. This is achieved by setting EDD D1 branch 4 current to a value given by equation (13)

$$I_4 = (V_4 > VLIMP)\ ?\ \frac{V_4}{AOL0 \cdot \mathrm{limexp}\left\{SFACT3 \cdot \left[\frac{V_4}{VLIMP} - 1\right]\right\} + 500} :$$
$$\left(V4 < VLIMN\right)\ ?\ \frac{V_4}{AOL0 \cdot \mathrm{limexp}\left\{SFACT3 \cdot \left[\frac{V_4}{VLIMN} - 1\right]\right\} + 500} : \frac{V_4}{AOL0} \qquad (13)$$

Where, *SFACT3* is a scaling factor and *limexp* is a Verilog-A style exponential function whose value is restricted to a finite range at large function arguments. Figure 7 illustrates a plot of *AOL0* as a function of V_4 (12 to 15 V) for four values of *SFACT3*, demonstrating the reduction of differential gain when the amplifier model saturates at *VLIMP*. This important effect appears not to have been modelled by previously published operational amplifier macromodels.

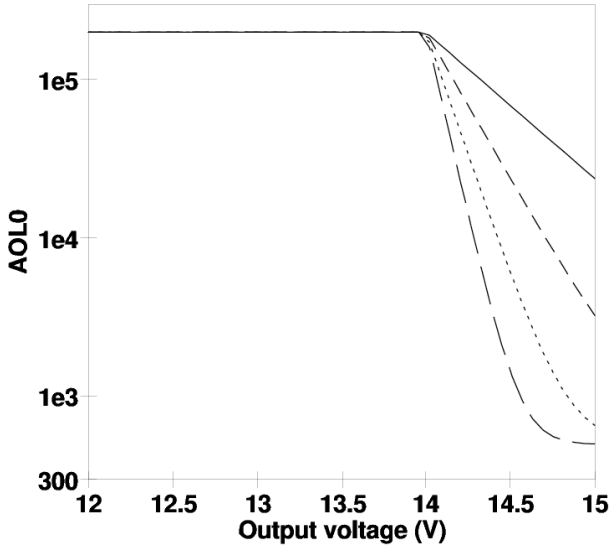


Figure 7. Plot of *AOL0* against V_4 (12 to 15 V) for four values of *SFACT3* showing reduction of *AOL0* at V_4 > *VLIMP*: solid line *SFACT3* = -30, dash line *SFACT3* = -60, dot line *SFACT3* = -100 and *SFACT3* = -150.

8. Output current limiting

Output current limiting occurs when the load current exceeds the maximum allowed value for a given operational amplifier. The maximum current is defined by parameter *ILMAX*. Components SRC6, SRC10 and EDD D1 (branch 1) limit the load current to *ILMAX*. One feature of the compact macromodel is novel, this being the use of EDD D1 branch 1 as a replacement for back-to-back semiconductor diodes. Equation (14) gives an expression for the current flowing through this device.

$$I_1=(V_1>0)\ ?\ 5e-15.\left(\text{limexp}\left\{\frac{V_1}{VT}\right\}-1\right)\ :\ -5e-15.\left(\text{limexp}\left\{\frac{V_1}{VT}\right\}-1\right) \qquad (14)$$

Where, $VT=vt(300)$ is the thermal voltage at 300 K. Figure 8 illustrates a plot of I_1 against V_1. Model parameter *SFACT1* is used to accurately adjust the magnitude of the simulated clamping current to the value specified by *IMAX*. In the model the maximum load current is also specified as a function of temperature by equation (15).

$$ILMAXT=IL_{MAX}+IL_{MAX}\,TC.\left|\ T-TN\right| \qquad (15)$$

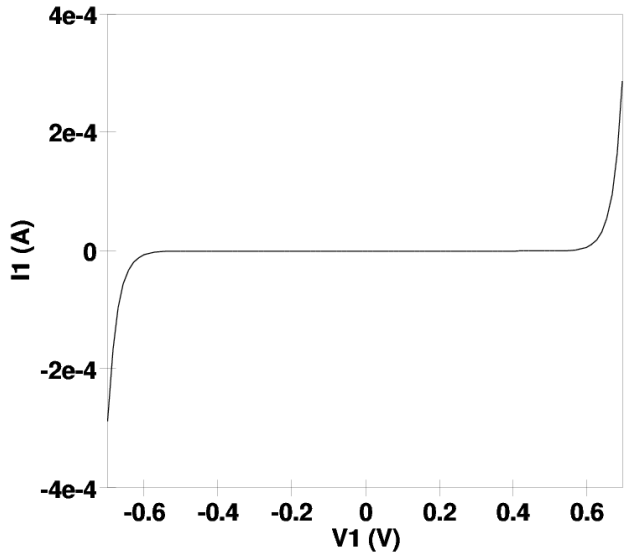


Figure 8. Plot of EDD D1 branch 1 current I1 against branch voltage V1.

9. Power-supply configuration

A high percentage of operational macromodels, including the original Boyle model, have their internal signals referenced to ground. This is satisfactory for operational amplifiers operated from symmetrical power supplies but does not allow single supply devices or applications with non-symmetrical power supplies to be simulated correctly. The compact macromodel shown in Figure 1 employs a floating signal reference system with controlled sources SRC12 and SRC13 generating the correct reference voltage by averaging the voltages applied to power-supply pins P_VCC1 and P_VEE1.

10. Power-supply current sensing

Operational amplifier supply-current sensing is an often used technique for implementing current-mode circuits [18]. Unfortunately, very few operational amplifier macromodels correctly sense power-supply current but require additional external networks in order to represent this important feature [6]. This deficiency has been rectified in the new compact operational amplifier macromodel through the inclusion of a simple, but effective, addition to the model which mirrors load current in the power-supply leads. Current controlled voltage source SRC11 senses the current flowing in the external load. This is converted to voltage and applied to branch 1 of EDD D2. The current flowing in this branch and the internal charge are both set to zero, making branch 1 effectively a high impedance probe that monitors applied voltage V_1. EDD D1 branches 2 and 3 act as current sources that inject current into the power-supply leads. The magnitude and polarity of the injected currents mirror that in the load, being determined by the if-then-else statements given in equations (16)-(17).

$$I_2 = (V_1 > 0) \; ? \; V_1 : 0 \tag{16}$$

$$I_3 = (V_1 < 0) \; ? \; -V_1 : 0 \tag{17}$$

Current controlled current generator SRC9 connected between supply pins P_VCC1 and P_VEE1 causes a constant DC current to flow between the power-supplies, modelling the standing current drawn by an operational amplifier. The value of this current is given by equation (18).

$$I(SRC9) = \frac{PWD}{(VCC - VEE)} \tag{18}$$

Where, *PWD* is the operational amplifier power dissipation and *VCC* and *VEE* are the power-supply voltages. Figure 9 shows a typical plot of simulated power-supply sensed current as a function of load current for the default UA741 parameters.

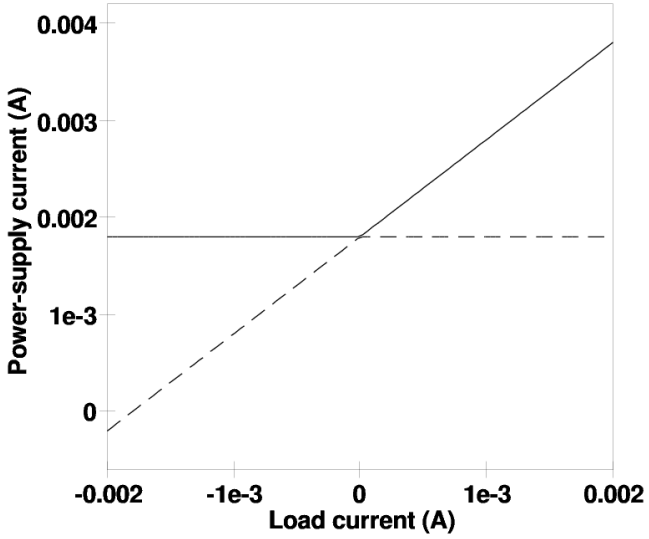


Figure 9. Power-supply current against load current for the default UA741 parameters.

11. Conclusions

The combination of conventional plus linear and non-linear equation defined components provides a highly flexible macromodelling resource, opening up new possibilities in the design of integrated circuit macromodels. In this paper the concept of a compact macromodel has been introduced and demonstrated with an example operational amplifier model that uses subcircuit parameters which can be found in the majority of manufacturer's data sheets. Most of the data, from which the parameters are extracted, are either published as minimum, typical or worst case values or graphs showing their variation with power-supply voltages, frequency or temperature. All parameters, with the exception of the temperature coefficients, are estimated to be accurate to a few percent. However, temperature coefficients are probably not as accurate due to the fact that simple linear functions of temperature have been assumed. If higher accuracy is required a higher order polynomial could be fitted to the relevant temperature dependent data and the appropriate compact macromodel equations changed. The example compact macromodel extends the range of commonly modelled operational amplifier characteristics to include, common-mode range effects, differential gain reduction when output voltage saturation occurs, power-supply current sensing and parameter variation with changing circuit temperature. When required, additional sections can be easily added to model other operational amplifier features, including for example, noise [9] and power-supply rejection effects [8]. It is also possible to model self-heating effects with the Qucs EDD component. This is achieved by connecting an EDD branch to a subcircuit pin, allowing an external voltage to be monitored whose value is proportional to operational amplifier temperature changes generated by device power dissipation. One feature of the compact macromodel schematic illustrated in Figure 1(c) is worth commenting on, namely that this diagram does not contain any semiconductor devices. This is a direct consequence of the fact that semiconductor device current/voltage characteristic equations and if-then-else statements can be embedded in the EDD behavioural equations, eliminating the need for clamping or limiting diodes. One of the advantages of the compact macromodelling approach, when compared to classical SPICE macromodelling, is centred on the fact that the technique is equation based rather than circuit component based, making modelling of complex circuits more straightforward. The performance of the example operational amplifier compact macromodel has been verified for quiescent (DC), time (transient) and frequency (AC) domains and has been found to operate consistently across domains with a performance comparable with previously published macromodels.

12. References

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Appendix 1. A brief summary of Qucs features

Qucs is a universal circuit simulator developed by a group of international scientists and engineers using the GNU/Linux operating system. It is released under the GPL license and distributed in binary and source code from the Qucs Sourceforge.net website [17]. The package has been successfully compiled and run on most of the popular computer operating systems. Qucs is a circuit simulator with a graphical interface that supports schematic capture, analysis control, and simulation post-processing using equations. It currently supports the following analogue analysis types: DC, AC, AC noise, S-parameter, S-parameter noise and transient.

Appendix 2. The Qucs multi-terminal non-linear equation defined device

The Qucs equation defined device (EDD) is a nonlinear component with multiple branches [4]. Branches are numbered from one to eight. The electrical characteristics of branch n are determined by voltage V_n, current I_n and stored charge Q_n. Branch currents can be non-linear functions of V_n. Stored charge can be non-linear functions of I_n and V_n. These functions must be explicit expressions of the form $I(V_n)$ and $Q(V_n,I_n)$ which can also include numerical constants, variables from Qucs equation blocks (within which the order of items is immaterial), subcircuit parameters, Verilog-A operators and mathematical functions plus other functions defined by Qucs. Conditional current and charge equations can be selected by C style ? : if-then-else statements [12].