Advances in compact semiconductor device modelling and circuit macromodelling with the Qucs GPL circuit simulator

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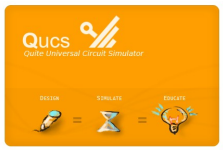
- **Background**
- **Circuit Simulation**
- **Compact device modelling and circuit macromodelling**
- **Summary and future work**



Presented on April 3, 2009, at MOS-AK meeting, IHP, Frankfurt (Oder), Germany

Background

- Qucs is an open source circuit simulator
- Developed using GNU/Linux under the General Public License (GPL)
- Available for most of the popular computer operating systems, including GNU/Linux, Windows®, Solaris®, NetBSD, FreeBSD and MacOS®
- Qucs is one of the GPL circuit simulators taking part in the MOS-AK Verilog-A standardization initiative

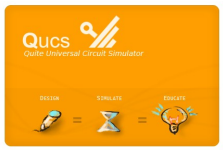
Previously reported details of the simulator capabilities can be found at MOS-AK links

http://www.mos-ak.org/premstaetten/papers/MOS-AK_QUCS_ngspice_ADMS.pdf
http://www.mos-ak.org/munich/posters/P04_MOS-AK_Brinson.pdf
http://www.mos-ak.org/eindhoven/papers/06_Qucs_MOS-AK_Eindhoven.pdf

Or in the following publications

S. Jahn and M. E. Brinson, **Interactive compact device modelling using Qucs equation-defined devices**, International Journal of Numerical Modelling (IJNM): Electronic Networks, Devices and Fields, vol. 21, no. 5, May 2008, pages 335-349.

M. E. Brinson and S. Jahn, **Qucs: A GPL software package for circuit simulation, compact device modelling and circuit macromodelling from DC to RF and beyond**, International Journal of Numerical Modelling (IJNM): Electronic Networks, Devices and Fields, in press, published online 5 Sep. 2008.



Circuit Simulation

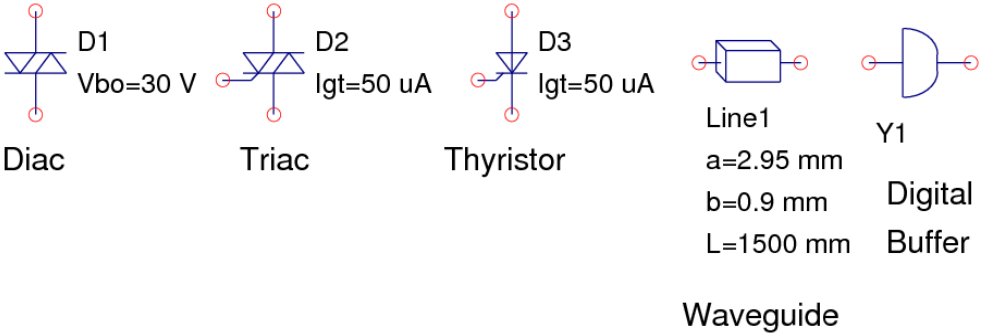
Qucs current versions: production 0.0.14; development 0.0.15

Recent enhancements:

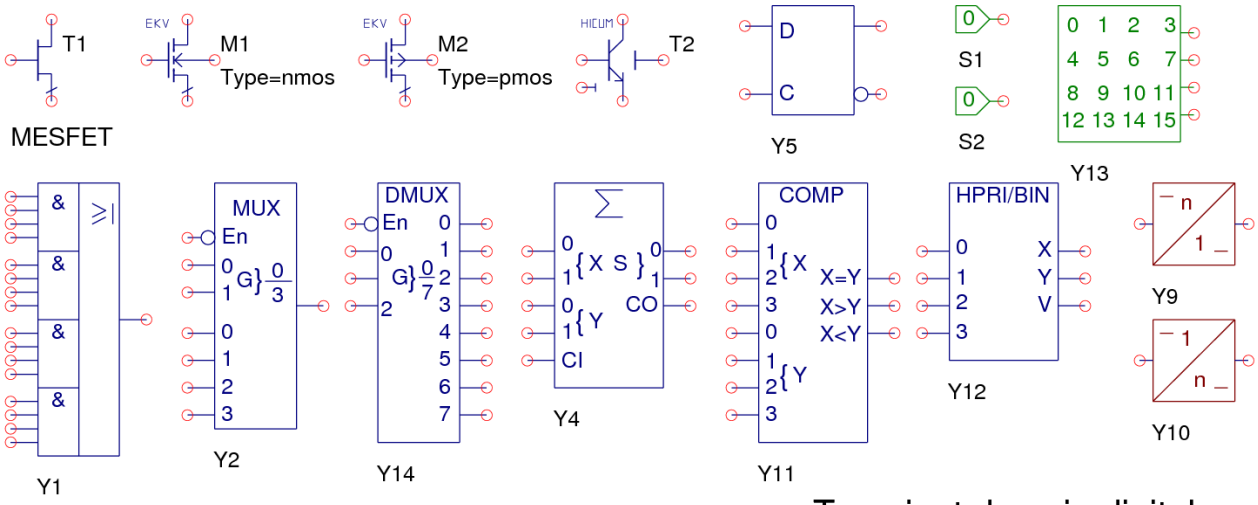
- Implemented 3 and more argument versions of PlotVs() in the equation solver.
- Support for sub- and super-scripts in graphical text paintings
- Implementation of multi-port equation defined RF device (RFEDD). S, Y and Z parameters available
- Implemented 2-port equation defined RF device including S, Y, Z, H, G, T and A-parameters
- Added noise figure property to amplifier model
- Existing HICUM models can now be converted from SPICE by the QucsConv tool into model library entries
- Simulation time for digital files (Verilog and VHDL) now stored in additional configuration file
- Implementation of ddx() operator in equations
- Added coplanar lines (with and without back plane metalisation) to the Qucs Transcalc tool
- Support of US letter formats for schematic frame
- Allowing parameter sweep and other variables in constant parameter simulation boxes
- Added post install script for MacOSX as well as appropriate icons

Additional models and libraries

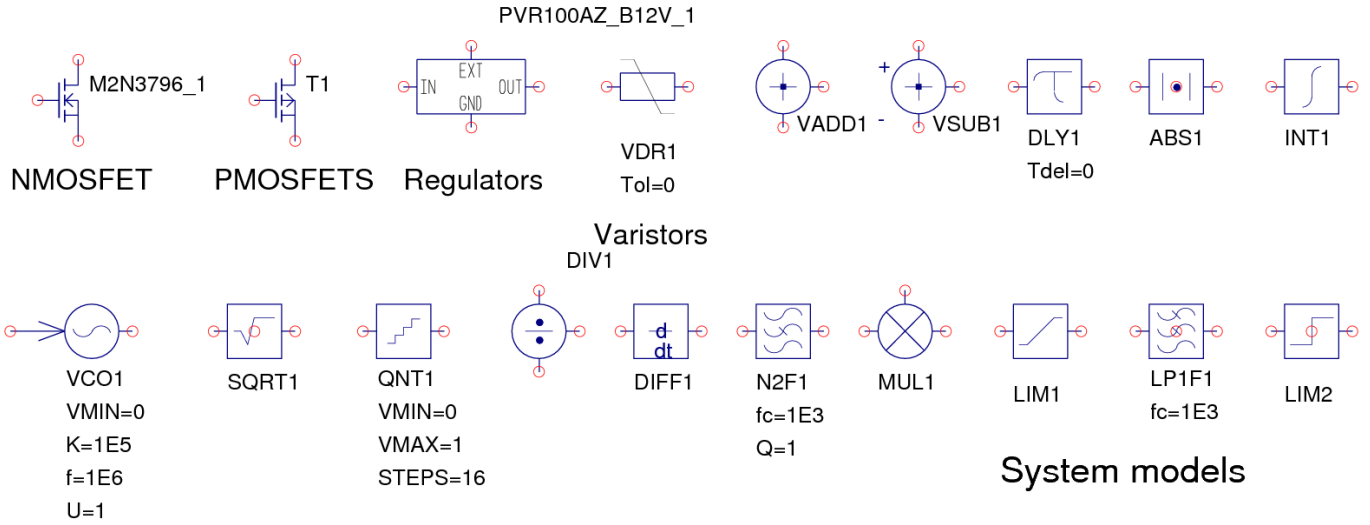
Hand crafted
C++ models



Verilog-A device
models and circuit
macromodels



Model libraries



Compact device modelling and circuit macromodelling

The Qucs circuit simulator provides a mature mix of simulation and analysis routines which are launched from a graphical environment specifically designed for schematic drawing, netlist entry, and simulation control

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Compact device modelling and circuit macromodelling tools

↓

A convenient, interactive and powerful modelling system for building and testing multi-domain simulation models in the following categories

↓

Hand crafted C++ models

Component based subcircuit models

Component based circuit macromodels

Non-linear equation defined device (EDD) models

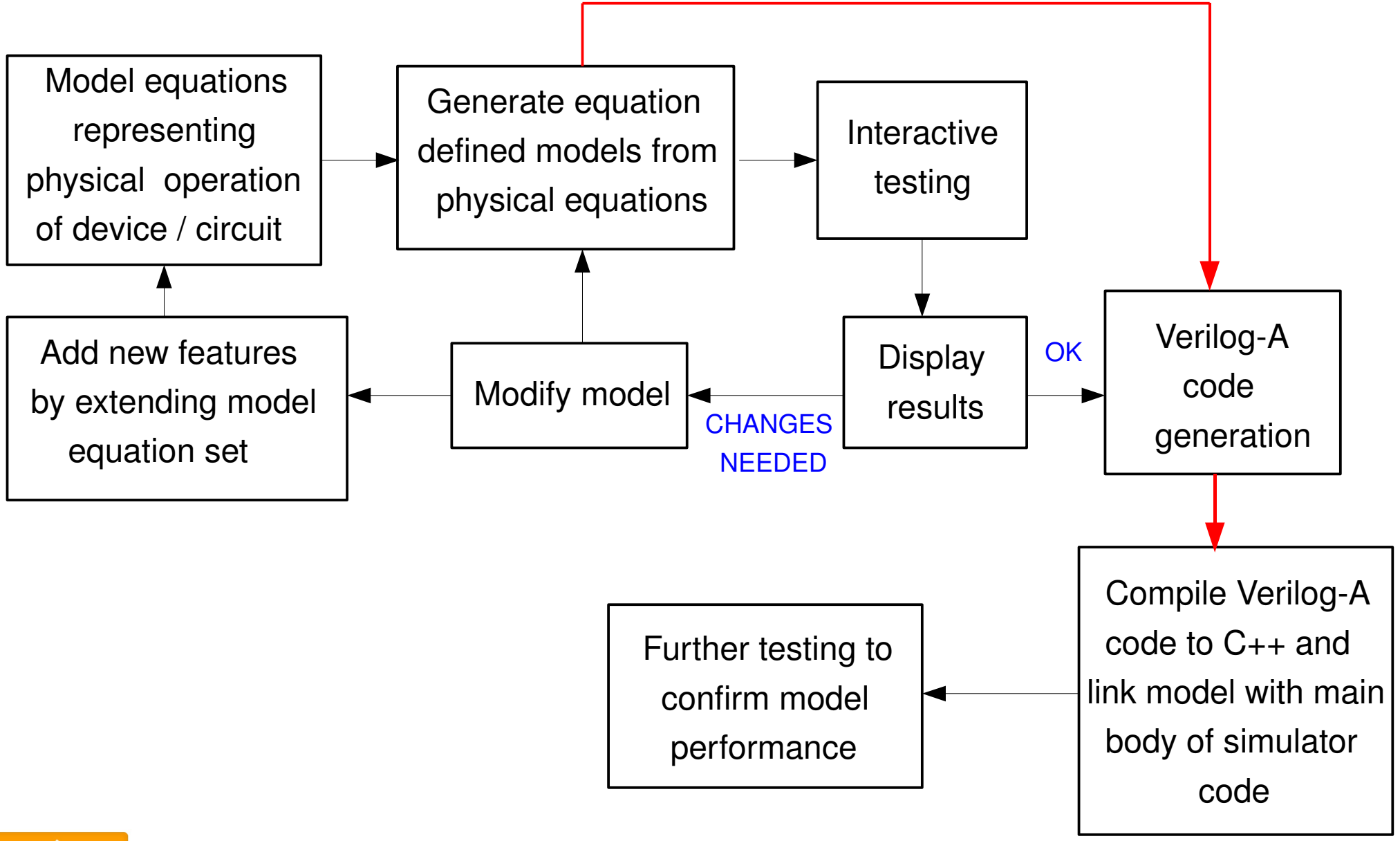
Verilog-A compact device models

Radio frequency equation defined device (RFEDD) models

Verilog-A circuit macromodels

Compact device modelling and circuit macromodelling

Equation based compact model and circuit macromodel construction



Compact device modelling and circuit macromodelling

Building a Qucs equation based model: part 1- DC characteristics

EPFL-EKV v2.6 long channel nMOS equations → Symbol

$$Vg = V(gate) - V(bulk),\quad Vs = V(source) - V(bulk),\quad Vd = V(drain) - V(bulk)$$

$$VGprime = Vg - VTO + PHI + GAMMA \cdot \sqrt{PHI}$$

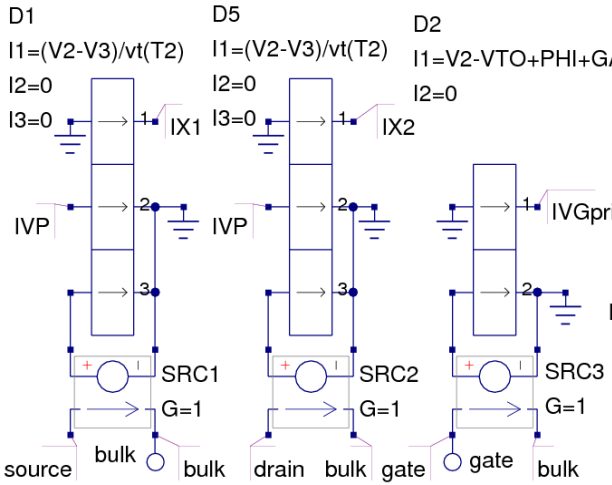
$$VP = VGprime - PHI - GAMMA \cdot \left[\sqrt{VGprime + \left(\frac{GAMMA}{2}\right)^2} - \frac{GAMMA}{2} \right]$$

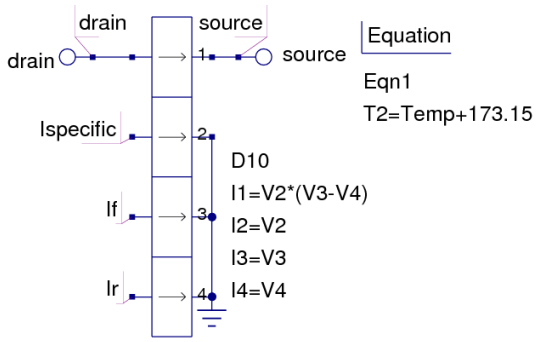
$$n = 1 + \frac{GAMMA}{2} \cdot \sqrt{VP + PHI + 4 \cdot Vt},\quad BETA = KP \cdot \frac{W}{L} \cdot \frac{1}{1 + THETA \cdot VP}$$

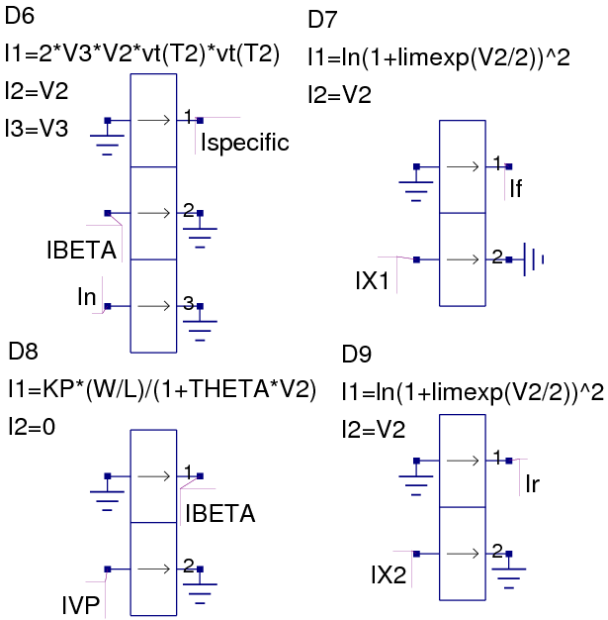
$$X1 = \frac{Vp - Vs}{Vt},\quad If = \left[\ln(1 + limexp(X1/2))\right]^2,\quad X2 = \frac{Vp - Vd}{Vt},\quad Ir = \left[\ln(1 + limexp(X2/2))\right]^2$$

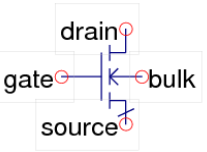
$$Ispecific = 2 \cdot n \cdot BETA \cdot vt^2,\quad Ids = Ispecific \cdot (If - Ir)$$

Model









EKVLC
File=name
L=10e-6
W=10e-6
VTO=0.5
GAMMA=0.7
PHI=0.5
KP=50e-6
THETA=50e-3
Temp=26.85

Compact device modelling and circuit macromodelling

Building a Qucs equation based model: part 2- intrinsic charge characteristics

EPFL-EKV v2.6 long channel nMOS equations

$$nq = 1 + \frac{GAMMA}{2\cdot\sqrt{VP + PHI + 1e\text{-}6}}$$

$$Xf = \sqrt{0.25 + If}\,,\quad Xr = \sqrt{0.25 + Ir}$$

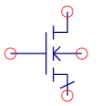
$$qI = -nq\cdot\left[\frac{\frac{4}{3}\cdot(Xf^2 + Xf\cdot Xr + Xr^2)}{Xf + Xr} - 1\right]$$

$$qB = \frac{-GAMMA\cdot\sqrt{VP + PHI + 1e\text{-}6}\cdot 1}{vt} - \left[\frac{nq-1}{nq}\right], when\ \ VGprime > 0$$

$$qB = \frac{-VGprime}{vt}, when\ \ VGprime \le 0$$

$$qG = -qI - qB\,,\quad Cox = COX\cdot W\cdot L\,,\quad Q(I,B,D,S,G) = Cox\cdot vt\cdot q(I,B,D,S,G)$$

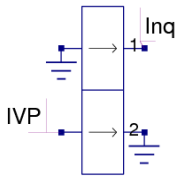
Symbol



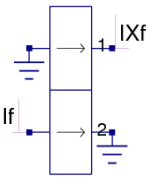
EKVLC1
L=10e-6
W=10e-6
VTO=0.5
GAMMA=0.7
PHI=0.5
KP=50e-6
THETA=50e-3
Temp=26.85
COX=3.45e-3
Xpart=0.6

Model

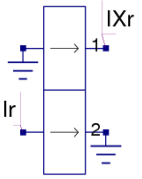
D11
I1=1+GAMMA/(2*sqrt(V2+PHI+1e-6))
I2=0

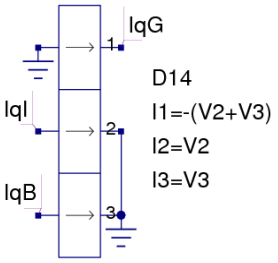


D12
I1=sqrt(0.25+V2)
I2=0



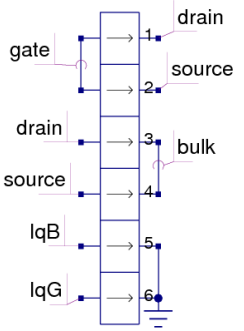
D13
I1=sqrt(0.25+V2)
I2=0





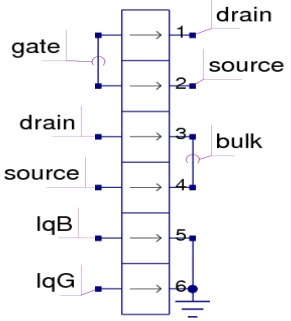
D14
I1=-(V2+V3)
I2=V2
I3=V3

Equation
Eqn1
Spart=1-Xpart
Qox=COX*W*L*vt(T2)



D17
I1=0
Q1=Xpart*V6*Qox
Q2=Spart*V6*Qox
Q3=Xpart*V5*Qox
Q4=Spart*V5*Qox
I5=0
I6=V6

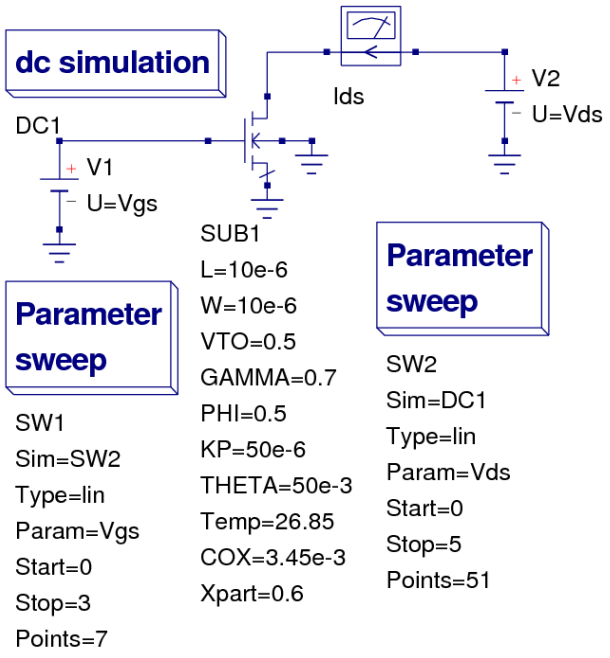
Equation
Eqn1
Spart=1-Xpart
Qox=COX*W*L*vt(T2)

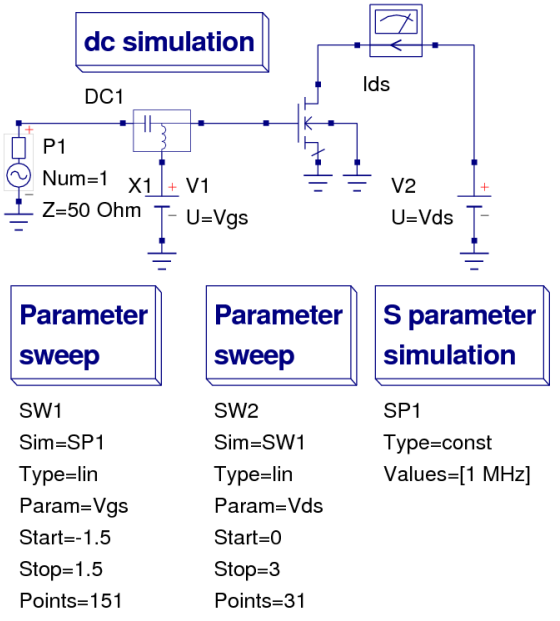


D17
I1=0
Q1=Xpart*V6*Qox
Q2=Spart*V6*Qox
Q3=Xpart*V5*Qox
Q4=Spart*V5*Qox
I5=0
I6=V6

Compact device modelling and circuit macromodelling

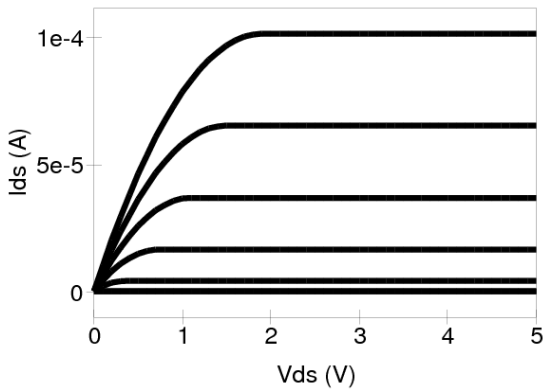
Interactive testing and parameter extraction

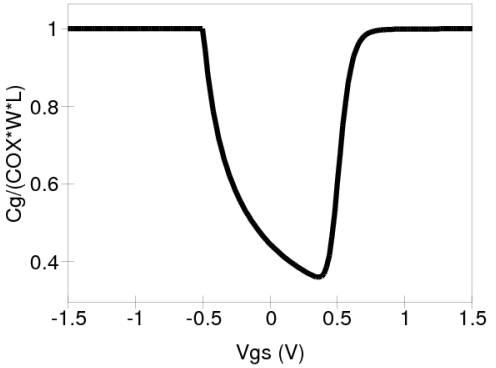


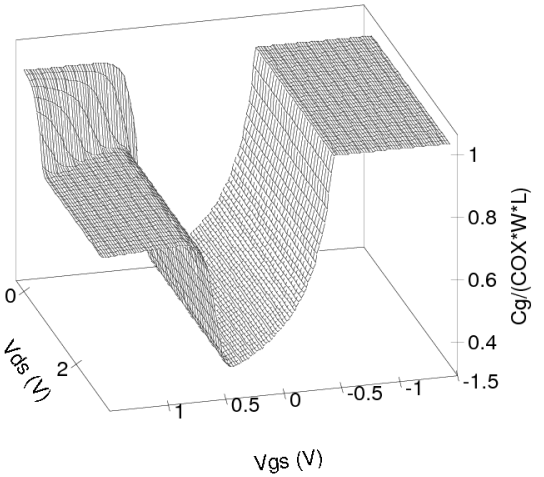


EKVLC1
L=10e-6
W=10e-6
VTO=0.5
GAMMA=0.7
PHI=0.5
KP=50e-6
THETA=50e-3
Temp=26.85
COX=3.45e-3
Xpart=0.6

Equation
Eqn1
L=10e-6
W=10e-6
COX=3.45e-3
Cg_norm=COX*W*L
Omega=2*pi*frequency
Y=stoy(S)
Cg=imag(Y[1,1]/Omega)
Cg_2D_plot=PlotVs(Cg/Cg_norm,Vgs)
Cg_3D_plot=PlotVs(Cg/Cg_norm,Vds, Vgs)
Cg_a=PlotVs(Cg,Vgs)



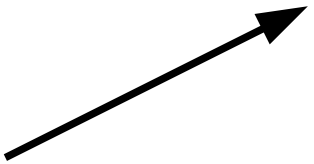




Compact device modelling and circuit macromodelling

Verilog-A code generation

```
`include “disciplines.vams”
`include “constants.vams”
module EKVLC(drain, gate, source, bulk);
inout drain, gate, source, bulk;
electrical drain, gate, source, bulk;
`define attr(txt) (*txt*)
parameter  real L=1e-6 from [1e-20 :inf] `attr(info=”Channel length”);
..
..
real VGprime,VP, n, BETA, X1, If, X2, Ir, Ispecific, Ids;
real nq, XF, Xr, ql, qB,qG;
analog begin
@(initial_model) begin
   Spart=1-Xpart; Qox=COX*W*L; T2=Temp+273.15; vt=`P_K*T2/`P_Q;
end
Vg=V(gate)-V(bullk); Vs=V(source)-V(bulk); Vd=V(drain)-V(bulk);
VGprime=Vg-VTO+PHI+GAMMA*sqrt(PHI);
VP=VGprime-PHI-GAMMA*(sqrt(VGprime+(GAMMA/2)^2)-GAMMA/2);
n=1+GAMMA/(2*sqrt(VP+PHI+4*vt);
BETA=KP*(W/L)*1/(1+THETA*VP);
X1=(VP-Vd)/vt; If=ln(1+limexp(X1/2))^2;
X2=(VP-Vs)/vt; Ir=ln(1+limexp(X2/2))^2;
Ispecific=2*n*BETA*vt*vt;
Ids=Ispecific*(If-Ir);
I(drain,source)  <+ Ids;
```

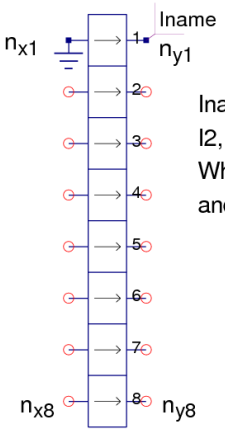
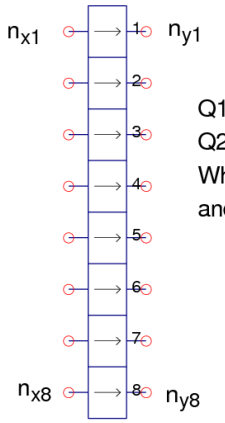


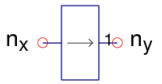
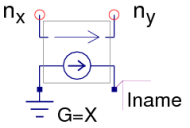
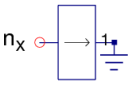
```
nq=1+GAMMA/(2*sqrt(VP+PHI+1e-6);
Xf=sqrt(0.25+If); Xr=sqrt(0.25+Ir)
ql=-nq*( (4/3)*(Xf^2+Xr*Xf+Xr^2)/(Xf+Xr)^2 -1);
if (VGprime > 0)
     qB=-GAMMA*sqrt(VP+PHI+1e-6);
else qB=-VGprime/vt;
qG=-ql-qB;
I(gate, drain)<+ddt(Xpart*qG*Qox;
I(gate, source)<+ddt(Spart*qG*Qox);
I(drain, bulk)<+ddt(Xpart*qB*Qox);
I(source, bulk)<+ddt(Spart*qB*Qox);
end
endmodule
```

Compact device modelling and circuit macromodelling

Relationship between Qucs schematic symbols and Verilog-A code fragments

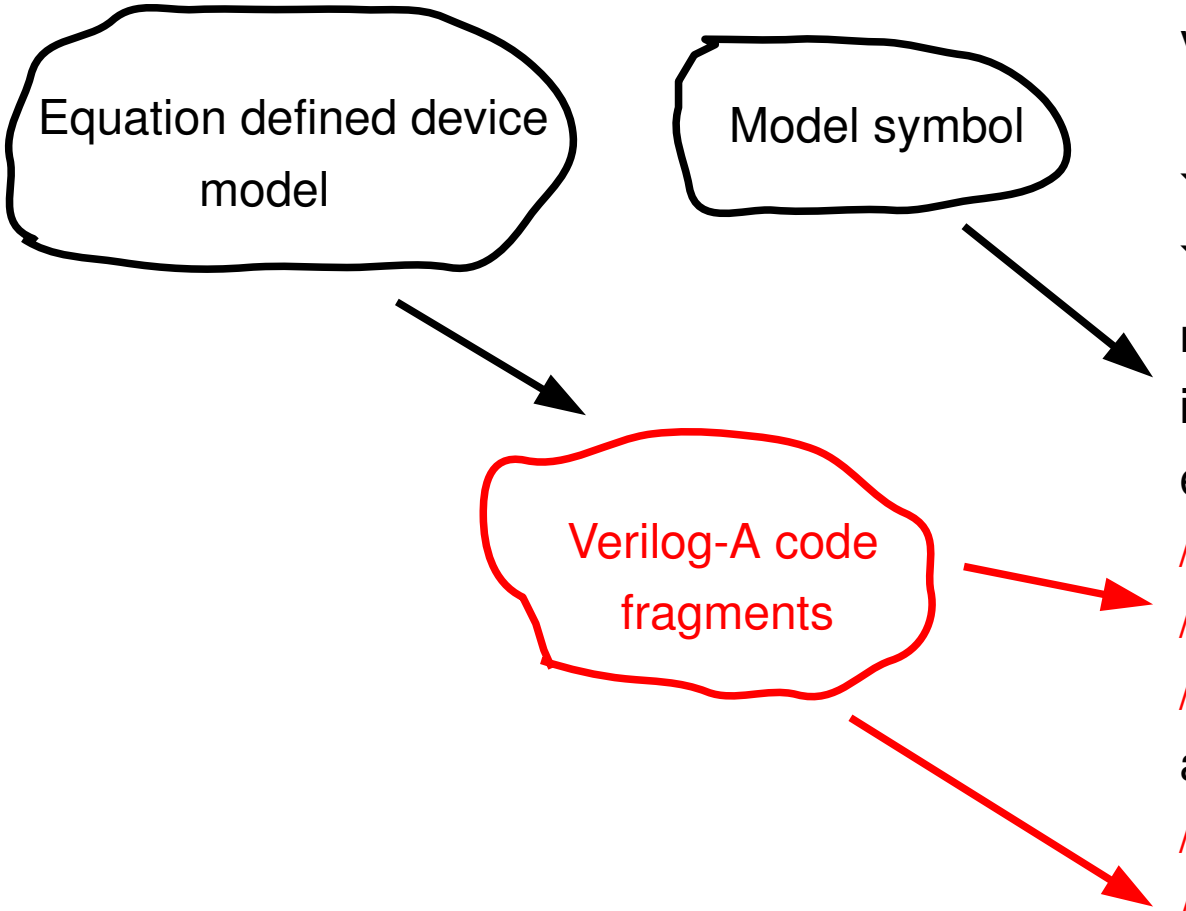
Fundamental EDD blocks

Qucs symbol	Quantity equations	Verilog-A code fragment
	Iname = I1 = f(V2, V3, ... V8) I2, I3, ... I8 = 0 and Q1, Q2, ... Q8 = 0. Where Vm = V(n_{xm}, n_{ym}) or Vm = V(n_{xm}), and 2 ≤ m ≤ 8.	Iname = f(V2, V3, ... V8); Or Iname <+ f(V2, V3, ... V8);
	Q1 = f(V1, V2, ... V8, I1, I2, ... I8) Q2, ... Q8 = 0. Where Vm = V(n_{xm}, n_{ym}) or Vm = V(n_{xm}), and 1 ≤ m ≤ 8.	I(n_{x1}, n_{y1}) <+ ddt(Q1); Or I(n_{x1}, n_{y1}) = ddt(Q1);

	Quantity equations	Verlog-A code fragment
(a) Model initialisation block	Equation Eqn1 con1= ..... con2= ..... con3=	@(initial_model) begin con1 = ...; con2 = ...; con3 = ...; end
(b) Standard resistors		I(n_x, n_y) <+ V(n_x, n_y)/R; I(n_x, n_y) <+ white_noise((FourKT/R, "thermal"); Where FourKT = 4.0 · `P_K · $temperature, and `P_K = 1.3806505e-23 K^{-1}, $temperature is the resistor temperature in Kelvin.
(c) Noise free resistors	 I1 = V1/R = V(n_x, n_y)/R	I(n_x, n_y) <+ V(n_x, n_y)/R;
(d) Voltage controlled current block	 Iname = X · V(n_x, n_y)	Iname = X*V(n_x, n_y);
(e) current to voltage conversion block	 Iname = I1 = V1	Iname = V(n_x);

Compact device modelling and circuit macromodelling

Generating Verilog-A code: Qucs equation defined devices via Verilog-A code fragments to a Verilog-A standardised template



Verilog-A model template

```
`include “disciplines.vams”
`include “constants.vams”
module name (P1, P2, P3, ..... Pn);
inout P1, P2, P3, ....Pn;
electrical P1, P2, P3, ..... Pn;
// Definition of local internal nodes
// Parameter values and descriptions
// Definition of internal variables
analog begin
// Initialisation code
// Quantity equations
// Current contributions
// Noise contributions
end
endmodule
```

Compact device modelling and circuit macromodelling

Improvements/compatibility between Qucs equation defined devices and ADMS Verilog-A code

- From Qucs 0.0.15, version 2.3.0 of the ADMS Verilog-A compiler is required to compile new Verilog-A models
- Qucs XML interface significantly improved with many bug fixes
- Reduction in the number of steps required to link ADMS compiled C++ code to the Qucs simulator and graphical user interface
- First stage in the implementation of a modular Verilog-A to linked C++ model interface implemented – eventual target a fully operating “turn-key” system
- Improved coverage of Verilog-A language, including for example implementation of model code initialisation using the @(initial_model) begin .... end block
- For compatibility with Verilog-A the function ddx has been added to Qucs equation defined devices

Compact device modelling and circuit macromodelling

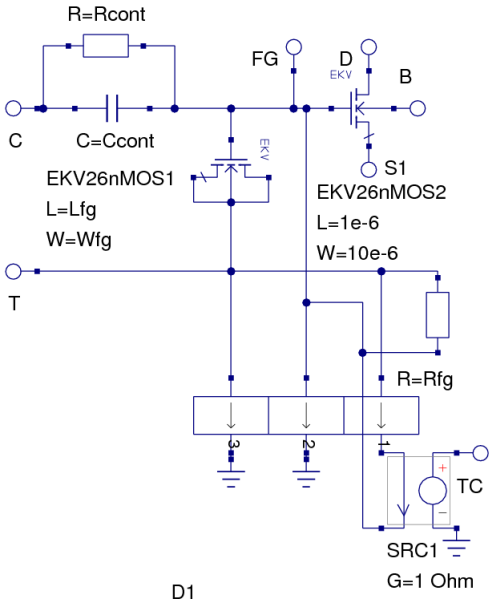
Adding physical effects to equation defined device models: Synapse floating gate MOS tunnelling current example

Tunnelling equation

$$TC = \alpha \cdot \exp\left(\frac{\beta}{Vox}\right)\ A$$

$$\alpha = 9.35e9\ A,\ \beta = -368.04\ V,\ Vox = Vtun - FG\ V.$$

Model

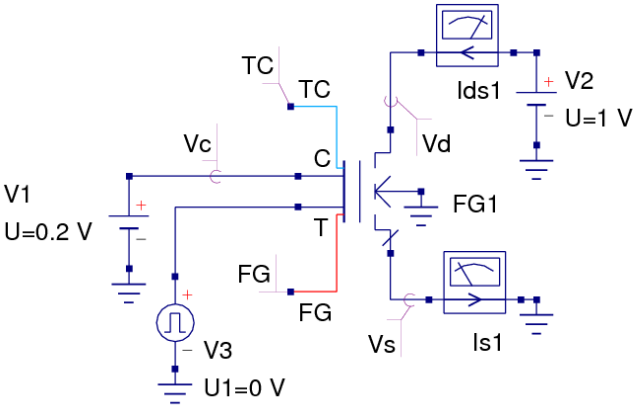


Equation

Eqn1
Lfg=1e-6
Wfg=10e-6
Tor=10000
Cox=3.45e-3
Lcont=10e-6
Wcont=200e-6
Koxide=3
Ccont=Wcont*Lcont*Cox/Koxide
Rcont=Tor/Ccont
Cfg=Wfg*Lfg*Cox
Rfg=Tor/Cfg

D1
I1=(V3 >=V2) ? 9.35e8*exp(-368.04/(V3-V2+1E-20)) : 0
I2=0
I3=0

Symbol and test circuit



transient simulation

TR1
Type=lin
Start=0
Stop=1.5 ms
Points=151
InitialStep=0.1 ns
MinStep=1e-18
reltol=0.001
abstol=1 pA
vntol=1 uV

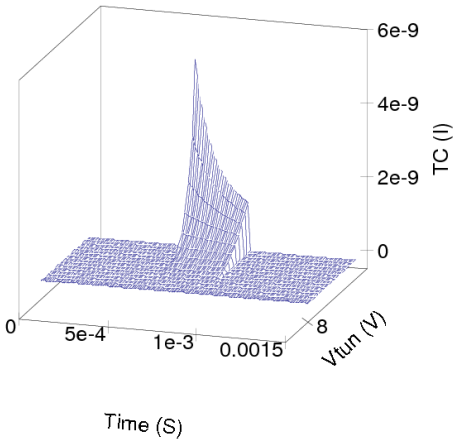
dc simulation

DC1

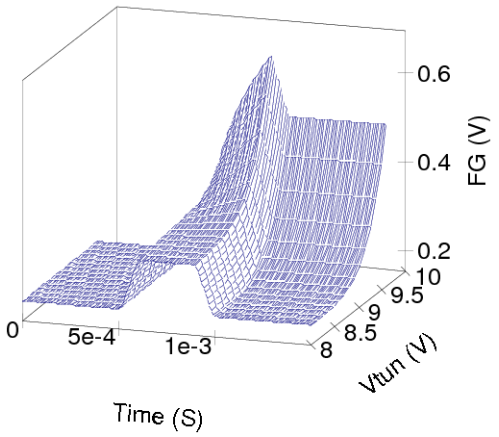
Parameter sweep

SW1
Sim=TR1
Type=lin
Param=Vtun
Start=8
Stop=9.6
Points=15

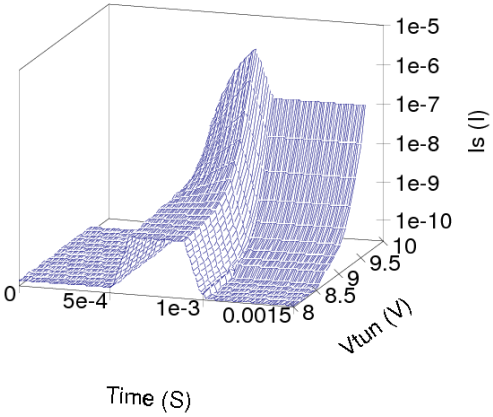
Tunnel current



Floating gate voltage



Source current



Adding non-linear equation defined devices to small signal simulation: introduction to the Qucs radio frequency equation defined device (RFEDD)

- Qucs RFEDD is a frequency dependent equation defined device based on two-port and multi-port electrical network structures
- Two-port RFEDD are similar in structure to the well-known two-port networks commonly employed in the linear analysis of amplifiers and filters
- Multi-port RFEDD allow, for example, modelling of directional couplers, isolators and other multi-port high frequency devices
- Admittance (Y), impedance (Z), scattering (S), hybrid (H), inverse hybrid (G), transmission (A) and scattering transmission (T) two-port devices are implemented
- In contrast to the two-port device, the multi-port RFEDD can only be defined for Y, Z or S networks
- Qucs RFEDD parameters are numerical or algebraic complex numbers. The latter can be functions of numerical constants, variables from Qucs equation blocks, subcircuit parameters, mathematical operators and functions defined in the Verilog-A HDL and the Qucs function library
- The real and imaginary parts of RFEDD parameters may also be functions of small signal
- simulation frequency (F) or operator S ($S = j \,.\, \omega = j \,.\, 2 \,.\, \pi \,.\, F$)

Compact device modelling and circuit macromodelling

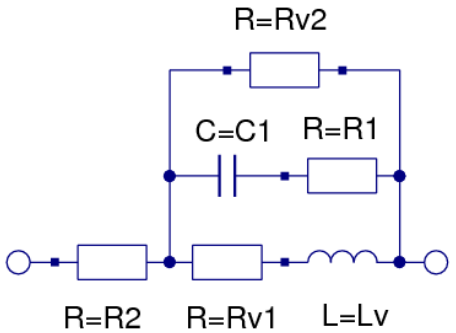
Modelling high frequency components with RFEDD: high-frequency inductance example*

Equations and model

$$Rv1 = K1 \cdot \sqrt{F}, \quad Rv2 = K2 \cdot \sqrt{F}$$

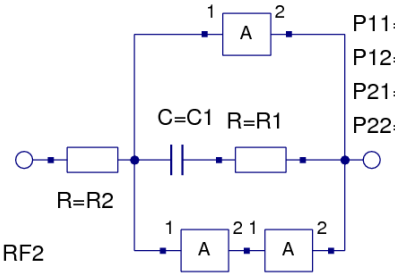
$$Lv = [K3 - K4 \cdot \ln(K5 \cdot F)] \cdot 1e\text{-}6$$

Where K1, K2, K3, K4 and K5 are constants



Qucs RFEDD model

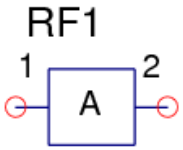
COIL1
R1=6200
R2=1.59
K1=1.49e-5
K2=0.268
K3=1.19
K4=1.4e-2
K5=6.9e-6
C1=0.139e-12



RF1
P11=1
P12=K2*sqrt(F)
P21=0
P22=1

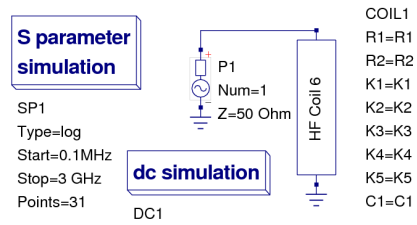
RF2
P11=1
P12=K1*sqrt(F)
P21=0
P22=1

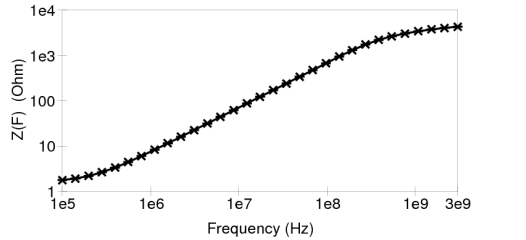
RF3
P11=1
P12=j*2*pi*F*(K3-K4*ln(K5*F))*1e-6
P21=0
P22=1

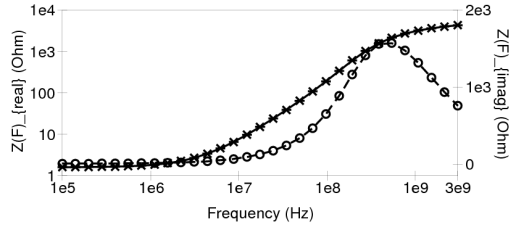


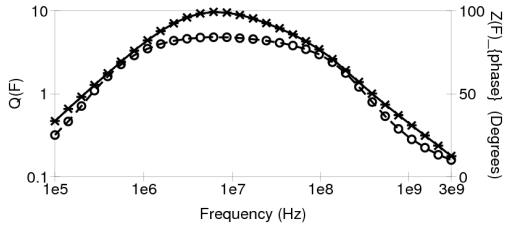
$$[A] = \begin{bmatrix} P11 & P12 \\ P21 & P22 \end{bmatrix} = \begin{bmatrix} 1 & Z(real) + j \cdot Z(imag) \\ 0 & 1 \end{bmatrix}$$

Simulation results



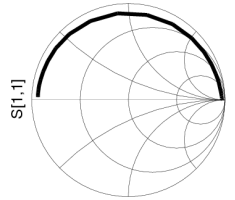






Equation

Eqn1
Zdata=stoz(S)
Z=PlotVs(Zdata[1,1], frequency)
ZR=PlotVs(real(Zdata[1,1]), frequency)
ZI=PlotVs(imag(Zdata[1,1]), frequency)
ZPHASE=PlotVs((180/pi)*arctan(ZI/ZR), frequency)
Q=PlotVs(abs(ZI)/ZR, frequency)



Equation

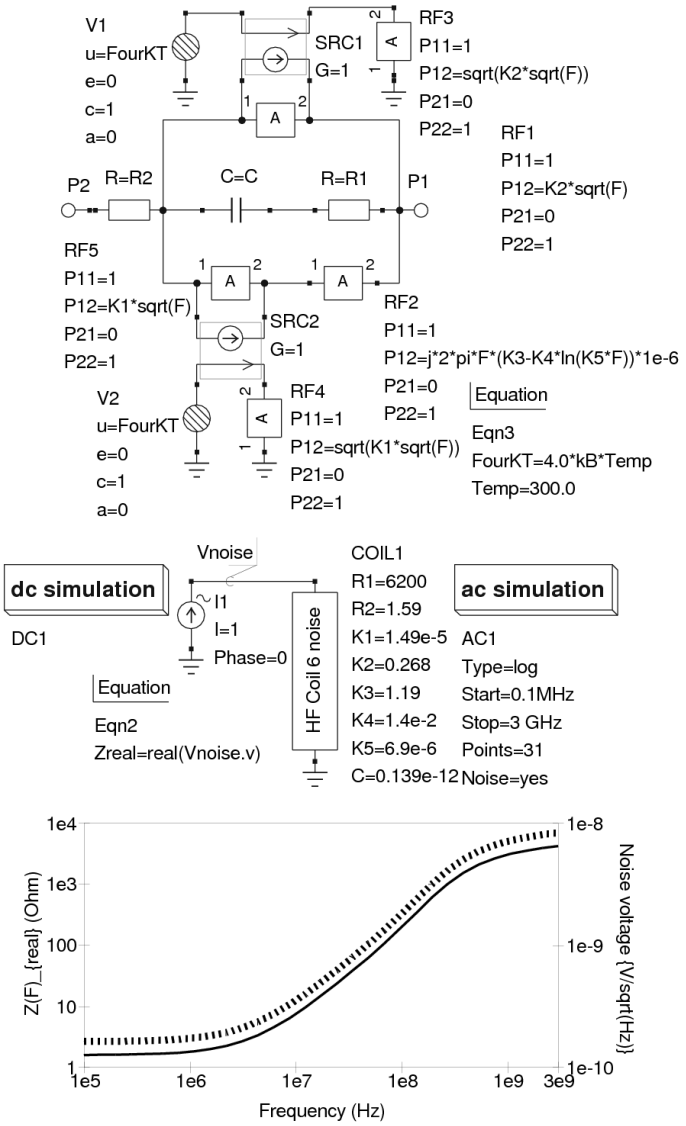
Eqn2
Freq=logspace(100e3, 3e9,31)
Omega=2*pi*Freq
P1=Omega*C1
P2=Omega*Lv
P3=Rv1+Rv2
P4=Rv1*Rv2
P5=R1*Rv1
P6=Lv/C1
P7=Rv2*(P5+P6)
P8=R1*P3
P9=P8+P4+P6
P10=P2-(1/P1)
P11=(P2*R1)-(Rv1/P1)
P12=(P9*P9)+(Rv2*P10+P11)*(Rv2*P10+P11)
ZRcalc=R2+((P7*P9)+ (Rv2*P11)*(Rv2*P10+P11))/P12
PLZRcalc=PlotVs(ZRcalc, Freq)
ZIcalc=((P9*Rv2*P11)-P7*(Rv2*P10+P11))/P12
PLZIcalc=PlotVs(ZIcalc, Freq)
Zcalc=sqrt(ZRcalc*ZRcalc+ZIcalc*ZIcalc)
PLZcalc=PlotVs(Zcalc, Freq)
Qcalc=abs(ZIcalc)/ZRcalc
PLQcalc=PlotVs(Qcalc, Freq)
PHASEcalc=arctan(ZIcalc/ZRcalc)
PLPHASEcalc=PlotVs(PHASEcalc*180/pi, Freq)
Lv=(K3-K4*ln(K5*Freq))*1e-6
C1=0.139e-12
R1=6200.0
R2=1.59
K1=1.49e-5
K2=0.268
K3=1.19
K4=1.4e-2
K5=6.9e-6
Rv1=K1*sqrt(Freq)
Rv2=K2*sqrt(Freq)

*M.E. Brinson and S, Jahn, **Modelling of high-frequency inductance with Qucs non-linear radio frequency defined devices**, International Journal of Electronics, Vol. 96, No. 3, March 2009, pp. 307-321.

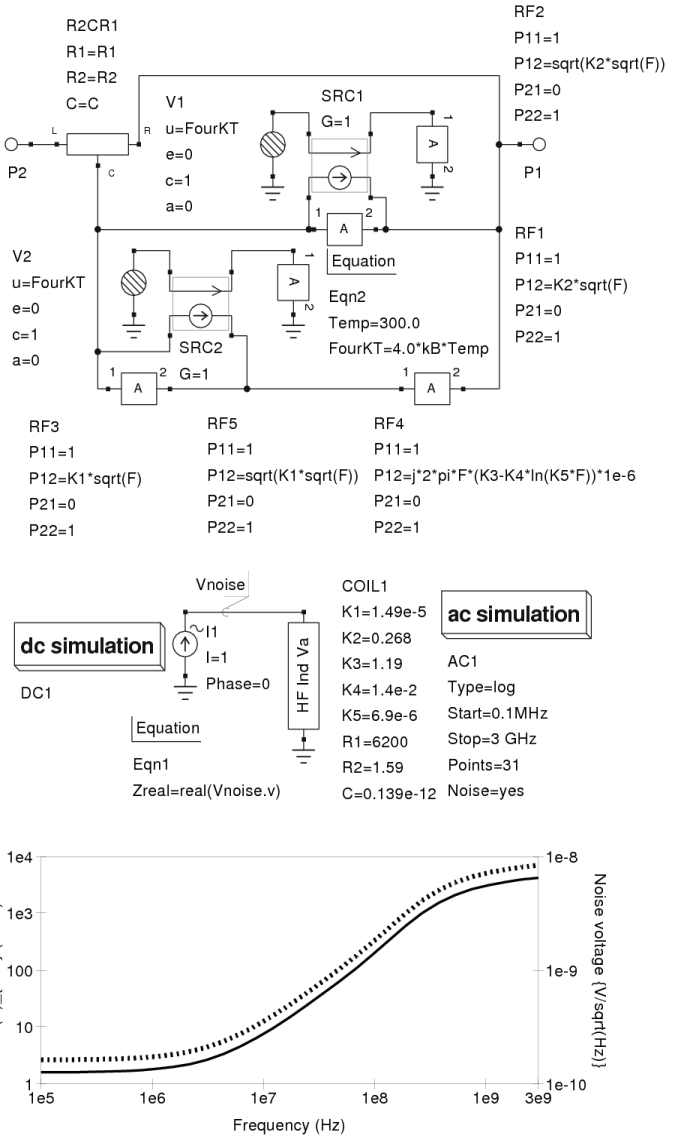
Compact device modelling and circuit macromodelling

Modelling high frequency components with RFEDD: high-frequency skin effect noise

Noise model: standard
plus RFEDD non-linear components



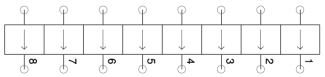
Noise model: Verilog-A block
plus RFEDD non-linear components

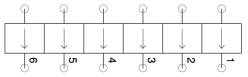


Compact device modelling and circuit macromodelling

Parameters for a general purpose compact operational amplifier macromodel with typical UA741 values as default

Name	Symbol	Description	Unit	Default
IB	I_B	Input bias current	A	80e-9
IB_TC	I_BTC	Input bias temp. coeff.	A $^oC^{-1}$	-1e-9
VOFF	V_{OFF}	Input offset voltage	V	7e-4
VOFF_TC	$V_{OFF}TC$	Input offset voltage temp. coeff.	V $^oC^{-1}$	1e-5
IOFF	I_{OFF}	Input offset current	A	1e-8
IOFF_T	$I_{OFF}TC$	Input offset current temp. coeff.	A $^oC^{-1}$	-2e-10
RD	R_D	Differential input resistance	Ω	2e6
RD_TC	R_DTC	Differential input res. temp. coeff.	$^oC^{-1}$	1.82e4
CD	C_D	Differential input capacitance	F	1.4e-12
AOL_0	AOL0	Differential gain at DC	dB	105
GBP	GBP	Differential unity gain frequency	Hz	1e6
FP2	FP2	Differential gain second pole freq.	Hz	3e6
CMRR_0	CMRR0	DC common-mode rejection ratio	dB	90
FCM	FCM	Common-mode gain zero frequency	Hz	200
CMR	CMR	Common-mode range voltage	V	12
PSRT	PSRT	Positive signal slew rate	Vs^{-1}	5e5
NSRT	NSRT	Negative signal slew rate	Vs^{-1}	5e5
RO	R_O	Output resistance	Ω	75
ILMAX	IL_{MAX}	Maximum DC output current	A	3.4e-2
ILMAX_TC	$IL_{MAX}TC$	Max. DC output current temp. coeff.	A $^oC^{-1}$	-7.1e-5
VLIMP	VLIMP	Maximum positive output voltage	V	14
VLIMN	VLIMN	Maximum negative output voltage	V	-14
Tnom	Tnom	Circuit parameter measurement temp.	^oC	26.85
Temp	Temp	Circuit temperature	^oC	26.85
SFACT1	SFACT1	Current limit scale factor	V	0.85
SFACT2	SFACT2	Common-mode range scale factor	V	10
SFACT3	SFACT3	Differential voltage gain scale factor		-100
PWD	PWD	Power consumption	W	50e-3





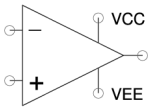
```
D1
Type=explicit
I1=(V1>0) ? 5e-16*(limexp(V1/VT)-1) : -5e-16*(limexp(-V1/VT)-1)
Q1=0
I2=0
Q2=0
I3=V3
Q3=CP2*V3
I4=(V4 > (VLIMP) ) ? V4/(AOL_0*limexp(SFACT3*( (V4/VLIMP)-1)) + 500)  :  (V4 < VLIMN)  ? V4/(AOL_0*limexp( SFACT3*((V4/VLIMN) - 1)) + 500) : V4/AOL_0
Q4=CP1*V4
I5=(V5 > SLRTP) ? SLRTP : (V5 < -SLRTN) ? -SLRTN : V5
Q5=0
I6=0
Q6=0
I7=CMR*tanh(V7/SFACT2)
Q7=0
I8=(V3 >= VLIMP) ? VLIMP : (V3 <= VLIMN) ? VLIMN: V3
Q8=0
```

```
D2
I1=0
I2=(V1 > 0) ? V1 : 0
I3=(V1 < 0) ? -V1 : 0
I4=PWD/((V5-V6)+1e-4)
I5=0
Q5=0
I6=0
Q6=0
```

EDD quantity equations

Equation based compact Macromodels:

operational amplifier example*



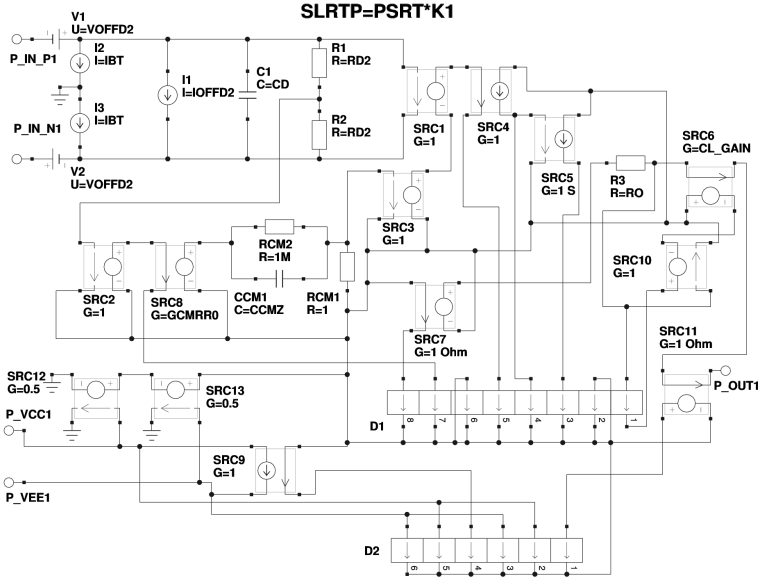
Symbol+parameters

Equations

```
SUB1
GBP=1e6
PSRT=0.5e6
NSRT=0.5e6
CMRRDC=90.0
FCM=200
AOLDC=106.0
FP2=3e6
RO=75
CD=1.4e-12
RD=2e6
IOFF=20e-9
IB=80e-9
VOFF=0.7e-3
ILMAX=34e-3
VLIMP=14
VLIMN=-14
SFACT1=0.85
SFACT2=10
CMR=12
Temp=26.85
IB_TC=-1e-9
VOFF_TC=10e-6
Tnom=26.85
IOFF_TC=-200e-12
RD_TC=18.2e3
ILMAX_TC=-0.071e-3
SFACT3=-100
PWD=54e-3
```

Equation

```
Eqn1
GCMRR0=1e6/CMRR_0
AOL_0=10^(AOLDC/20)
CMRR_0=10^(CMRRDC/20)
ILMAXT=ILMAX+ILMAX_TC*(T-TN)
VOFFT=VOFF+VOFF_TC*(T-TN)
RDT=RD+RD_TC*(T-TN)
IBT=IB+IB_TC*(T-TN)
IOFFT=IOFF+IOFF_TC*(T-TN)
T=Temp+273.15
TN=Tnom+273.15
CL_GAIN=SFACT1/ILMAXT
K1=1/(2*pi*GBP)
VT=vt(300)
CP1=K1
CP2=1/(2*pi*FP2)
CCMZ=1/(2*pi*1e6*FCM)
VOFFD2=VOFFT/2
IOFFD2=IOFFT/2
RD2=RDT/2
SLRTN=NSRT*K1
SLRTP=PSRT*K1
```

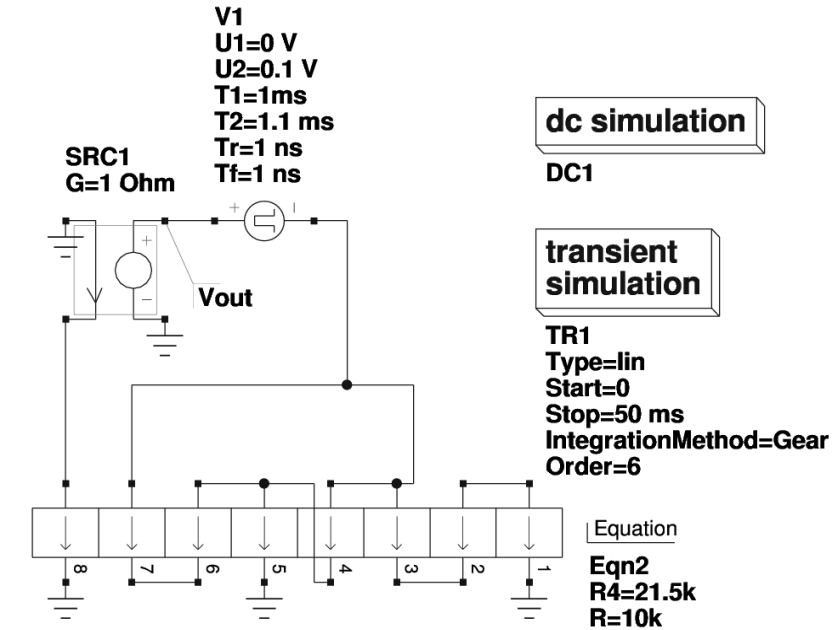


*M.E. Brinson and S, Jahn, **Compact macromodelling of operational amplifiers with equation defined devices**, International Journal of Electronics, Vol 96 (2), February 2009. pp. 109-122.

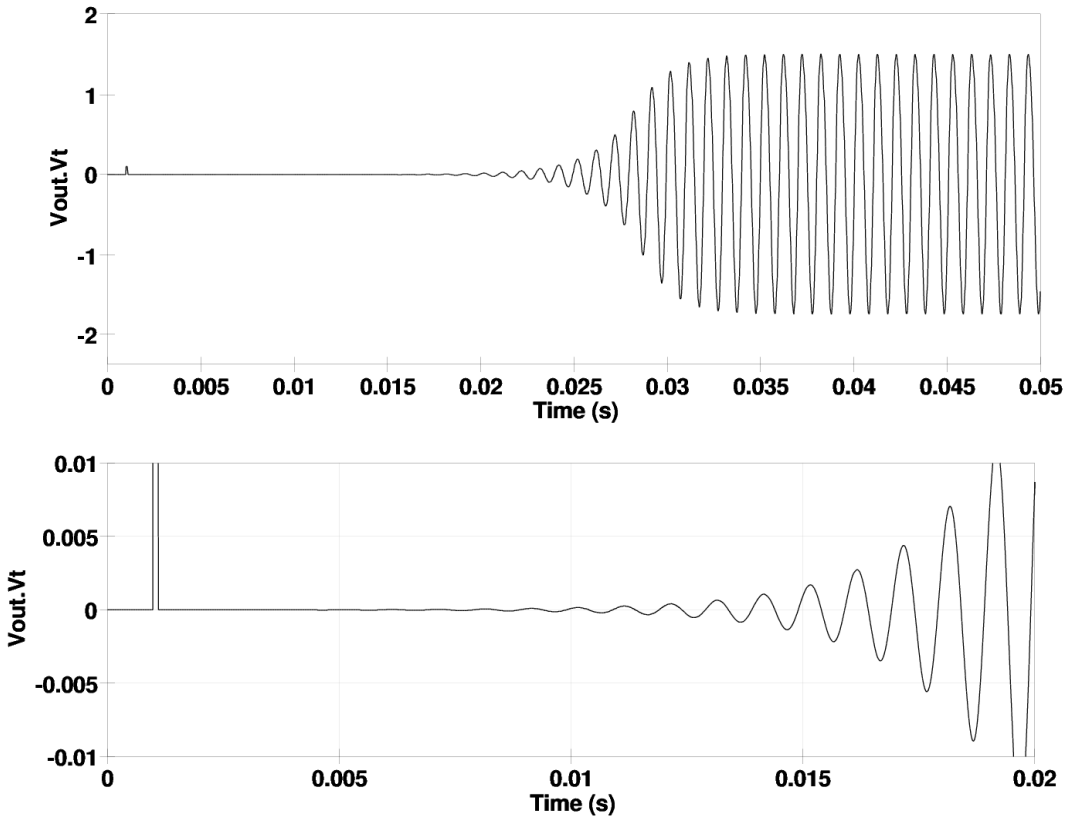
Compact device modelling and circuit macromodelling

Equation defined device modelling of circuit blocks

Oscillator Circuit



Output voltage plotted against time

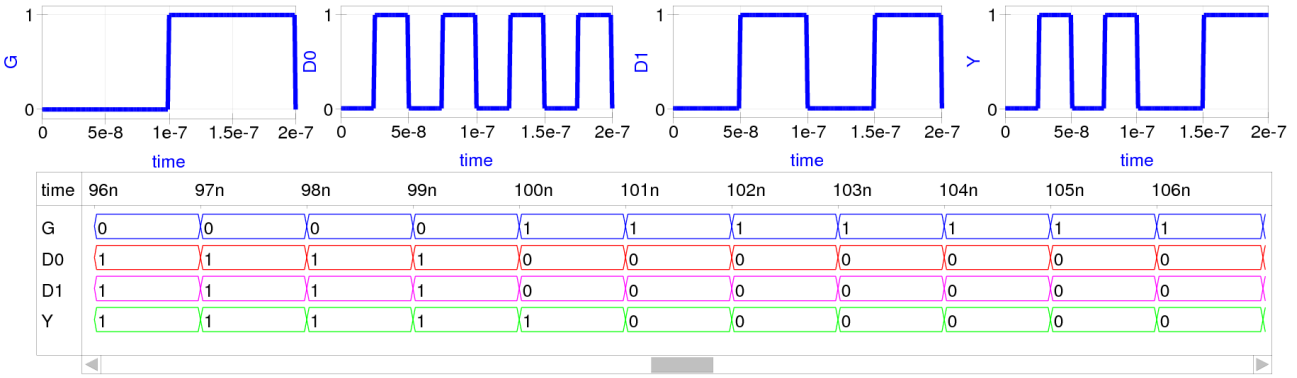


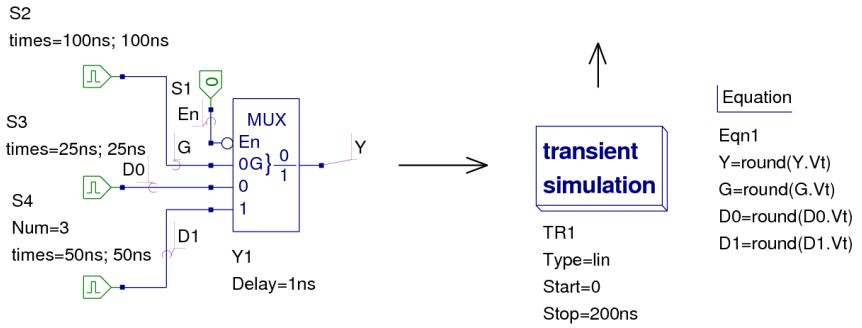
Circuit equations

Compact device modelling and circuit macromodelling

Digital simulation: one symbol -> multi-hardware description language code generation

An unusual application of Verilog-A



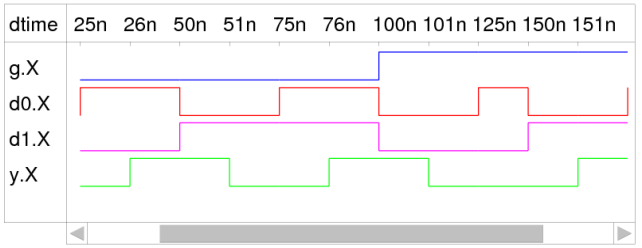


VHDL

Verilog

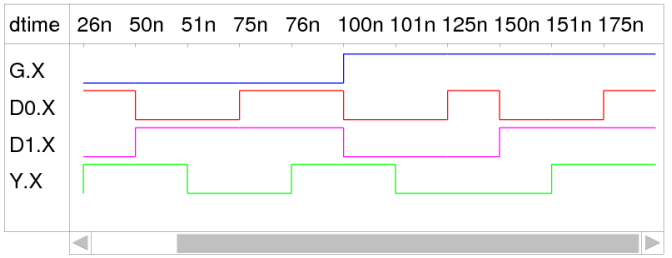
digital simulation

Digi1
Type=TimeList
time=200 ns
Model=VHDL



digital simulation

Digi1
Type=TimeList
time=200 ns
Model=Verilog

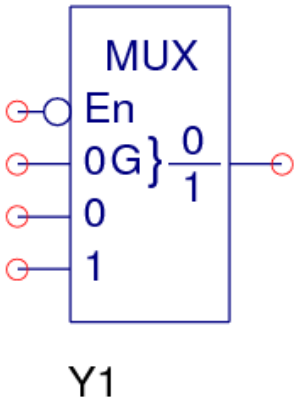


Compact device modelling and circuit macromodelling

Qucs HDL code generation

```
// Y1 mux2to1
 assign  netY = net_regY1netY;
 reg     net_regY1netY=0;
 always @ (netEn or netG or netD0 or netD1 )
  net_regY1netY <=   #1000 ( netD1 && netG )  || ( netD0 &&  ( ~netG ) )  ;
```

Verilog



Transient

VHDL

```
Y1 : process (netEn , netG , netD0 , netD1)
        begin
            netY <= ( not netEn) and ( ( netD1 and netG ) or  ( netD0 and ( not netG ) ) ) after 1 ns;
    end process ;
```

```
`include "disciplines.vams"
`include "constants.vams"
module mux2to1 (EN, A, D0, D1, Y);
 inout EN, A, D0, D1, Y;
 electrical EN, A, D0, D1, Y;
 electrical n1, n2;
//
 `define attr(txt) (*txt*)
 parameter real TR=6 from [1.0:20.0]
     `attr(info="tranfer function high scaling factor");
 parameter real Delay = 1e-9 from [0: inf]
    `attr(info="output delay" unit="s");
//
 real Rd, Ccc, In1;
//
analog begin
@(initial_model)
  begin
    Rd = 1e3;
    Ccc= Delay*1.43/Rd;
  end
In1 = (1-V(EN))*(V(D1)*V(A)+V(D0)*(1-V(A)));
I(n1) <+ -0.5*(1+tanh(TR*(In1-0.5)));
I(n1) <+ V(n1);
I(n1, n2) <+ V(n1,n2)/Rd;
I(n2) <+ ddt(Ccc*V(n2));
I(Y)  <+ -V(n2);
I(Y) <+ V(Y);
end
endmodule
```

Summary and future work

Summary

The hierarchical approach to compact semiconductor device modelling and circuit macromodelling outlined in this presentation stresses the role equation defined device modelling techniques will take on as GPL simulator technology evolves in the future.

Future work

- Add more MOSFET models – for example BSIM3, BSIM4 and PSP
- Extend the range of optoelectronic device models
- Improve the Verilog-A and Qucs interface documentation
- Further develop the Verilog-A modular “turn key” capabilities
- Cooperate with other “modellers” to add emerging technology device models to Qucs
- General development to reduce bugs and add facilities listed in the package to-do lists