Current Conveyor Macromodels for Wideband RF Circuit Design

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***Abstract*—A high percentage of analogue integrated circuit designs use voltage domain signal processing techniques. Given the fact that integrated circuit current conveyors are high bandwidth current processing devices, often with superior RF performance when compared to comparable voltage domain devices, it is surprising that the number of current mode integrated circuits available, as standard of-the-shelf industrial items, is so small. This paper introduces equation-defined device and Verilog-A synthesis approaches to the macromodelling of current conveyor integrated circuits. To illustrate the proposed modelling techniques the properties of a number of modular behavioural level current conveyor macromodel cells are described and their performance compared. The material presented is intended for analogue device modellers and circuit designers who wish to simulate current domain integrated circuit designs. It also demonstrates how synthesized Verilog-A functional blocks can be derived from equation-defined device and conventional component subcircuits to form functional, computationally efficient current conveyor macromodels.**

***Index Terms*—Qucs, current conveyors, compact semiconductor device modelling, equation-defined devices, macromodels, Verilog-A model synthesis.**

I. Introduction

Behavioural modelling of integrated circuits with macromodels has evolved into an established modelling technique [1], particularly after Boyle et al. [2] published a computationally efficient operational amplifier macromodel that included a mixture of first and second order device charcteristics. A macromodel in this context implies a collection of linear and non-linear simulation component models, combined as a subcircuit, where the simulated electrical signals at the subcircuit input-output pins appear to be similar to those generated by a physical device. Adding Qucs equation-defined device (EDD) technology [3,4] to behavioural macromodelling introduces a powerful algebraic capability for specifying the non-linear properties of semiconductor devices and integrated circuits. This approach has become more firmly entrenched with the adoption of the Verilog-A hardware description language for compact semiconductor device modelling [5]. Although Verilog-A compact device modelling is well established for compact semiconductor device modelling, its use for conventional circuit macromodelling is often assumed or implied by the nature of the hardware description language. This paper proposes a structured route for compact macromodelling from original specification through preliminary model design, with equation-defined defined device technology, to final optimized Verilog-A macromodel, via Verilog-A model synthesis. To demonstrate the proposed macromodelling procedure the properties and relationships between current conveyor macromodels, at different levels of circuit abstraction, are described. A number of Qucs [6] simulation test-bench circuits, plus typical simulation data are also included, and their performance compared.

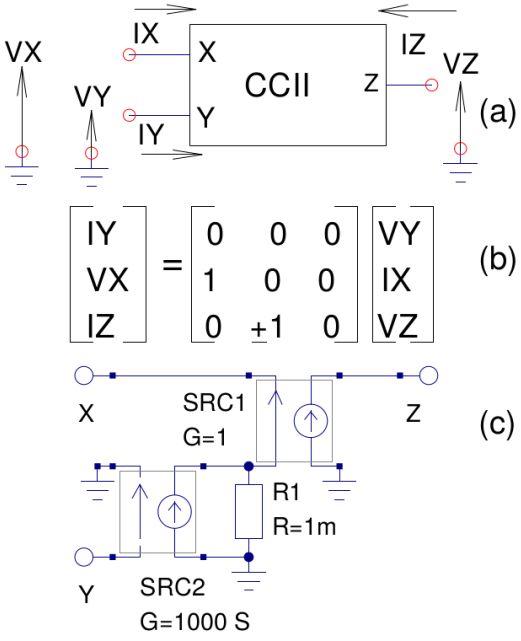

Fig. 1. Specification for a second generation current conveyor macromodel: (a) Qucs schematic symbol, (b) port current/voltage relationships in matrix form, (c) a first level ideal macromodel.

II. Current Conveyor Principles

The first generation current conveyor (CCI) was introduced by Sedra and Smith in 1968 [7] as a three port circuit building block for analogue signal processing. In 1970 the same authors [8] reported an improved second generation device (CCII) which overcame a number of limitations inherent in the original device specification. Today the CCII current conveyor is an RF current mode device which finds application in wideband amplification, filtering and other signal processing

functions [9,10]. An additional source of reference for current conveyor principles and RF applications can be found in the IEE publication edited by Toumazou, Lidgy and Haigh [15]. A schematic symbol for a CCII is shown in Fig. 1 (a). The ideal current/voltage relationships at the device ports are $IY = 0$ (high input impedance at Y terminal $\rightarrow \infty$), $VX = VY$ (low input impedance at X terminal $\rightarrow 0$) and $IZ = \pm\ IX$ (high output impedance at Z terminal $\rightarrow \infty$). These relationships can be expressed in the matrix form given in Fig. 1 (b), where the $\pm$ sign in equation $IZ = \pm IX$ signifies the direction of IZ current flow in comparison to current IX: called $CCII+$ when $IZ = IX$ and $CCII-$ when $IZ = -IX$. Fig. 1 (c) introduces a level one macromodel of a CCII device, where the electrical properties of the input and output ports are set by linear voltage controlled current source SRC2, which functions as a voltage follower, and by current controlled current source SRC1, which acts as a current follower. The level one CCII macromodel represents an ideal device which has an infinite signal frequency bandwidth, see the current mode amplifier shown in Fig.2.

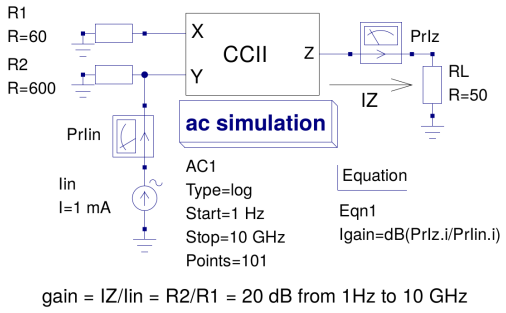

Fig. 2. A current conveyor current amplifier: $gain = IZ/Iin = R2/R1$.

III. QUCS EDD MACROMODELS AT DIFFERENT LEVELS OF CIRCUIT ABSTRACTION

For integrated circuit macromodels to be useful design aids they must be stable and function without convergence problems in all circuit simulation domains, including the steady state AC large signal Harmonic Balance and transient shooting method domains. They should also be defined at different levels of circuit abstraction from ideal to non-linear, allowing choice of macromodel to meet the requirements of a given circuit simulation. A significant improvement in macromodel simulation run-time performance can sometimes result with circuit simulators which include Verilog-A synthesizers/compilers that generate C++ code level models from Verilog-A modules [11,12]. In this paper five macromodel circuit abstraction levels are proposed, four at circuit schematic level, ideal to non-linear, and one at Verilog-A module level, see Table I.

TABLE I
MACROMODEL LEVELS OF CIRCUIT ABSTRACTION.

Level	Model Abstraction	Properties
1	Ideal	Fundamental current transfer characteristic
2	Linear DC	Level 1 plus input and output resistance and gain parameters
3	Small signal AC	Level 2 plus internal capacitance
4	Large signal non-linear	Level 3 plus nonlinear device parameters, including offset current and saturation effects
5	Verilog-A	Verilog-A module representation of macromodels levels 1 to 4

A. Level 2 Current Conveyor Macromodel

The simple level one macromodel shown in Fig. 1 (c) assumes that the properties of a current conveyor are ideal with controlled sources that have matched unity gain transfer functions and that the X port input resistance is zero and that the Y and Z ports have infinite input and output resistance, respectively. In reality a real current conveyor has properties which are far from ideal. Fig. 3 introduces the macromodel for the next level of circuit extraction. This adds port resistors RX, RY and RZ and the gain parameters $P1$ and $P2$. The latter two determine how close the voltage and current follower transfer functions are to unity. The combination of RX and $EDD - D1$ sense current IX and generate conveyor current IZ. The graph of gain against frequency illustrated in Fig. 3 is for data obtained with the simulation test bench shown in Fig. 2 and $R1 = 10\Omega$ to compensate for port IX resistance increase to 50Ω.

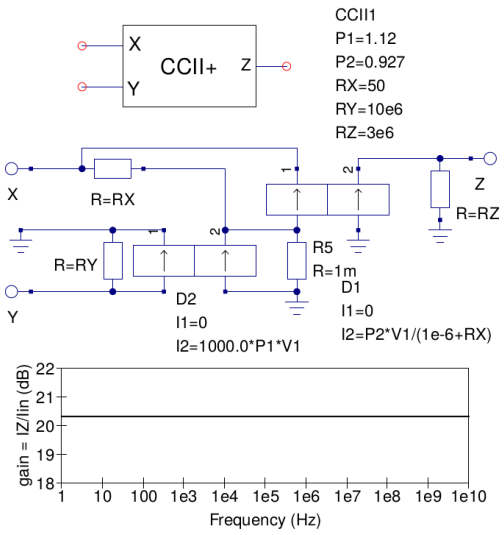

Fig. 3. Level 2 current conveyor macromodel: $RX = 50\Omega$, $RY = 10\text{M}\Omega$, $RZ = 3\text{M}\Omega$, $P1 = 1.12$ and $P2 = 0.927$.

B. Level 3 Current Conveyor Macromodel

The level one and level two CCII macromodels have an infinite frequency bandwidth. This, of course, is not true for a real current conveyor integrated circuit. In reality all three

device ports have a finite capacitance connected to ground which causes the current gain frequency response to decrease at high frequencies. A level three CCII+ macromodel is shown in Fig. 4. With the port capacitors set to 4.5 pF, small signal AC simulation indicates that the current amplifier has two poles between 50 MHz and 800 MHz resulting in 40 dB per decade roll-off in the gain response at frequencies above 1 GHz. Frequency domain analysis of the level three CCII+ macromodel yields the following transfer function equations

$$V(n1) = \frac{R2 \cdot RY \cdot P1 \cdot Iin}{(R2 + RY) \cdot [1 + j \cdot \frac{\omega}{\omega_{yp}}]} \tag{1}$$

$$IX = \frac{[1 + j \cdot \frac{\omega}{\omega xz}] \cdot V(n1)}{(R1 + RX) \cdot [1 + j \cdot \frac{\omega}{\omega xp}]} \tag{2}$$

$$IZ = \frac{P2 \cdot IX}{[1 + j \frac{\omega}{\omega zp}]} \tag{3}$$

where $V(n1)$ is the voltage at node $n1$, see Fig. 4, and

$$\omega yp = \frac{(R2 + Ry)}{CY \cdot R2 \cdot RY} \tag{4}$$

$$\omega xz = \frac{1}{CX \cdot R1} \tag{5}$$

$$\omega xp = \frac{(R1 + RX)}{CX \cdot R1 \cdot RX} \tag{6}$$

$$\omega zp = \frac{(RZ + RL)}{CZ \cdot RZ \cdot RL} \tag{7}$$

With $R1$ = 10 Ω and RX = 50 Ω, $\omega xz \approx \omega xp$ indicating that pole-zero cancellation takes place in the expression for IX, yielding

$$\frac{IX}{Iin} = \frac{P1 \cdot P2 \cdot R2 \cdot RY}{(R1 + RX) \cdot (R2 + RY) \cdot [1 + j \cdot \frac{\omega}{\omega yp}] \cdot [1 + j \cdot \frac{\omega}{\omega zp}]} \tag{8}$$

where $fyp = \omega yp/(2 \cdot \pi)$ = 707.36 MHz and $fzp = \omega zp/(2 \cdot \pi)$ = 58.94 MHz for the CCII+ parameter values listed in the caption to Fig. 4 and RL = 50Ω. Qucs-0.0.19-S/Ngspice .PZ pole-zero analysis confirms the three pole and the single zero frequencies, see Table II.

TABLE II
LEVEL THREE CCII MACROMODEL POLE-ZERO FREQUENCIES.

Pole number	ω_p **(radians)**	f_p **(Hz)**
1	-2.67e10	-4.25e9
2	-4.44e9	-707.66e6
3	-3.70e8	-58.89e6
Zero number	ω_z **(radians)**	f_z **(Hz)**
1	-2.22e10	-3.53e9

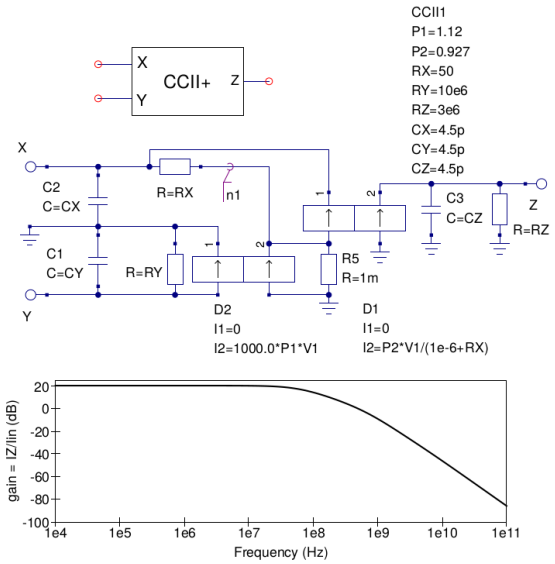

Fig. 4. Level 3 current conveyor macromodel: RX = 50Ω, RY = 10MΩ, RZ = 3MΩ, $P1$ = 1.12 and $P2$ = 0.927, CX = CY = CZ = 4.5pF.

C. Level 4 Current Conveyor Macromodel

Level four current conveyor macromodels are applicable where non-linear circuit properties have a critical effect on simulation accuracy. One extension to the level three CCII+ macromodel, which is necessary to simulate large signal performance correctly, is a circuit extension that handles CCII+ operation at signal levels approaching, and above or below, DC supply voltages. An example of a level four CCII+ macromodel is shown in Fig. 5 where the voltage follower output voltage $V(n1)$ is modelled by a $tanh$ limiter function given by

$$V(n1) = P1 \cdot V(Y) \cdot (1.0 - tanh(abs(V(Y)/(Scale \cdot VMAX)) \tag{9}$$

where $-VMAX$ and $+VMAX$ represent the CCII+ negative and positive DC supply voltages, and $Scale$ is a scaling factor which determines the degree of limiting at voltages greater than $+VMAX$ or less than $-VMAX$. A suitable value for parameter $Scale$ can be found by simulating the performance of a unity gain CCII+ current amplifier with $VMAX$ kept

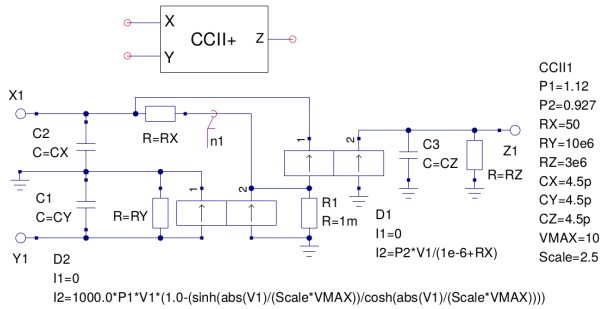

Fig. 5. Level 4 current conveyor macromodel: DC power supply voltage $VMAX$ = 10V and scale factor $Scale$ = 2.5.

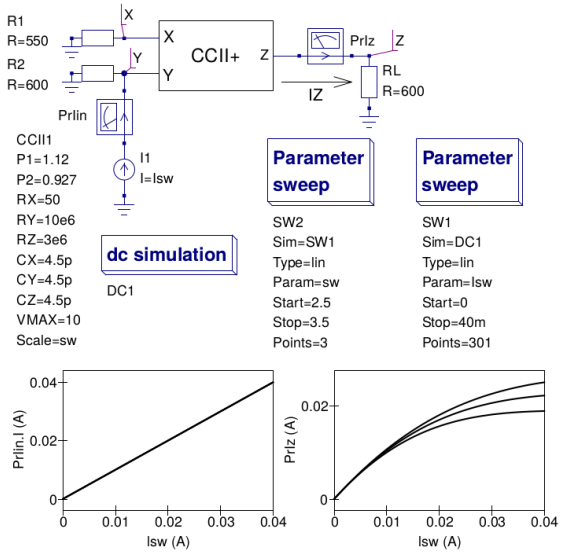

Fig. 6. Unity gain current amplifier: DC power supply voltage $VMAX$ = 10V and 2.5 $>= Scale <=$ 3.5.

constant and $Scale$ scanned over finite range, see Fig. 6. When parameter $Scale$ is set to a large value, for example $\geq$ 10, the level four CCII+ macromodel reverts to the level three macromodel.With $Scale$ = 2.7 the CCII+ current amplifier peak output current IZ and peak output voltage $V(Z)$ are effectively clamped to 20mA and 10V respectively, see Fig. 7.

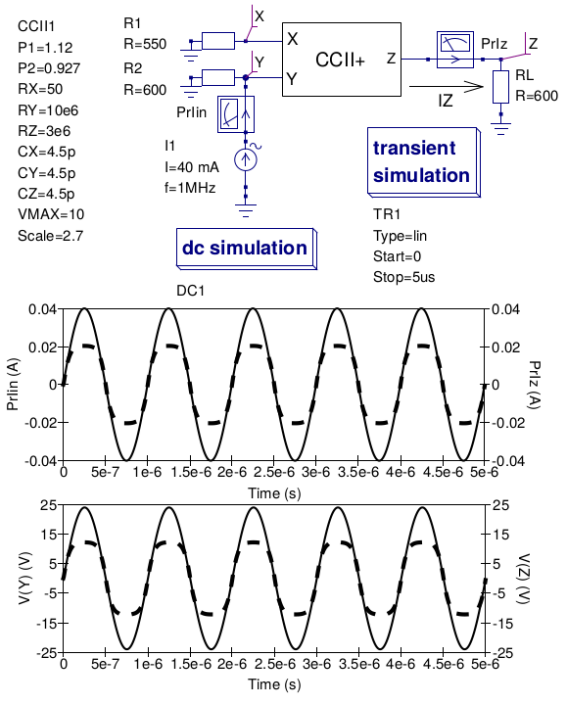

Fig. 7. Transient simulation of a unity gain CCII+ current amplifier: test circuit and simulation plotted current and voltage data; left side scale solid line and right side scale dotted line.

IV. Verilog-A Current Conveyor Macromodels

In many design projects conventional macromodels are more than adequate for simulating circuit performance. However, as the size of a macromodel circuit increases, or if its circuit is very non-linear, simulation may require significant amounts of computing time. Replacement of complex circuit level macromodels by low level C or C++ code models synthesized from the Verilog-A hardware description language can sometimes reduce circuit simulation time, significantly. However, this statement is not meant to imply that macromodel levels one to four are redundant but rather that they are simply stages in a structured process for generating computationally efficient Verilog-A macromodels. Recent developments in Qucs compact device modelling capabilities have shown that Verlog-A modules can be synthesized automatically from circuit schematics [13,14], yielding a direct link between the level one to level four CCII macromodels and compiled C++ macromodels. The Qucs Verilog-A model synthesiser allows macromodels or compact device models to be constructed from the Qucs and SPICE components listed in Table III. These are a mixture of linear passive components R, C and L, linear controlled sources VCCS, CCCS, VCVS and CCVS, non-linear components EDD and B, an algebraic equation block EQN and subroutine features PIN, SUB and SPARAM. The synthesized Verilog-A module code for a level five CCII+ macromodel is listed in Fig. 8. The Qucs Verilog-A synthesizer automatically adds white noise current to each macromodel resistor. However, to simulate CCII+ noise correctly additional noise contributions must be added to the macromodel voltage and current followers. This can be done using Qucs INOISE generators with their shot and flicker noise outputs set at appropriate values.

TABLE III
Built-in Qucs/SPICE components for constructing Verilog-A synthesized macromodels and device models.

Component code	Type	Qucs	SPICE
R	Resistor (linear)	X	
C	Capacitor (linear)	X	
L	Inductor (linear)	X	
VCCS	Voltage controlled voltage source	X	
CCCS	Current controlled current source	X	
VCVS	Voltage controlled voltage source	X	
CCVS	Current controlled voltage source	X	
EDD	Equation-Defined Device	X	
B	B type current source		X
EQN	Equation block	X	
INOISE	Current noise source	X	
PIN	Subcircuit pin	X	
SUB	Subcircuit	X	
SPARAM	Subcircuit parameter	X	

V. A Comparison of Current Conveyor Behavioural and Synthesized CCII+ Macromodels in the AC Domain

Illustrated in Fig. 9 are two wideband CCII+ instrumentation amplifiers connected to simulate differential and common mode output voltage signals generated from a common resistive signal source. The instrumentation amplifiers

```
`include "disciplines.vams"
`include "constants.vams"
module Level4_CCII+(X, Y, Z);
inout X, Y, Z;
electrical n1, Y, X, Z;
parameter real P1=1.12;     parameter real P2=0.927;
parameter real RX=50;       parameter real RY=10e6;
parameter real RZ=3e6;      parameter real CX=4.5p;
parameter real CY=4.5p;     parameter real CZ=4.5p;
parameter real VMAX=10;   parameter real Scale=2.5;
analog begin
@(initial_model) begin   end
I(n1) <+ -((-V(n1))/( 1m ));
I(n1) <+ white_noise( 4.0*`P_K*( 26.85 + 273.15) /
       ( 1m ), "thermal" );
I(Y) <+ V(Y)/( RY );
I(Y) <+ white_noise( 4.0*`P_K*( 26.85 + 273.15) /
        ( RY ), "thermal" );
I(Z) <+ -(P2*V(n1,X)/(1e-6+RX));
I(X,n1) <+ V(X,n1)/( RX );
I(X,n1) <+ white_noise( 4.0*`P_K*( 26.85 + 273.15) /
        ( RX ), "thermal" );
I(Z) <+ -((-V(Z))/( RZ ));
I(Z) <+ white_noise( 4.0*`P_K*( 26.85 + 273.15) /
       ( RZ ), "thermal" );
I(Y) <+ ddt( V(Y) * CY );
I(X) <+ ddt( (V(X)) * CX );
I(Z) <+ ddt( (V(Z)) * CZ );
I(n1) <+ -(1000.0*P1*V(Y)*(1.0-(sinh(abs(V(Y))/(Scale*VMAX))/
         cosh(abs(V(Y))/(Scale*VMAX)))));
end
endmodule
```

Fig. 8. Qucs Verilog-A module code for a level 5 macromodel synthesized from the level 4 $CCII+$ macromodel given in Fig. 5: for clarity long Verilog-A statements have been spread over two consecutive lines.

are constructed using six level four CCII+ current conveyor macromodes of the type shown in Fig. 5. The instrumentation amplifier gain is given by $R1/R2$ and is set to unity in Fig. 9. The differential gain and common mode gain graphs drawn in Fig. 9 are typical for an instrumentation amplifier where the common mode rejection ratio (CMRR) has a high dB value at low frequencies then reduces at 20dB per decade till a corner frequency is reached where a pole in the CMRR frequency response causes the low frequency zero in the common mode gain to be canceled out. A series of simple timing tests suggest the relative performance figures for the instrumentation amplifier circuit are Qucs Verilog-A = 1, Qucs-S/Ngspice = 3 and Qucs qucsator = 8, which suggest that a significant improvement of around eight times, in simulation time, can be gained by synthesizing level five Verilog-A macromodels from level four, or simpler, macromodels.

VI. Conclusions

By combining conventional component simulation models with Qucs Equation-Defined Devices and SPICE B type current sources to form a macromodel, at a stage prior to

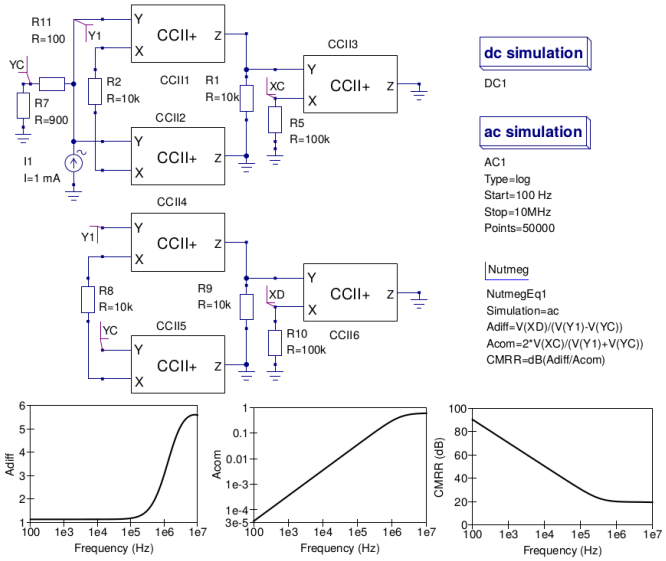

Fig. 9. High bandwidth instrumentation amplifier.

conversion to a Verilog-A module, it is possible to define a series of five distinct macromodelling levels, increasing modelling flexibility and opening new possibilities in integrated circuit macromodelling. In this paper the concept of model level has been employed to demonstrate integrated circuit macromodel development from simple linear models to complex non-linear models. The macromodel level concept has been extended to introduce an additional model level which adds compact Verilog-A modules at the highest level of the modelling hierarchy. This fifth model level is intended for use with circuit simulators that have Verilog-A compiler capabilities for generating C++ model code from Verilog-A modules generated, by hand or by automatic synthesis, from model schematics. To demonstrate the use of macromodels the paper introduces, and discusses, the capabilities of a set of five different macromodel cells suitable for simulating RF wideband current conveyor integrated circuits in all simulation domains. A series of CCII macromodel circuit test benches are outlined and their relative performance described. The results from these test cases indicate that the proposed macromodel level five Verilog-A module reduces circuit simulation times by a measurable amount which could be significant in the simulation of large RF current mode integrated circuits.

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