FOSS CAD/EDA Tools Supporting The European Open Access PDK Initiative

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FOSDEM'24

Libre-SOC, FPGA and VLSI Devroom

Brussels 3 February 2024

FOSS CAD/EDA Tools Supporting The European Open Access PDK Initiative

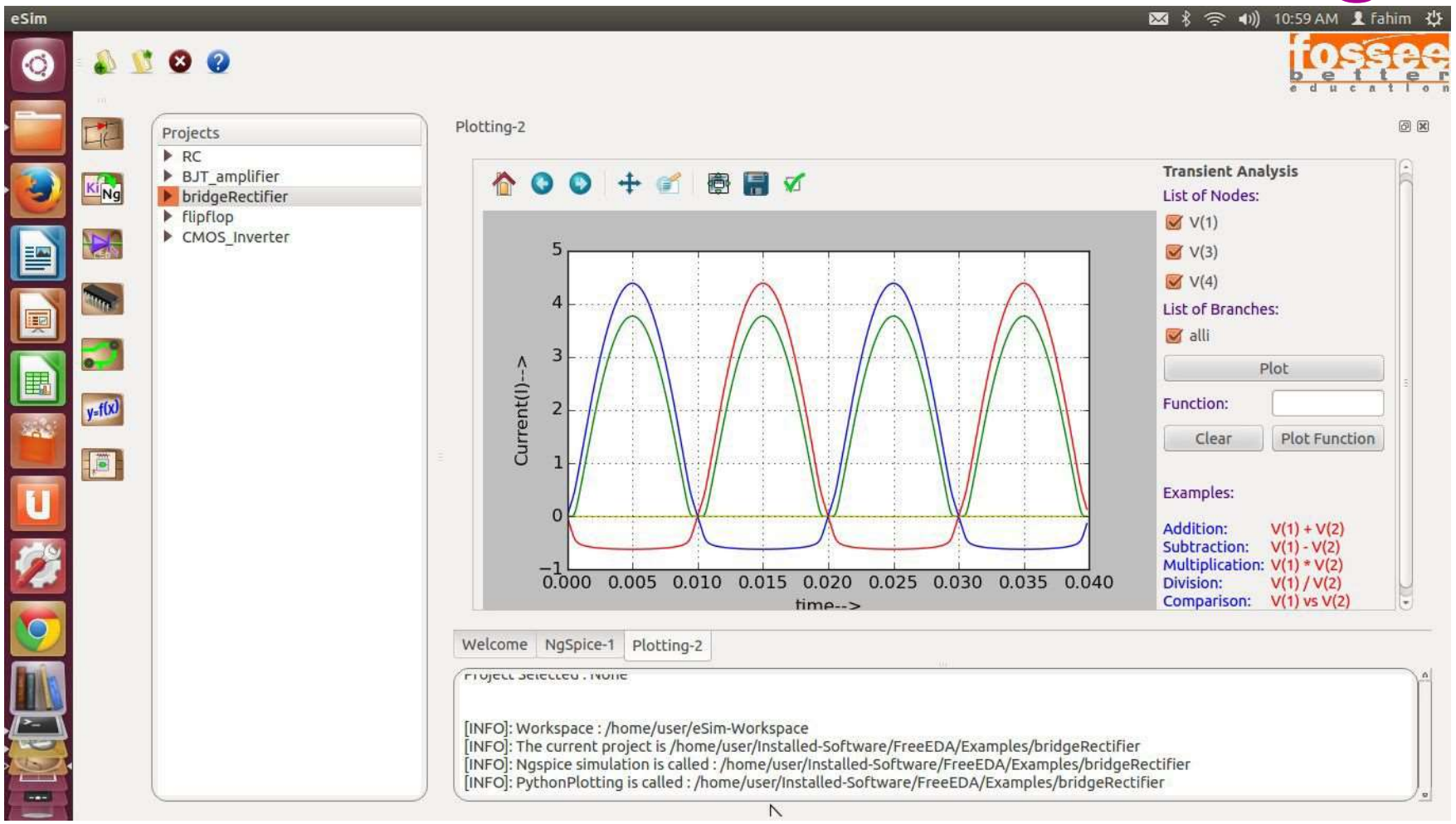
Outline:

- Motivation
- eSim FOSSEE Tool for IC Design
- Open PDK Initiative
  - SkyWater (US), GF (US), AIST ACPS (J), IHP (D)
- IHP Open PDK and FOSS Tools Development
- What's next?
  - Open PDK and FOSS to Empower Researchers and IC Designers
  - IHP Open PDK Roadmap
  - Challenges and Opportunities
- Acknowledgment

Motivation: A call for Building Talent and Skills

[REF] EU Chips Act Drives Pan-European Full-Stack Innovation Partnerships
Plenary Session at ISSCC, FEB.20, 2023
Jo De Boeck, Executive VP and CSO, imec and KU Leuven, Belgium

eSim FOSSEE Tool for IC Design



Features of eSim

- Draw circuits using **KiCad**, create a netlist and simulate using **ngspice**
- Add/Edit SPICE Models and subcircuits using the Model / Subcircuit Builder tools
- Perform Mixed-Signal ngspice Simulation
- Design PCB layouts and generate Gerber files using KiCad
- Support for Ubuntu and Windows

[REF] https://esim.fossee.in/home

Open PDK Initiative

The Open-Source FPGA Foundation offers a set of free and open-source tools enabling fast prototyping for FPGA chips and automated EDA support, through open standard collaboration https://osfpga.org/about-us/

- **Semiconductor R&D**: Tapeout of a design is one of the most important aspects of academic semiconductor research and development.
- **Prohibitive cost**: The prohibitive cost of tapeout and complications therein has prevented the majority of R&D folks and startups from participating.
- **Open-Source**: Open PDK Initiative plans to promote and facilitate the usage of open source FPGA technologies.
- **Free tapeouts**: Open PDK Initiative plans to offer a very simple flow for tapeout, and several of those will be free or at minimal costs.

Available Resources:

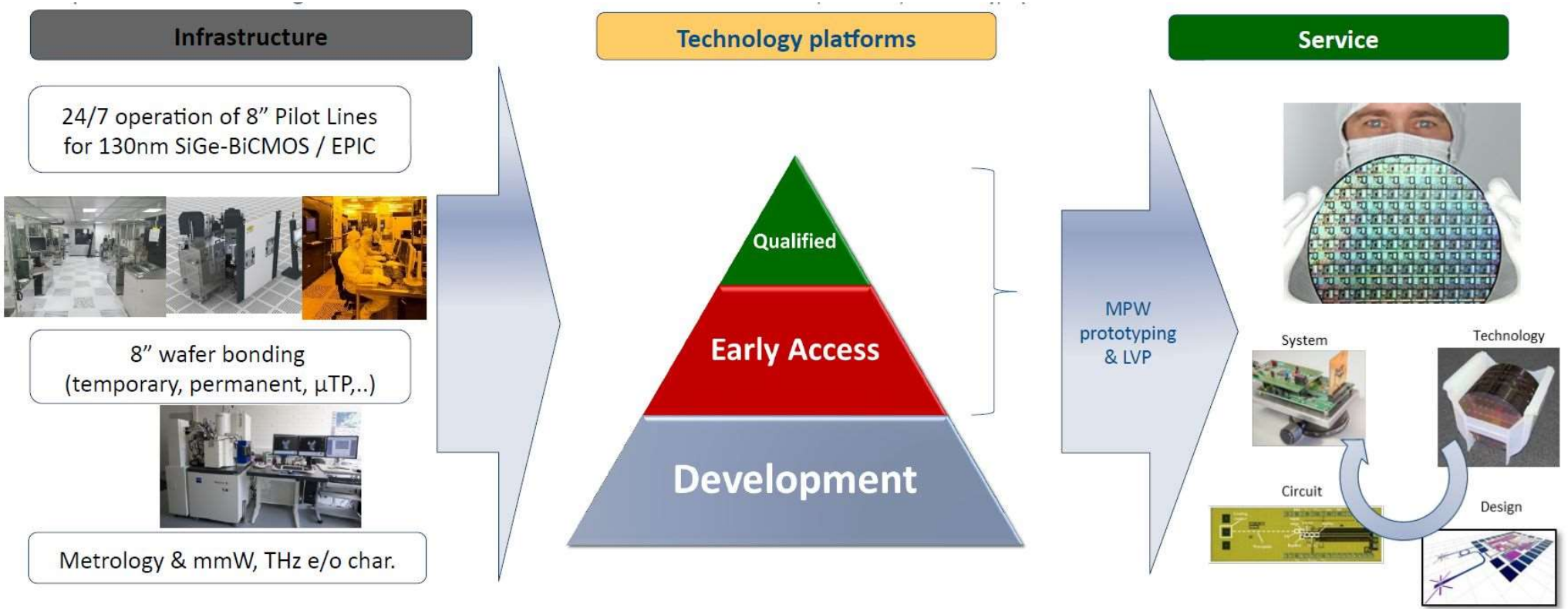
- SkyWater Open 130nm CMOS PDK: https://github.com/google/skywater-pdk
- OpenLane RTL2GDS Compiler: https://github.com/efabless/openlane
- Caravel Harness: https://github.com/efabless/caravel
- Caravel User Project: https://github.com/efabless/caravel_user_project
- Open MPW Precheck: https://github.com/efabless/open_mpw_precheck

FAQ:

- https://efabless.com/open_mpw_faq

IHP Frankfurt (Oder)

Institute for High Performance Microelectronics

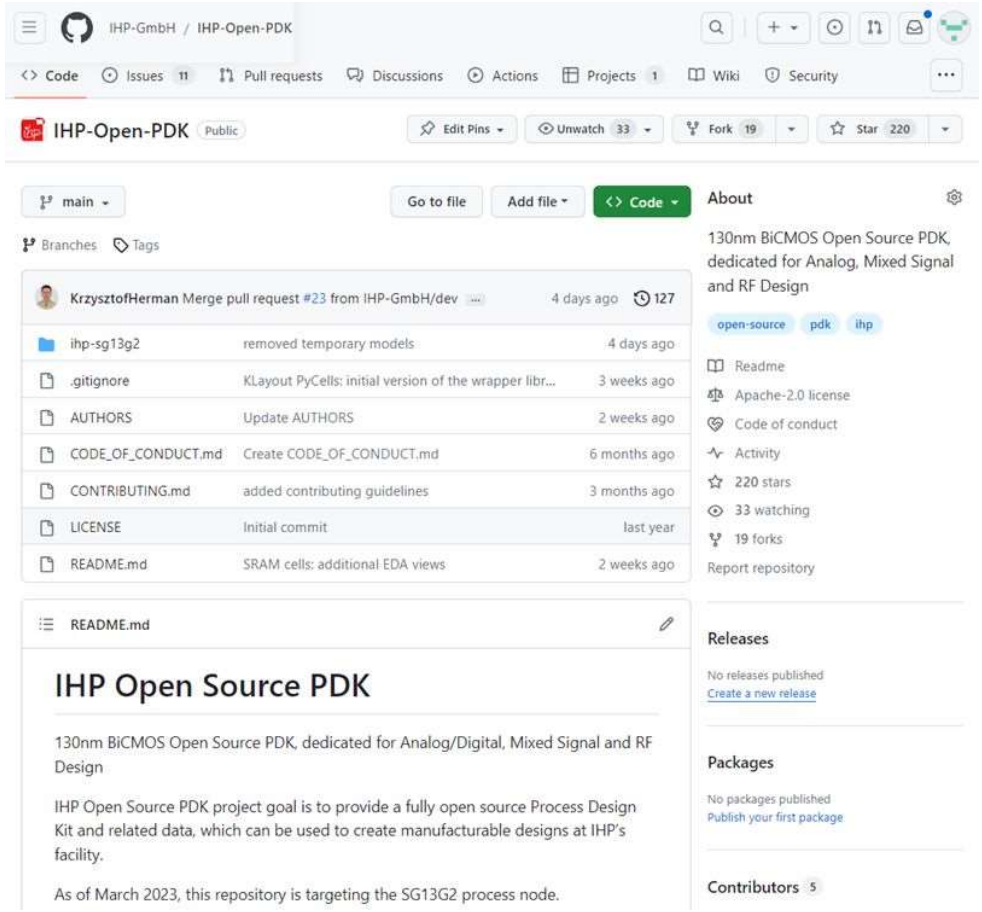


[REF] 130nm BiCMOS Open Source PDK, dedicated for Analog/Digital, Mixed Signal and RF Design
https://github.com/IHP-GmbH/IHP-Open-PDK
Networking Workshop FMD-QNC 27th 28th of June 2023
https://github.com/IHP-GmbH/IHP-Open-PDK/wiki/Networking-Workshop-FMD-QNC

IHP Open PDK and FOSS Tools Development

- IHP started on existing experiences from SkyWater PDK <https://github.com/google/skywater-pdk>
- IHP will offer an analog design flow, later RF design
- Quality should fulfill requirements for academic education
- Open Tools has to be improved, interface development is crucial
- For a sustainable approach, we/IHP have to improve capabilities to a level to support productive projects
- Secure long term funding for MPW and Foundry Service
- Achieve industrial/non-public funding

IHP Open PDK Project on GitHub

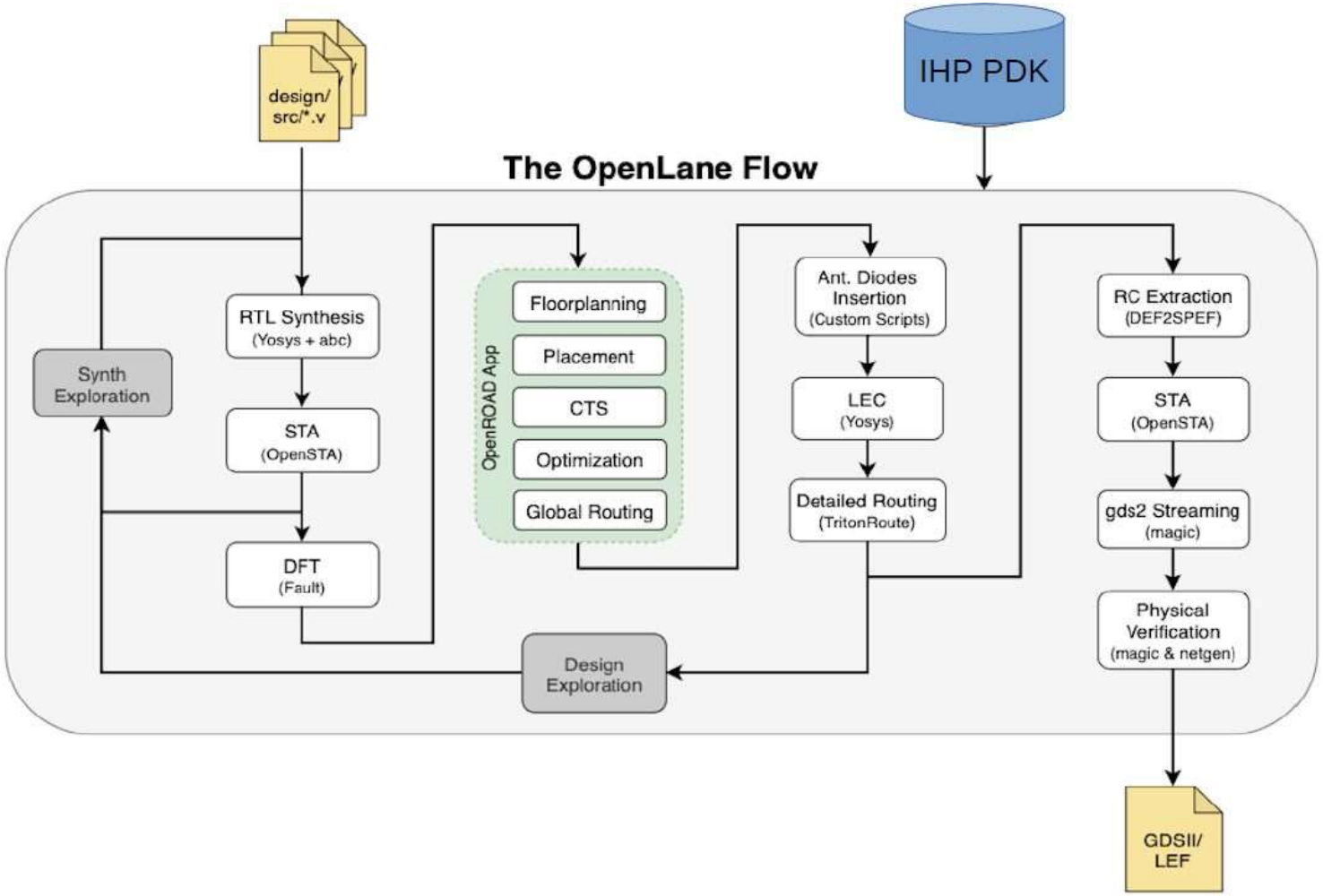


PDK Contents:

- Project Roadmap Gantt chart
- SG13G2 Process Specification & Layout Rules
- Base cell set with limited set of standard logic cells
- SRAM cells
- Primitive devices (GDS)
- GDS Test structures
- MOS/HBT/Passives measurement data
- KLayout layer property and tech files
- KLayout DRC deck (minimal rule set)
- KLayout Parameterizable pycells (limited set)
- MOS/HBT/Passives ngspice/Xyce models
- xschem: device symbols, settings, testbenches
- OpenEMS: tutorials, scripts, documentation

[REF] 130nm BiCMOS Open Source PDK, dedicated for Analog/Digital, Mixed Signal and RF Design
https://github.com/IHP-GmbH/IHP-Open-PDK

Open Source Digital Design Flow



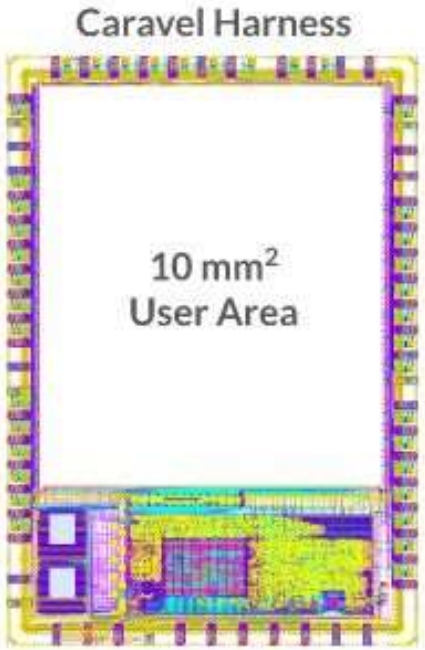
OpenLane is an automated RTL to GDSII flow based on several components including OpenROAD, Yosys, Magic, Netgen, CVC, SPEF-Extractor, KLayout and a number of custom scripts for design exploration and optimization. The flow performs all ASIC implementation steps from RTL all the way down to GDSII.

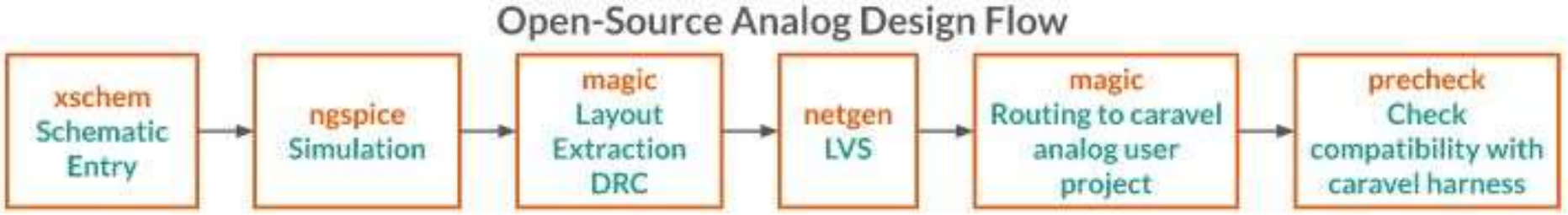
[REF] OpenLane is an automated RTL to GDSII flow
https://github.com/efabless/openlane
Alternative:LiP6 FOSS Logiciels: Alliance, Coriolis, Oceane, Standard Cell Libraries, Tas/Yagle
https://largo.lip6.fr/equipe-cian/logiciels/

FOSS Analog IC Design Flow

FOSS open-source analog design flow with the following tools:

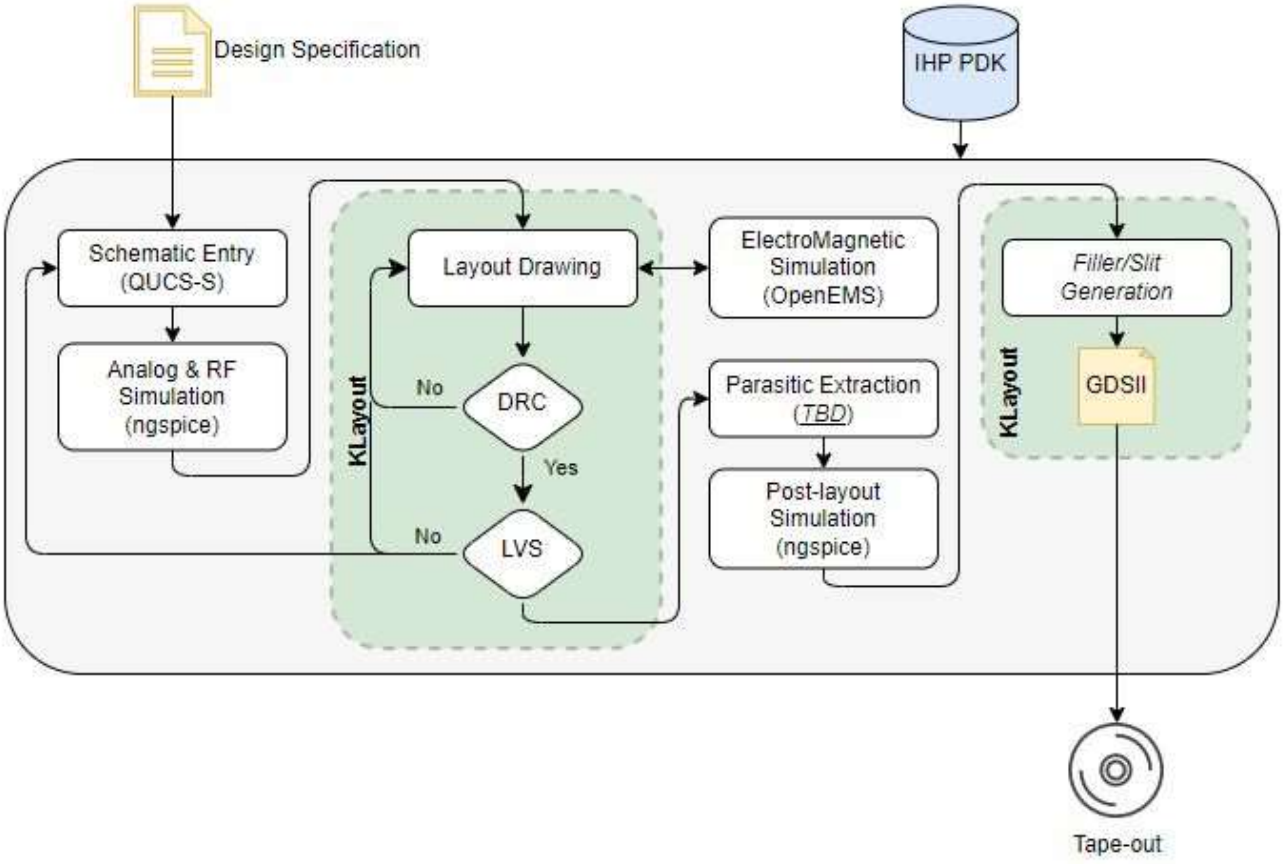
- **PDK** files from skywater-pdk and xschem_sky130.
- Schematic entry with **xschem**.
- Simulation with **ngspice**.
- Layout, extraction and DRC with **magic**
- LVS with **netgen**.
- Manual routing of design using magic into the caravel analog user project. This user project is verified with precheck tool and submitted to the shuttle.





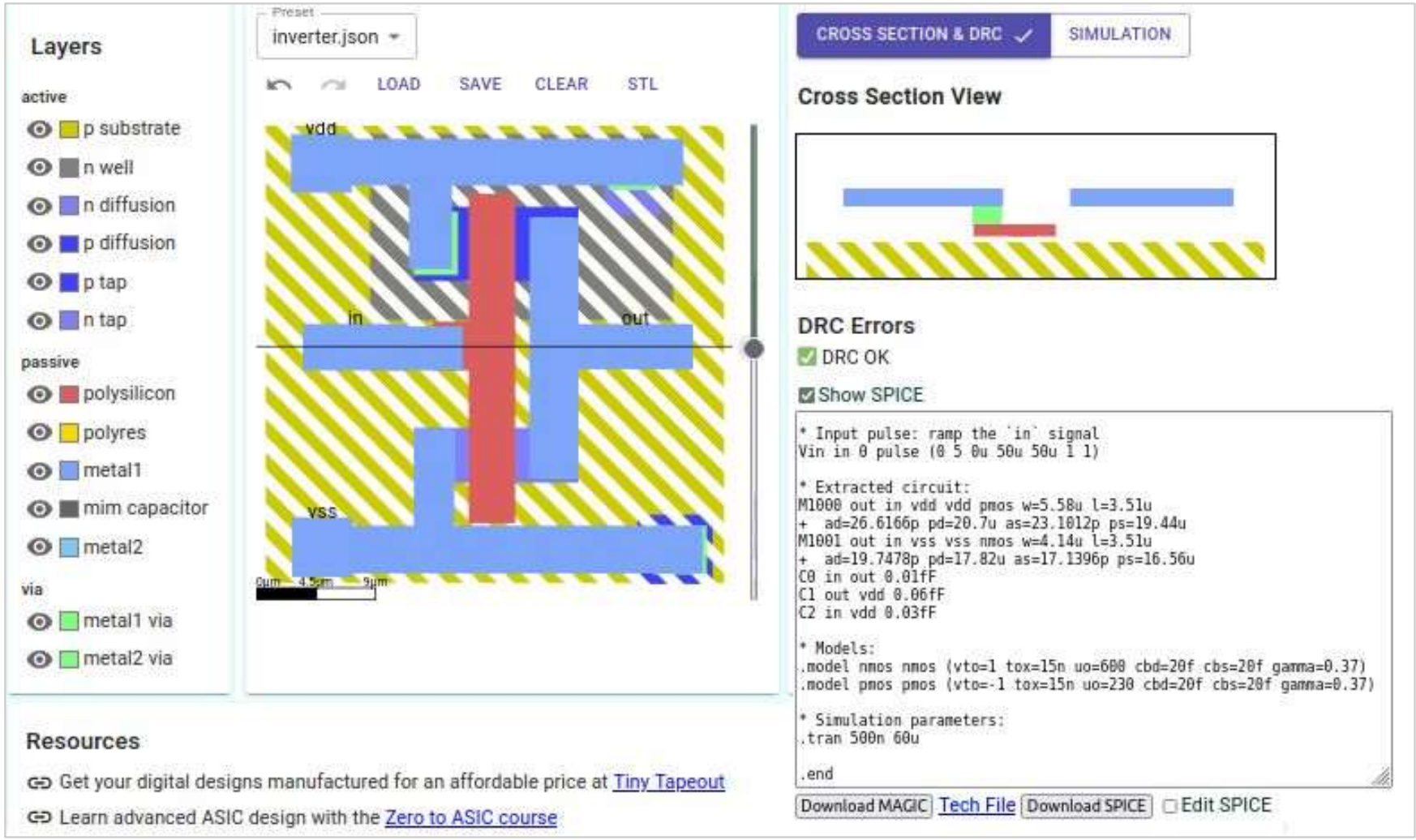
[REF] Prof. Priyanka Raina, Stanford, EE372 https://priyanka-raina.github.io/ee372-spring2022/
FOSS EDA Tools Wiki <https://semiwiki.com/wikis/industry-wikis/eda-open-source-tools-wiki/>
IIC-OSIC-TOOLS is an all-in-one Dockers for analog and digital chip design
<https://github.com/iic-jku/iic-osic-tools>

Analog/RF Open Source Design Flow



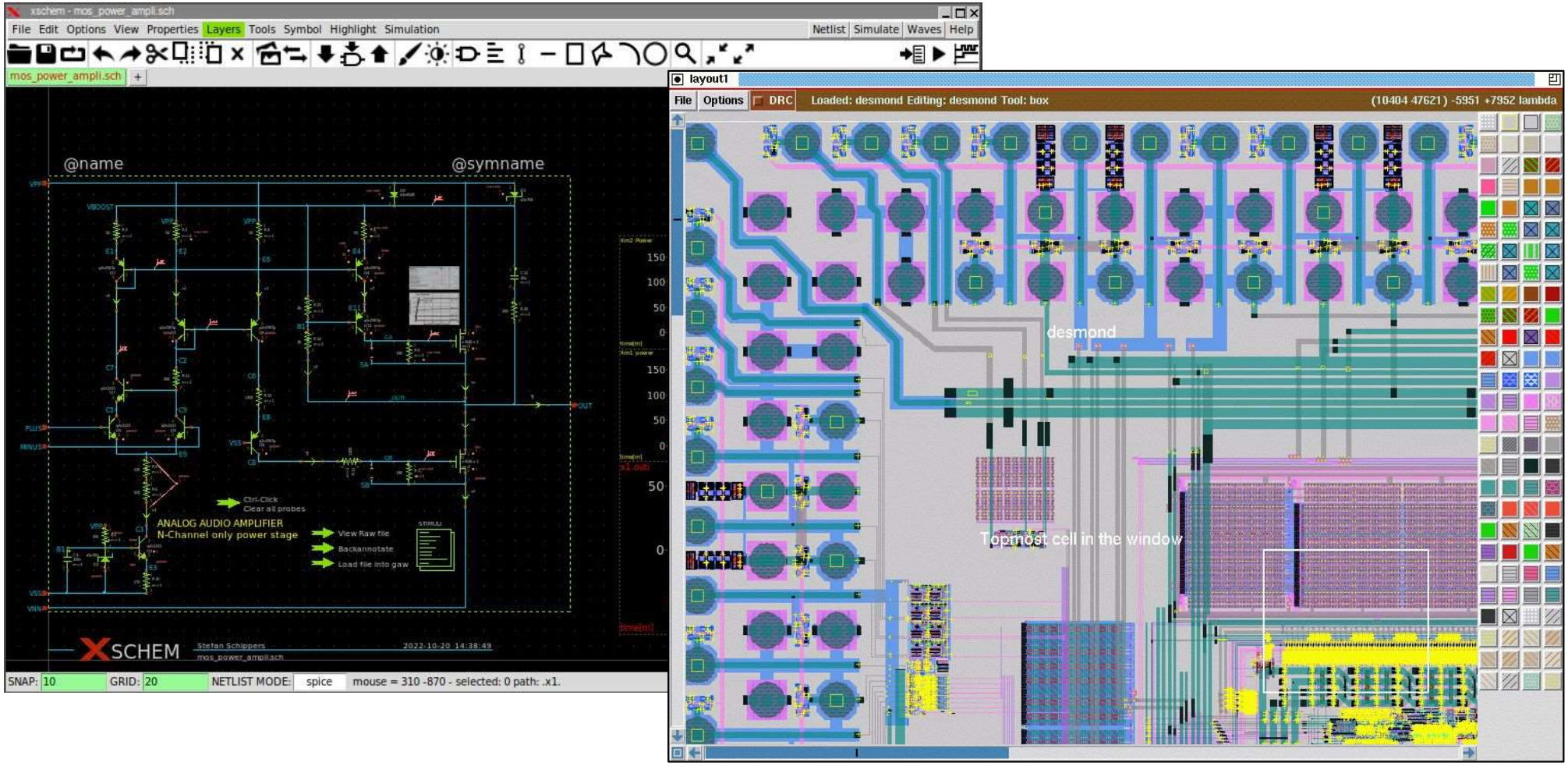
- KLayout-oriented flow
  - Layout design
  - Parametric cells
  - Physical Verification
- QUCS-S, xschem
- ngspice, xyce
- OpenEMS
- other (?)

SiliWiz



SiliWiz https://app.siliwiz.com/
Tiny Typeout https://tinytapeout.com/
Zero to ASIC course https://zerotoasiccourse.com/

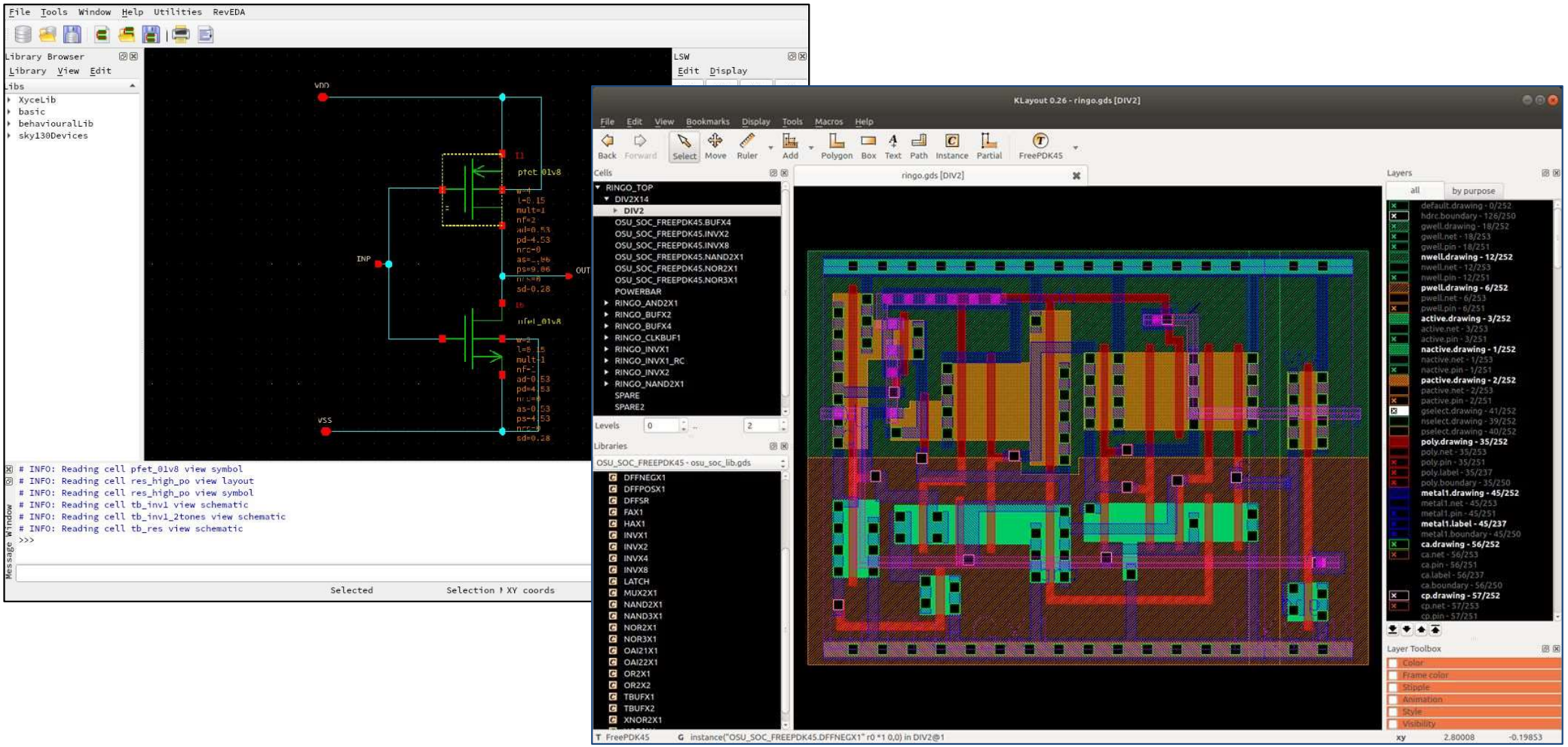
FOSS Schematic and Layout Editors



Xschem is a schematic capture program, it allows creation of hierarchical representation of circuits with a top down approach. By focusing on interfaces, hierarchy and instance properties, a complex system can be described in terms of simpler building blocks. A VHDL or Verilog or Spice netlist can be generated from the drawn schematic <https://xschem.sourceforge.io/stefan/index.html>

Magic version 8.3 is the official current released version of the program, a combined effort of the "Magic Development Team". The open-source license has allowed VLSI engineers with a bent toward programming to implement clever ideas and help magic stay abreast of fabrication technology. <http://opencircuitdesign.com/magic/>

FOSS Schematic and Layout Editors

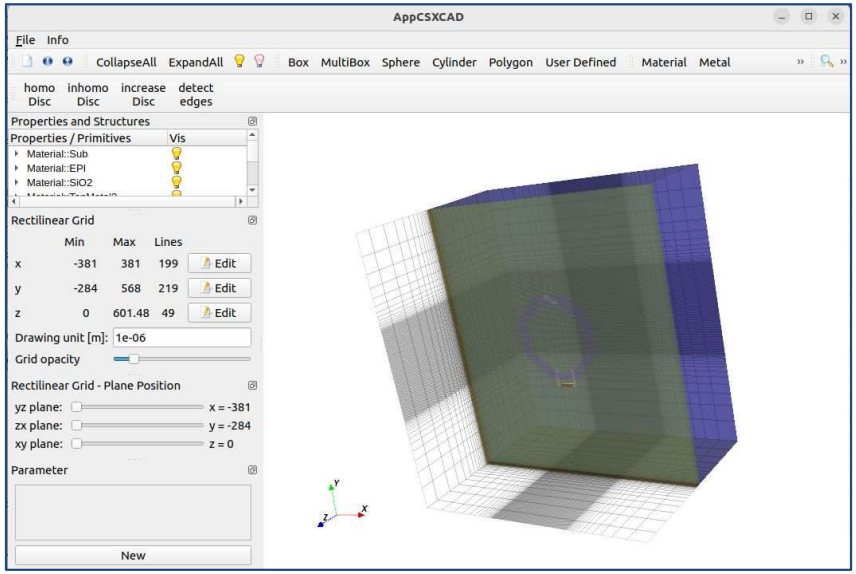


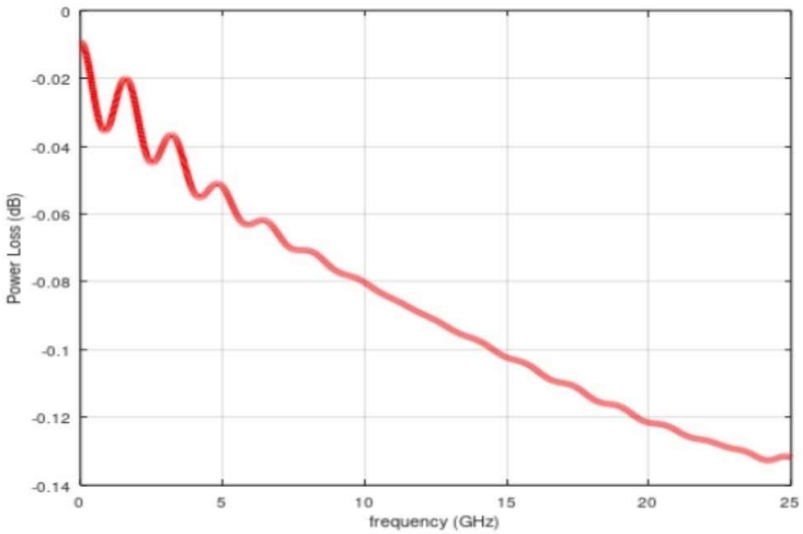
Revolution EDA offers a complete setup starting from schematic or Verilog-A entry, to simulation, layout, DRC and LVS. Symbols have integrated callback functions allowing accurate simulations.
[REF] <https://reveda.eu/>

KLayout has fast loading and accurate drawing, supports GDS and OASIS file formats with automatic uncompression of zlib compatible formats and is extensible and configurable to a large degree by custom Ruby or Python scripts
[REF] https://klayout.de/
https://peertube.f-si.org/video-channels/fsic2022/videos?sort=-publishedAtand page=2

OpenEMS ElectroMagnetic Solver

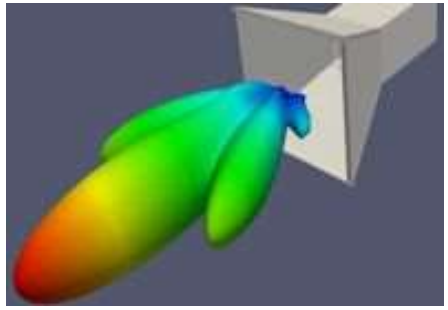
- 3D FDTD solution targeting RF EM simulations
- Model built by Python or Octave scripting
- Graphical viewer for model + mesh (CSXCAD)
- Visualisation: paraview or pyvista-module
- Some interfaces to EDA packages
  but no KLayout support yet
- No internal support for GDSII import, interface was created using Python library gdspy
- S-Parameter output
- Useful tutorials for RF examples
- Possible issue:
  - small residual energy at low frequency or DC might create DC leakage in simulation results
  - Mostly manual mesh definition
  - No user-friendly GUI for IC designer



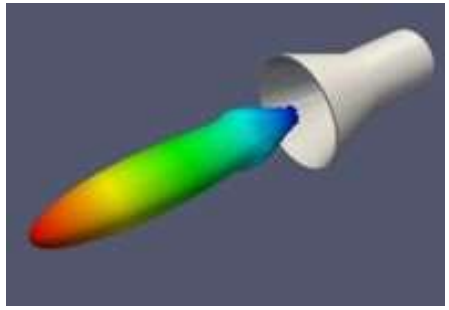


[REF] openEMS - free and open electromagnetic field solver using the FDTD method
https://www.openems.de/

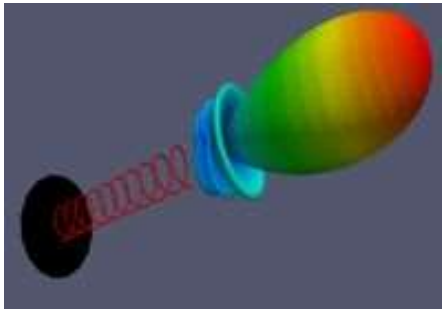
openEMS: FOSS Electromagnetic Field Solver



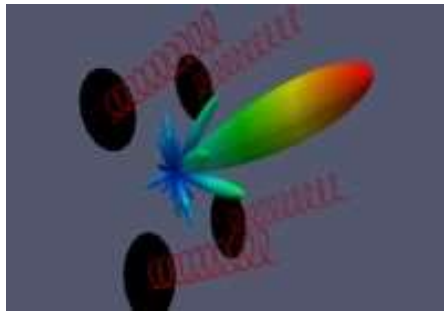
Horn antenna



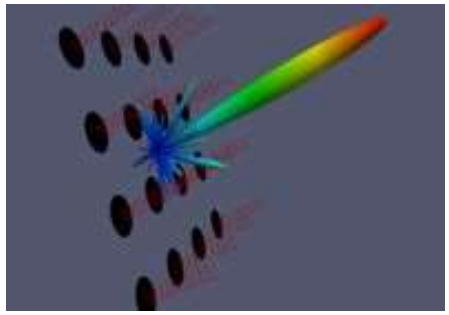
Conical horn antenna



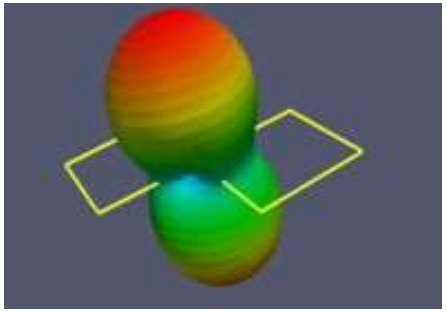
Helix antenna



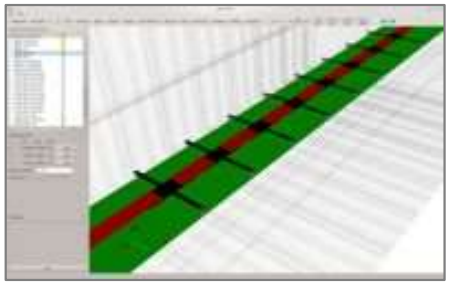
Helix antenna array



Large helix antenna array

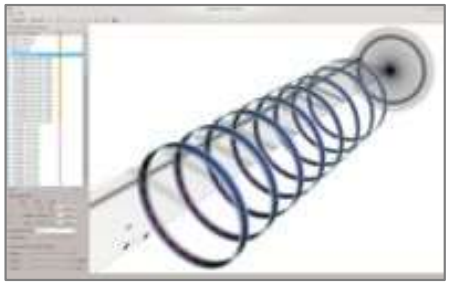


Biquad antenna



CRLH antenna

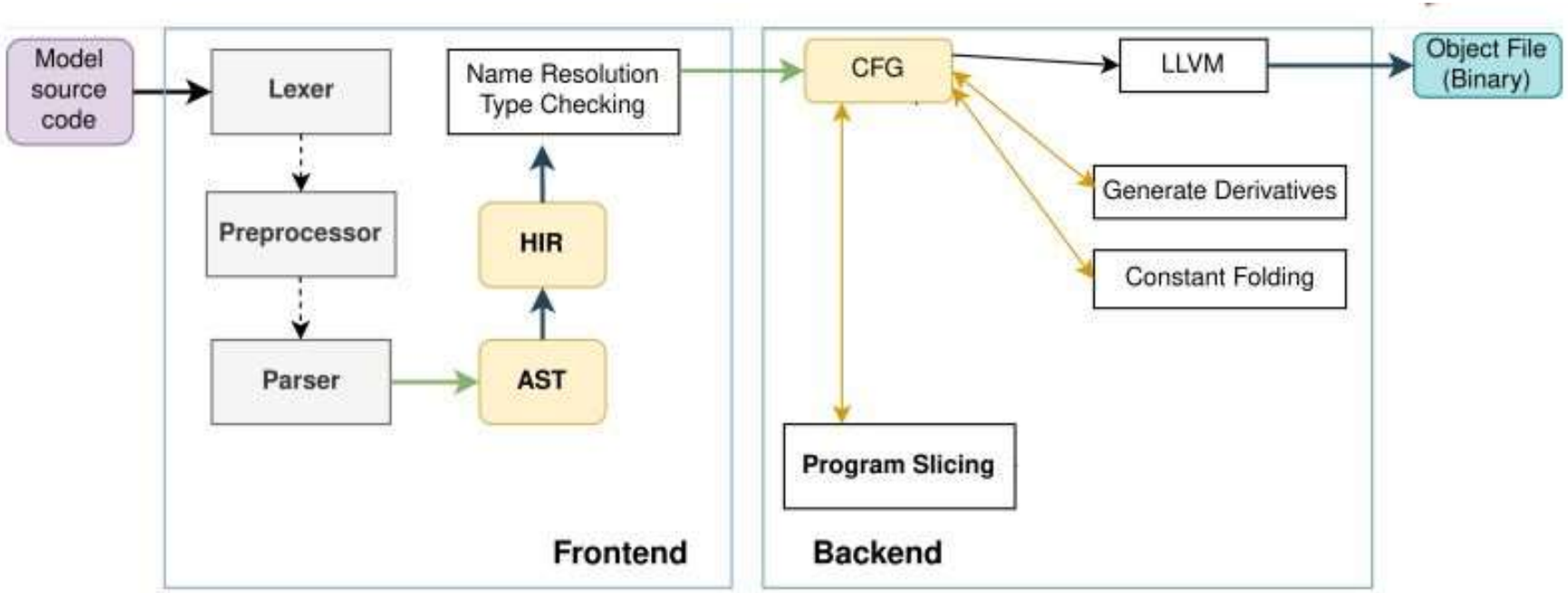
MRI birdcage model



MRI ring antennas

[REF] http://openems.de

OpenVAF: Next-Generation Verilog-A compiler



OpenVAF Roadmap

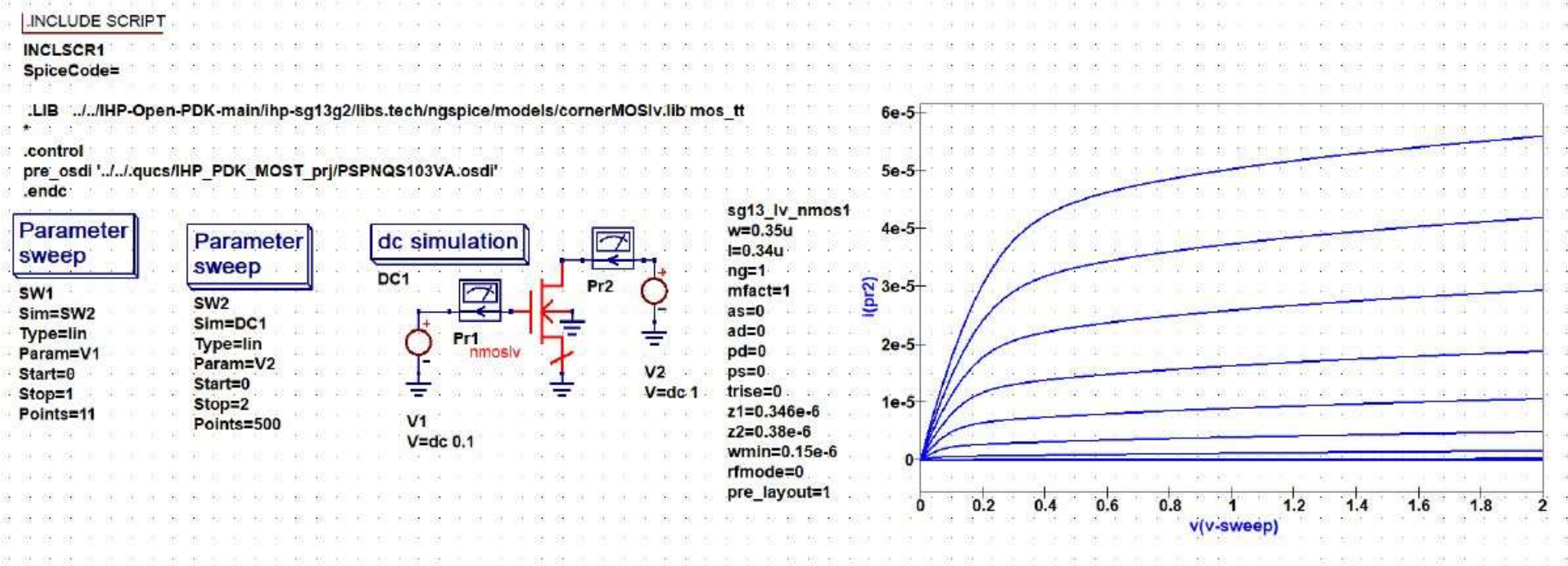
- Reaching full compliance with the Verilog-A standard
  - Behavioral modelling features
  - Support for features that allow defining full circuits/full PDKs in Verilog-A
- OSDI integration in Xyce
- Noise analysis (released with ngspice-42*)
- Improved documentation

[REF] P. Kuthe, M. Muller and M. Schroter, “VerilogAE: An open source Verilog-A compiler for compact model parameter extraction”, J-EDS, vol. 8, pp. 1416–1423, 2020 https://openvaf.semimod.de/

* https://ngspice.sourceforge.io/docs/ngspice-42-manual.pdf

Alternative: Felix Al Davis; Verilog-AMS in Gnucap; https://fosdem.org/2024/schedule/event/fosdem-2024-3560-verilog-ams-in-gnucap/

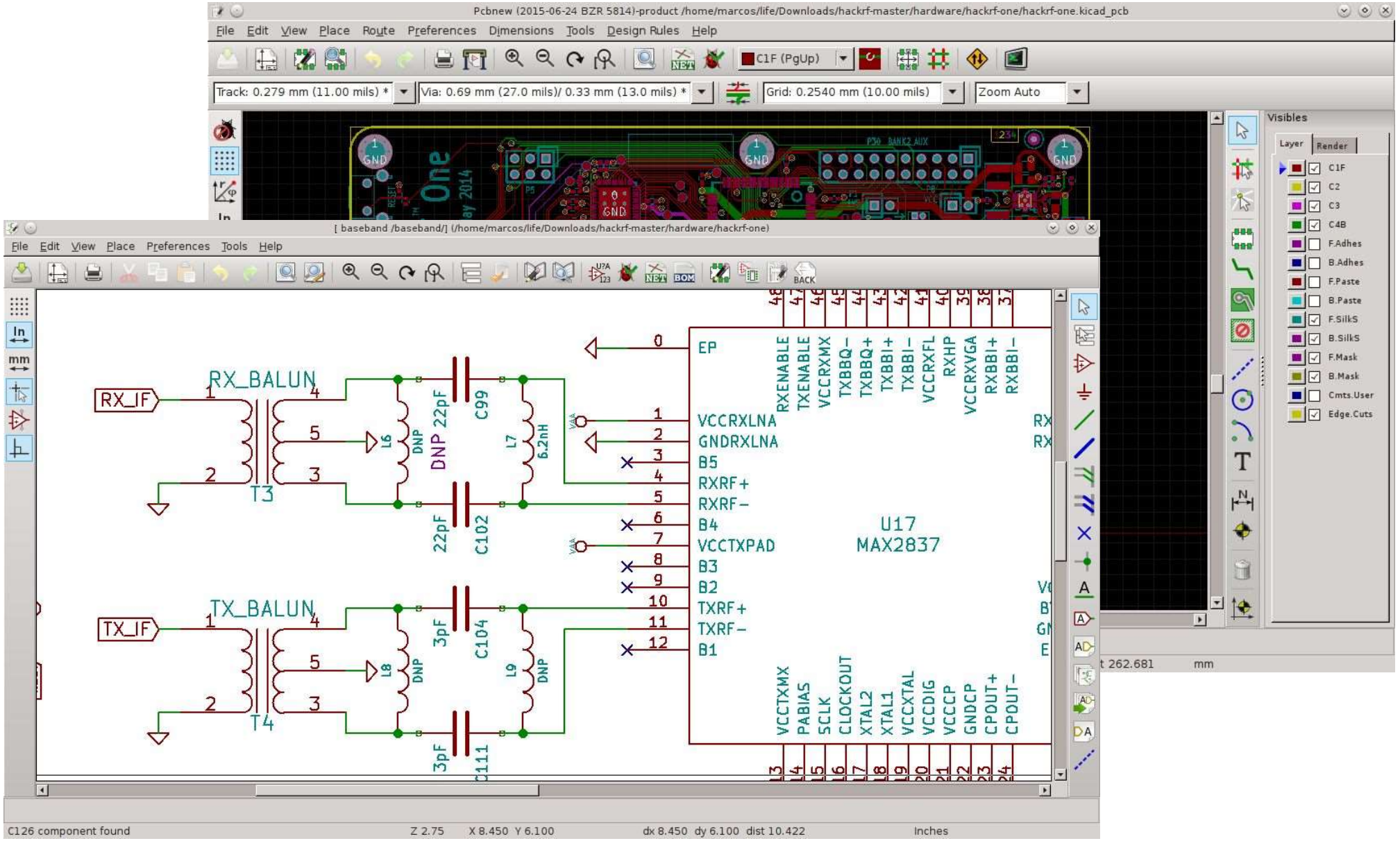
ngspice and QUCS-S Custom Library for IHP Open PDK



sg13g2 nMOS output characteristic test circuit

[REF] Qucs-S - circuit simulation program with Qt-based GUI
https://ra3xdh.github.io/

ngspice and KiCAD



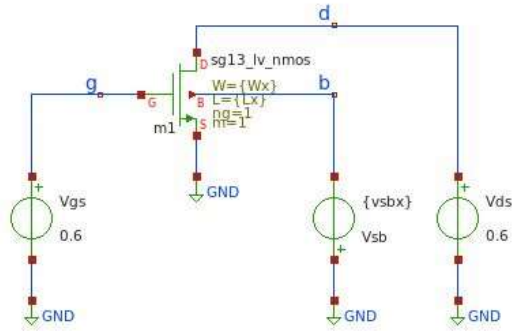
[REF] https://www.kicad.org/download/

Holger Vogt; ngspice circuit simulator - stand-alone and embedded into KiCad
https://fosdem.org/2024/schedule/event/fosdem-2024-2834-ngspice-circuit-simulator-stand-alone-and-embedded-into-kicad/

Analysis and Design of Integrated Circuits
EE 628 (University of Hawai‘i at Mānoa)

MODEL

```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
```



COMMANDS

```
.param temp=27
.param Wx=5u
.param Lx=0.13u
.param Vsbx=0
.dc Vgs 0 1.2 25m Vds 0 1.2 25m
.include tb_sg13_lv_nmos_save.spice

.control
*pre_osdi ./psp103_nqs.osdi
set wr_singlescale
*set wr_vecnames
option numdgt = 3

foreach L_val 0.13u 0.14u 0.15u 0.16u 0.17u 0.18u 0.19u
+ 0.2u 0.3u 0.4u 0.5u 1u 2u 3u
  alterparam Lx = $L_val
  foreach Vsb_val 0 0.2 0.4 0.6
    alterparam Vsbx = $Vsb_val
    reset
    run
    wrdata sg13_lv_nmos.txt all
    destroy $curplot
    set appendwrite
  end
end
op
show
.endc
```

EE 628 (University of Hawai‘i at Mānoa)

Analysis and Design of Integrated Circuits

Learn mixed-signal circuit design using open-source tools and create your own voltmeter chip!

This course is being developed in collaboration with the Microelectronics Commons California-Pacific-Northwest AI Hub.

[REF] Example of a university course targeting the IHP Open PDK https://github.com/bmurmann/EE628 to teach mixed-signal circuit design using open-source tools and create your own voltmeter chip! This course is being developed in collaboration with the Microelectronics Commons California-Pacific-Northwest AI Hub.

Iguana/PULP at IIS ETH Zürich (CH)

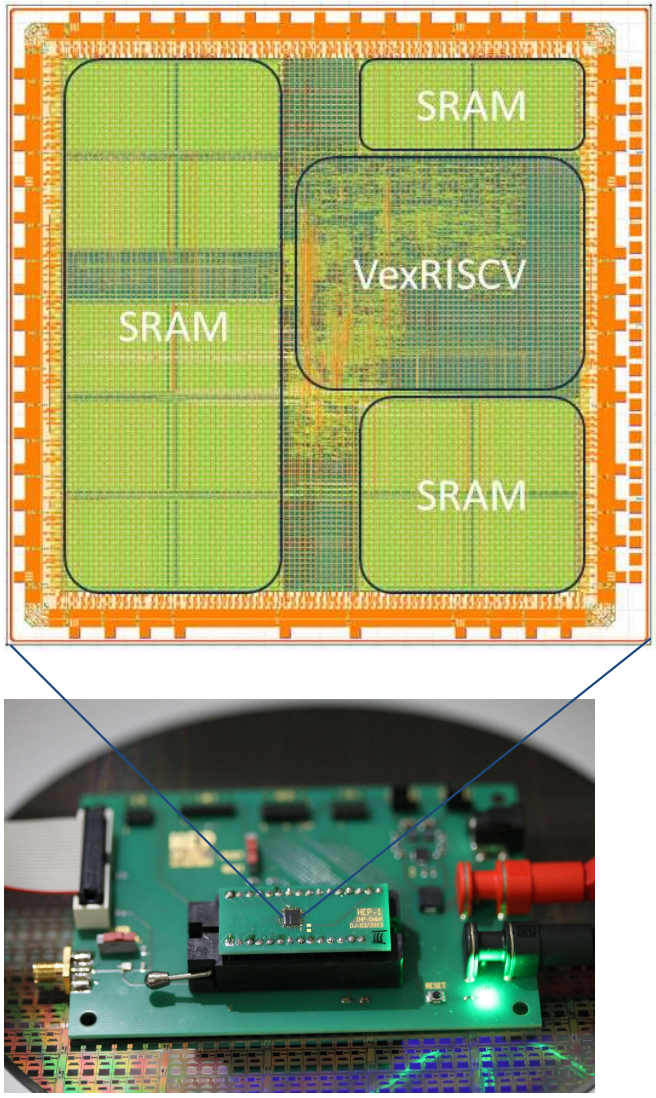
Main Details

Application	Pulp
Technology	130nm
Fab	IHP
Type	Research
Package	QFN88
Dimensions	6264µm x 6264µm
Gates	3 MGE
Voltage	1.2 V
Clock	60 MHz

Iguana is the first IIS ETHZ attempt at using the IHP 130nm Open PDK. The design is essentially the same as Cheshire platform using the CVA6 64-bit RISC-V processor originally developed as part of the PULP team. The design was completed using only open source standard cell libraries, and although an almost complete backend run was made with the OpenROAD tools, a last minute issue very close to the tape-out date resulted in a backup design using commercial EDA tools to be taped-out. Read about the design experience in presentation at the FSiC2023(slides). This design has received generous support from IHP Leibniz Institute for High Performance Microelectronics.

[REF] https://wiki.f-si.org/index.php?title=Industry-Grade_SystemVerilog_IPs_And_The_Open_Flow:_How_We_Synthesized_Iguana

Early adopter for OSH: Project HEP



Open Hardware Security Module

- Open Processor
- Open EDA
- Open PDK

Main Details

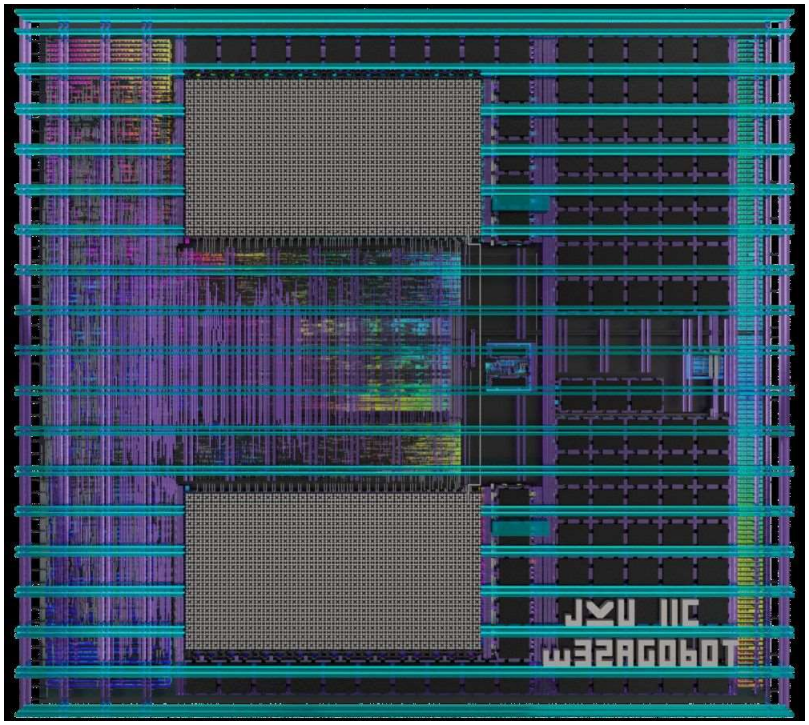
Application Hardware Security Module
Technology 130nm
Fab IHP
Type Prototype
Package Flip Chip
Dimensions 4610µm x 4580µm
(Vex: 1.3mm²; SRAM: 10.2mm²)
Peripherals UART, SPI, JTAG, GPIO
AES accelerator on the ABP3 bus (masked AES)

German early adopter OSH project

- Start 03/2021
- Initiator for IHP-Open130-G2
- First fully open ASIC TapeOut with IHP-Open130-G2
- Root of Trust extensions for IHP-Open130-G2 planned

Project GIT; riscv.org refering the project; Project website

SAR – ADC Project at JKU Linz (A)



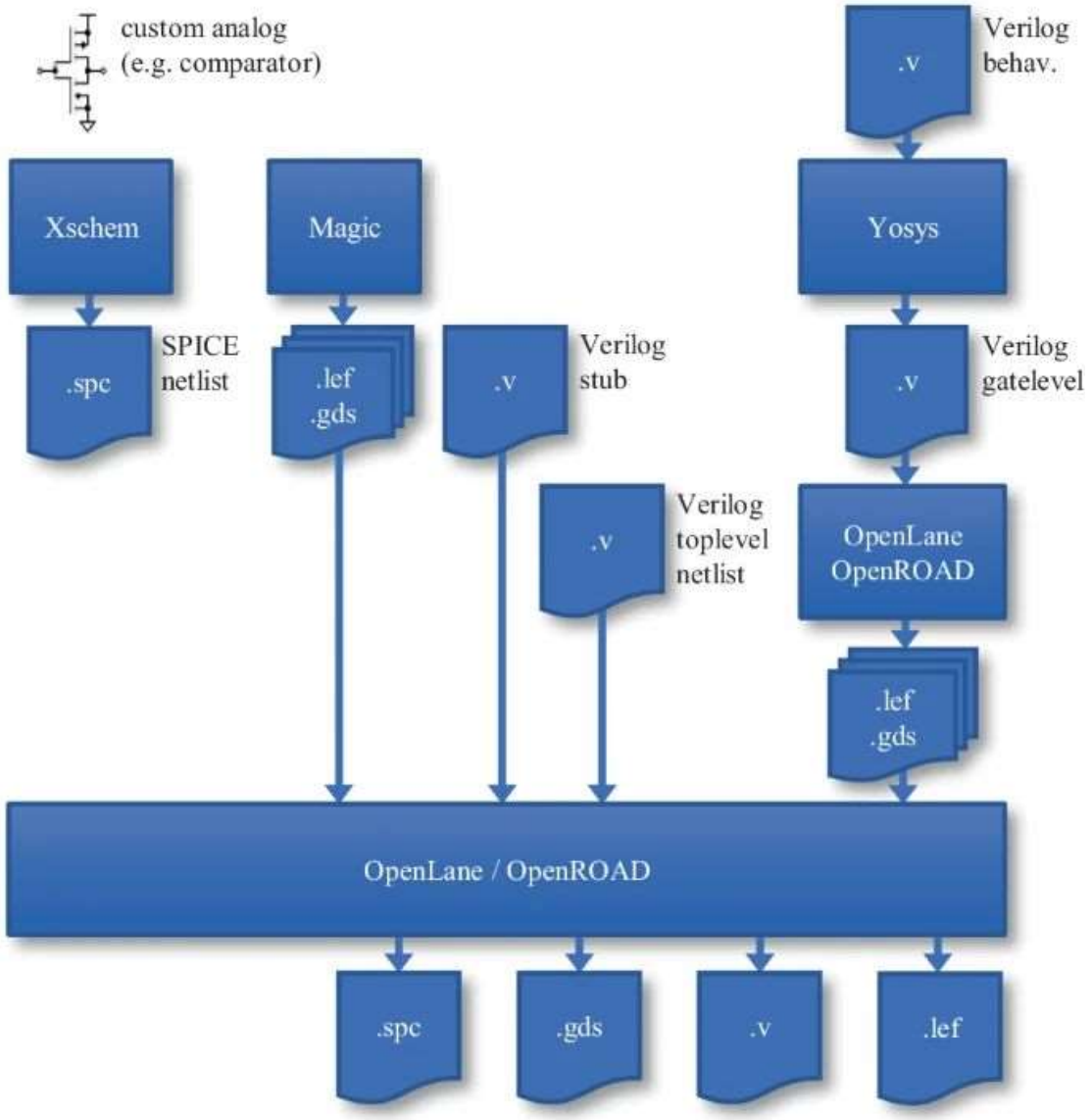
Design of a 1.2MS/s Charge-Redistribution Non-Binary SAR-ADC utilizing the Open-Source SKY130 PDK

https://github.com/iic-jku/SKY130_SAR-ADC1

- Transfer to open SG13G2 PDK in progress
- Mixed Signal capabilities of open PDK needed
- Both Design Projects can be used to benchmark and optimize open PDK and open Tools

[Note] IIC-OSIC-TOOLS is an all-in-one Docker image for SKY130/GF180/IHP130-based analog and digital chip <https://github.com/iic-jku/iic-osic-tools>

An open-sourced 1.44-MS/s 703-µW 12-bit non-binary SAR-ADC 130-nm CMOS at JKU Linz (A)



[REF] Fath, P., Moser, M., Zachl, G. *et al.* Open-source design of integrated circuits. *Elektrotech. Inftech.* (2024) https://doi.org/10.1007/s00502-023-01195-5

What's next?
FOSS to empower researchers and designers

FOSS eSim offers similar capabilities and ease of use as any equivalent proprietary software for schematic creation, simulation and PCB design, without having to pay a huge amount of money to procure licenses.
[REF] https://esim.fossee.in/

The **SSCS PICO Program**: Democratizing IC Design; first open-source IC design contest. Silicon fabrication using **free open** SKY130 PDK on eFabless' chipIgnite shuttle runs in 2021 and 2022, GF180MCU in 2023
[REF]https://sscs.ieee.org/about/solid-state-circuits-directions/sscs-pico-program

RISC-V is a **free and open** ISA enabling for a new era of processor innovation through open collaboration. Offers a new level of free, extensible software and hardware freedom on architecture, paving the way for the years ahead of computing design and innovation.
[REF https://riscv.org/about/

What's next?
IHP Open PDK Roadmap

It is important to leverage community efforts, public funding, corporate contributions and channel effort to foster common goals for an FOSS IC design flow based on open PDK

- Initiate cooperation and joint projects with open source community
  - no closed PDKs, no NDAs, no restrictive EDA licenses
- Demonstration of design training courses in academic institutions
  - Successful open source designs
- Support chip design possibilities for small commercial (SMEs) teams
  - Achieve commercial successful projects

What's next?
Challenges and Opportunities

Things We Need to Work On

- Limited functionality of open-source EDA tools
- Maintenance of tools and repos
- Best practices for team collaboration
- Standards for documentation and validation of "IP"
- Leveraging open-source for analog design automation
  "Grand challenge"
  - Full analog design automation (for arbitrary circuits) from requirements to layout is presently not feasible
  - We should focus on useful baby steps
    - Build large open-source libraries of proven circuit templates
    - Build a framework that can capture the intent and design steps of an experienced designer
    - re-use, reproducibility, partial automation BAG, ANAGEN, MOSAIC, …
    - Create fast quality assessment tools for circuits and layouts
  - Enable "big-data" approaches, away from "correct by construction"

[REF] Boris Murmann, University of Hawaii; Re-Energizing Analog Design using the Open-Source Ecosystem; MOS-AK Silicon Valley 2023; DOI: 10.5281/zenodo.10423729

Acknowledgment

- The IHP PDK Team with Rene Scholz, Open PDK Project Lead
- ETH Zurich + JKU Linz + all the open source community
- German public funded projects:
  - VE-HEP (16KIS1339K) https://elektronikforschung.de/projekte/ve-hep-1
  - IHP Open130-G2 (16ME0852) https://www.elektronikforschung.de/projekte/ihp-open130-g2
  - FMD-QNC (16ME0831) https://www.elektronikforschung.de/projekte/fmd-qnc
  - FMD-QNC with VDI/VDE (IHP PDK Workshop funding)

Arbeitskreis Modellierung von Systemen und Parameterextraktion
Modeling of Systems and Parameter Extraction Working Group

MOS-AK: 2024 Events

- 16th MOS-AK (CMC/IEDM timeframe)
  Silicon Valley, Dec.13, 2023
- FOSDEM
  Bruxelles (BE) Feb. 3-4, 2024
- MOS-AK/EDTM
  Bengaluru, March 3-6, 2024
- 8th Sino MOS-AK
  China, Aug. 2024
- 6th MOS-AK/LADEC
  Guatemala City (GT) May 8-10, 2024
- FSiC 2024
  Paris (Sorbonne) June 19-21, 2024
- Special CM Session, MIXDES
  Gdansk (PL) June 27-29, 2024
- 21st MOS-AK at ESSERC
  Bruges (BE) Sept. 9-12, 2024
- 17th MOS-AK (CMC/IEDM timeframe)
  Silicon Valley, Dec. 2024

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