

# High-Performance 50 $\mu\text{m}$ Silicon-Based On-Chip Antenna with High Port-To-Port Isolation Implemented by Metamaterial and SIW Concepts for THz Integrated Systems

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**Abstract** – A novel 50 $\mu\text{m}$  Silicon-based on-chip antenna is presented that combines metamaterial (MTM) and substrate integrated waveguide (SIW) technologies for integration in THz circuits operating from 0.28 to 0.30 THz. The antenna structure comprises a square patch antenna implemented on a Silicon substrate with a ground-plane. Embedded diagonally in the patch are two T-shaped slots and the edges of the patch is short-circuited to the ground-plane with metal vias, which convert the structure into a substrate integrated waveguide. This structure reduces loss resulting from surface waves and Silicon dielectric substrate. The modes in the structure can be excited through two coaxial ports connected to the patch from the underside of the Silicon substrate. The proposed antenna structure is essentially transformed to exhibit metamaterial properties by realizing two T-shaped slots, which enlarges the effective aperture area of the miniature antenna and significantly enhances its impedance bandwidth and radiation characteristics between 0.28 THz to 0.3 THz. It has an average gain and efficiency of 4.5dBi and 65%, respectively. In addition, it is a self-isolated structure with high isolation of better than 30dB between the two ports. The on-chip antenna has dimensions of 800 $\times$ 800 $\times$ 60  $\mu\text{m}^3$ .

## I. INTRODUCTION

Miniaturization is a key factor in RF System-on-Chip (SoC) design. In order to keep the transceiver size to a minimum, the antenna (which is the largest part of a typical transceiver module) has to be miniaturized. This is because the size of the antenna is a function of its wavelength. Traditionally, antennas are off-chip due to their size and because typical Silicon (Si) substrates are highly conductive. However, if the antenna can be realized on-chip, it can result in a fully integrated, low cost RF SoC with no bond wires and off-chip components. Antenna impedance can be utilized to replace the matching network interface between antenna and the RF circuits, which should reduce the overall size of the antenna. Though the initial on-chip antenna design has been reported almost a decade ago, not until recently, this concept has gained popularity with the advent of new technologies. Former on-chip antennas display high transmission loss and were not characterized for gain and radiation pattern whereas the latter designs often utilize additional processing steps to increase the resistivity of Si substrates in an attempt to enhance the on-chip antenna performance. However, the major challenge is the poor radiation efficiency due to lossy Si-substrate [1]. In this paper we overcome the drawbacks of the on-chip antenna by utilizing together metamaterial (MTM) and substrate integrated waveguide (SIW) technologies [2–4].

In recent years, substrate integrated waveguide cavities have been extensively studied for antenna miniaturization by using fraction modes such as half-mode (HM) [5], quarter-mode (QM) [6], and eighth-mode (EM) [7]. They can maintain a similar field distribution as that of TE<sub>110</sub> mode but their sizes are significantly reduced. For instance, the EM only occupies one-eighth cavity size of the full-mode (FM). However, EM-SIW cavity antenna elements have been rarely reported for the design of antenna systems.

This paper presents a high-performance antenna implemented on Silicon substrate for on-chip terahertz systems. The design of the proposed antenna combines MTM and SIW technologies to realize an antenna that operates from 0.28 to 0.30 THz with high radiation gain and efficiency performances. In addition, the proposed antenna structure provides high-isolation between the two feed ports of the antenna with no use of any additional isolation or decoupling networks.

## II. PROPOSED ON-CHIP ANTENNA FOR HIGH-PERFORMANCE AT THZ BAND

The structure of the proposed antenna is shown in Fig.1. It is constructed on a lossy Silicon (Si) substrate with thickness of  $50\mu\text{m}$ , dielectric constant of 11.9, and loss-tangent of 0.00025. The back-side of the Si-layer is covered in a ground-plane made of Aluminum with length, width, and thickness of  $800\mu\text{m}$ ,  $800\mu\text{m}$ , and  $5\mu\text{m}$ , respectively. On the top-side of the Si-layer a square patch antenna is implemented with length, width, and thickness of  $600\mu\text{m}$ ,  $600\mu\text{m}$ , and  $5\mu\text{m}$ , respectively. The periphery of the antenna is punctuated with metal vias to provide a short-circuiting pathway for surface currents to the ground-plane and to create a quarter-mode (QM) SIW cavity under the patch. Included in the patch are two narrow T-shaped slots located diagonally, as shown in Fig. 1. The T-shaped slots divide the single QM cavity into two equal eighth-mode (EM) sub-cavities. These two sub-cavities are connected with each other so that when excited by electromagnetic energy through a feeding port the energy is radiated at the cavity's edges as well as by the resonant T-shaped slots into free-space. A self-isolation mechanism is achieved by the proposed structure resulting in high-isolation between the two ports with no need for additional isolation or decoupling network. The antenna is excited through two coaxial feed ports. The center pin and outer conductors of coaxial feed ports are connected to the patch plane and ground-plane, respectively.

The T-shaped slots play the role of the series left-handed capacitances ( $C_L$ ) and the metal vias, which short-circuit the patch to the ground-plane under the Si-layer, act as shunt left-handed inductances ( $L_L$ ). This configuration essentially transforms the proposed structure to possess metamaterial properties. In fact, as the results below reveal it enables the proposed antenna for on-chip applications to achieve high performance in a miniaturized foot-print area [4].

The dimensions of the metamaterial slots and their spacing from each other, and dimensions of the metal vias and their spacing from each other have influence the performance of the antenna. The optimized structural parameters are tabulated in Table I. The proposed on-chip antenna has very compact dimensions of  $800 \times 800 \times 60 \mu\text{m}^3$ .

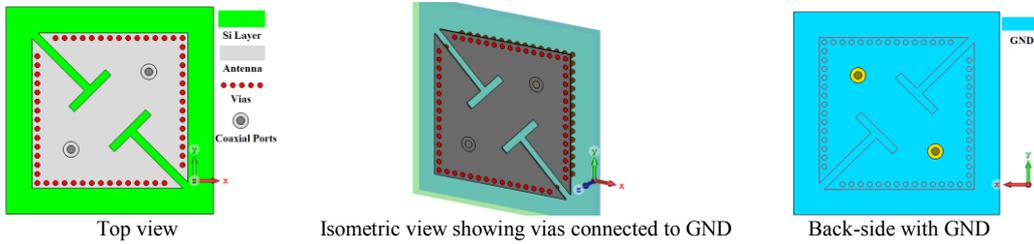


Fig.1. Proposed on-chip antenna layout based on MTM and SIW

TABLE I. STRUCTURAL PARAMETERS

| Patch size                              | Ground-plane size                       | Slot length      | Slot width      | Slot spacing     | Radius of the via | Via spacing     | Radius of the center pins | Radius of the outer conductors of feeding ports | Si-Layer thickness |
|---|---|------------------|-----------------|------------------|-------------------|-----------------|---------------------------|---|--------------------|
| $600 \times 600 \times 5 \mu\text{m}^3$ | $800 \times 800 \times 5 \mu\text{m}^3$ | $330\mu\text{m}$ | $30\mu\text{m}$ | $200\mu\text{m}$ | $10\mu\text{m}$   | $10\mu\text{m}$ | $15\mu\text{m}$           | $30\mu\text{m}$                                 | $50\mu\text{m}$    |

The S-parameter responses of the reflection ( $S_{11}$  &  $S_{22}$ ) and transition ( $S_{12}$  &  $S_{21}$ ) coefficients of the proposed on-chip antenna are shown in Fig. 2. This shows the antenna operates over a wide frequency range from 0.28 to 0.30 THz for  $S_{11} < -15\text{dB}$ , which corresponds to a fractional bandwidth of  $\sim 7\%$ . The average impedance match over its operation frequency range is 22dB and the average isolation level between the two ports is better than 30dB. The high isolation level results from the self-isolated mechanism in the proposed antenna. This is achieved with no additional isolation or decoupling structure.

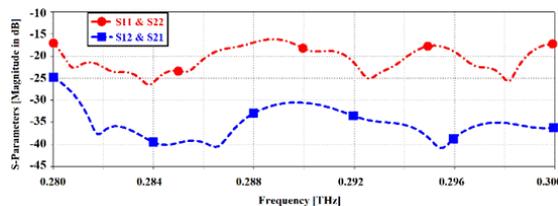


Fig.2. Reflection and transition coefficient responses ( $S_{11}=S_{22}$  &  $S_{12}=S_{21}$ ).

The radiation gain and efficiency of the proposed on-chip antenna versus frequency are shown in Fig. 3. The gain and efficiency peak at around 0.29 THz. Over the antenna's operating frequency range the minimum gain and efficiency are 4dBi and 57%, respectively, and the average gain and efficiency are ~4.5dBi and ~65%, respectively. The radiation E- and H-planes patterns of the proposed on-chip antenna at operating frequency of 0.29 THz are shown in Fig. 4. The antenna radiates bi-directionally in both E- and H-planes however the 3 dB beamwidth is considerably larger in the E-plane.

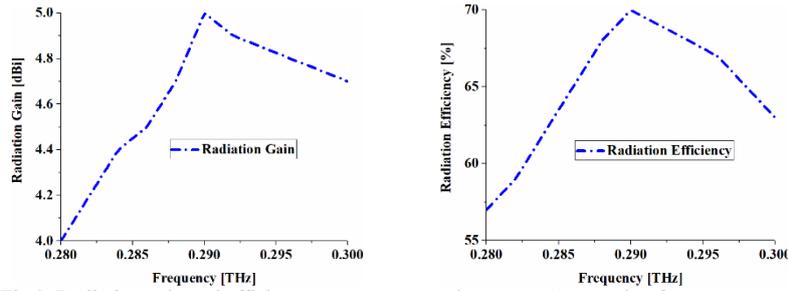


Fig.3. Radiation gain and efficiency responses over the antenna's operating frequency range.

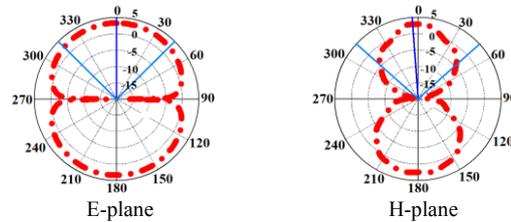


Fig.4. Radiation patterns in the E- and H-planes at 0.29 THz.

### III. CONCLUSION

By combining the metamaterial and SIW concepts in the proposed antenna design the effective aperture area of the on-chip antenna has enlarged and the surface waves and substrate losses have reduced. It is demonstrated that this leads to an improved impedance matching, impedance bandwidth, port-to-port isolation, radiation gain and efficiency, and radiation characteristics. The miniature antenna is intended for on-chip application in terahertz integrated circuits.

### ACKNOWLEDGEMENT

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