Interactive compact device modelling using Qucs equation defined devices

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SUMMARY

Recent trends in compact device modelling and circuit simulation suggest a growing movement towards standardisation of Verilog-A as a vehicle for semiconductor device specification and model interchange among commercial and open source simulators. This paper introduces a nonlinear equation defined device characterised by current, voltage and charge equations with a similar syntax to Verilog-A. The equation defined device has been implemented in Qucs and used extensively as a central feature in an interactive modelling system that allows straightforward prototyping of compact device models prior to translation into Verilog-A. To illustrate the properties and use of the Qucs equation defined device a number of examples centred on well-known SPICE models are described.

KEY WORDS: Qucs; equation defined devices; compact device modelling

1. INTRODUCTION

Qucs ("Quite Universal Circuit Simulator") [1] is an open source circuit simulator developed by a group of international scientists and engineers under the GNU General Public License (GPL). Both binary and source code versions of the package can be downloaded from http://qucs.sourceforge.net. Versions are available for most of the popular computer operating systems. The latest Qucs release marks a turning point in the development of the simulator's device and circuit modelling facilities. Release 0.0.11 introduced component values defined by equations, and for the first time allowed subcircuits with parameters. The current release, version 0.0.12, extends these features to add device model construction using symbolic equations that are similar to model code written in the Verilog-A language [2]. When designing the latest simulation and modelling features the Qucs development team has attempted to address the need to provide the package with an interactive and easy to use modelling system that allows

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straightforward compact device model construction. This paper presents an equation defined device approach to compact device modelling. A number of example semiconductor device and nonlinear component models are described. These are based on well-known SPICE models, and illustrate an interactive technique for compact device model development.

2. THE QUCS EQUATION DEFINED DEVICE (EDD)

Qucs EDD is a nonlinear equation defined device comprising one or more two terminal components whose properties are characterised by branch current, branch voltage and internal stored charge. EDD branch currents can be expressed as symbolic voltage functions, derived from any branch voltage in the same EDD, and stored charge that can be a function of branch voltage and branch current, again derived from any branch voltage and current in the same EDD. EDD is an advanced component, allowing users to construct their own models from a set of equations derived from physical device properties. EDD models can be combined with conventional circuit components and Qucs equation blocks to build compact device subcircuits. An EDD is a nonlinear component with up to eight branches. Each branch is characterised by current I_n, voltage V_n and charge Q_n where $1 \le n \le 8$. The eight branch limit can be increased, if required. Branches with I=0 and Q=0, that are connected to external inputs, act as high impedance voltage probes.

3. EDD MODELS WITH EXPLICIT EQUATIONS

The current Qucs release implements an explicit form of EDD [3], implying that the EDD current and charge equations must be expressed in the form I(V) and Q(V,I), where V and I are EDD branch voltages and currents, respectively. EDD two terminal branch components are characterised by the expressions given in equations (1) and (2)

$$I = I(V) \quad \text{and} \quad g = \frac{dI}{dV} \tag{1}$$

$$Q = Q(V, I) \quad \text{and} \quad c = \frac{dQ}{dV} = \frac{dQ(V)}{dV} + \frac{dQ(I)}{dV} \tag{2}$$

Where, g is the branch conductance and c is the branch capacitance. EDD nonlinear capacitance is extracted from branch charge, allowing implementation of differentiation rather than numeric or symbolic integration that is needed to derive branch charge from nonlinear branch capacitance. Similarly, branch conductance is determined by Qucs from the derivative of branch current. Qucs automatically creates symbolic derivatives during simulation. EDD equations may include constants, branch variables, variables from Qucs equation blocks, subcircuit parameters, the operators and functions defined in Verilog-A, plus additional functions selected from an extended set of mathematical functions held in a Qucs function library. Variables, constants and equations may be entered in any order in Qucs equation blocks. Conditional branch current and charge equations can be selected by if-then-else statements with a C like ternary operator (?:) syntax. Nested if-then-else statements are also allowed. EDD is similar, but more advanced, to the B type nonlinear controlled current/voltage sources implemented in SPICE 3f5 [4]. EDD is capable of

realising the same models as the SPICE 3f5 type B device plus an extensive range of more complex compact device models. Unlike Qucs EDD, SPICE 3f5 B style nonlinear controlled sources do not allow branch current and charge to be specified at the same time. A similar comment can be made regarding the use of if-then-else statements for defining conditional branch current and charge equations. Comparison of Qucs EDD features with those provided by commercial simulators is difficult, mainly due to the fact that lack of standardisation for such features is common amongst the current popular simulators. However, two observations are worth reporting. These involve the Qucs EDD structure which is essentially based on I(V) and Q(I,V) relationships that do not allow EDD branch voltages to be expressed as functions of branch currents. Firstly, both SPICE 3f5 and commercial simulators do not have this limitation, mainly through their use of controlled sources for nonlinear modelling. Qucs overcomes this limitation by allowing the use of a gyrator as a work-around. Gyrators can also be used with Qucs EDD to model nonlinear inductors (see section 8). Secondly, the EDD structure has been devised to allow simple translation of the EDD current and charge equations into Verilog-A.

4. AN EDD SEMICONDUCTOR DIODE MODEL

Figure 1 illustrates an EDD compact device model for a semiconductor diode. The diode I-V characteristic is determined by subcircuit parameters similar to the standard SPICE diode model parameters [5]. These are listed in Figure 1 as diode SUB1 subcircuit parameters. EDD diode current Id is the sum of branch currents I1, I2, I3 and I4, where I1 represents the current in the forward bias region of the diode characteristic, I2 the reverse bias region current and I3 plus I4 the reverse breakdown region current. The I-V relationship for each bias region is given by equations (3) to (6), where the diode voltage Vd equals EDD branch voltage V1.

$$I1 = Is \cdot \left(\mathrm{limexp}\left(\frac{V1}{N \cdot Vt} \right) - 1 \right) + V1 \cdot GMIN, \quad \forall \ (V1 > -5 \cdot N \cdot Vt) \tag{3}$$

$$I2 = -Is + V1 \cdot GMIN, \quad \forall \ (-Bv < V1) \text{ and } (V1 < -5 \cdot N \cdot Vt) \tag{4}$$

$$I3 = -Ibv, \quad \forall \ (V1 == -Bv) \tag{5}$$

$$I4 = -Is \cdot \left(\mathrm{limexp}\left(\frac{-(Bv + V1)}{Vt} \right) - 1 + \frac{Bv}{Vt} \right), \quad \forall \ (V1 < -Bv) \tag{6}$$

In these equations, Is is the diode saturation current, N is the emission constant, GMIN is a small conductance representing a large resistance in parallel with the diode (required to aid simulator DC convergence), Bv is the reverse breakdown voltage (entered as a positive number), Ibv is the reverse breakdown voltage (entered as a positive number), and Vt is the thermal voltage at 300 Kelvin. Equation block Eqn2 lists values for GMIN and Vt. Figure 1 illustrates DC simulation results for the EDD diode model together with those for the built-in Qucs diode model with identical parameters.

5. DIODE CAPACITANCE EFFECTS

The next stage in the development of an EDD compact diode model is to add capacitance effects; diffusion and depletion capacitance for the forward and reverse bias regions of operation, respectively. Figure 2 shows the compact EDD diode model with these added via contributions to the device charge. Again the same syntax as the standard SPICE diode model has been adopted in the derivation of the EDD charge equations. Diode diffusion and depletion capacitance are given by equations (7) and (8).

$$C_{diff} = \frac{dQ_{diff}}{dV_1} = Tt \cdot \frac{dI1}{dV1} \tag{7}$$

$$C_{dep} = \frac{dQ_{dep}}{dV_1} = Area \cdot Cj0 \cdot \left(1 - \frac{V_1}{Vj} \right)^{-m} \tag{8}$$

The total stored charge is $Q_d = Q_{diff} + Q_{dep}$. In Figure 2 diode charge is represented in the compact EDD diode model as either stored charge Q1 or stored charge Q2. If-then-else statements select the correct charge equation for each section of the diode DC operating range. Expressions for Q1 and Q2 are given by equations (9) and (10).

$$\begin{aligned} Q1 &= Tt \cdot I1 + Area \cdot Cj0 \int_0^{V1} \left(1 - \frac{V}{Vj} \right)^{-M} dV \\ &= Tt \cdot I1 + \frac{Area \cdot Cj0 \cdot Vj}{1-M} \left\{ 1 - \left(1 - \frac{V1}{Vj} \right)^{1-M} \right\}, \qquad \forall \ (V_1 < Fc \cdot Vj) \end{aligned} \tag{9}$$

$$\begin{aligned} Q2 &= Tt \cdot I1 + Area \cdot Cj0 \cdot \left\{ F1 + \frac{1}{F2} \int_{Fc \cdot Vj}^{V1} \left| F3 + \frac{M \cdot V}{Vj} \right| dV \right\} \\ &= Tt \cdot I1 + Area \cdot Cj0 \cdot \left\{ F1 + \frac{1}{F2} \cdot \left(F3 \cdot (V1 - Fc \cdot Vj) + \left(\frac{M}{2 \cdot Vj} \right) \cdot \left(V1^2 - (Fc \cdot Vj)^2 \right) \right) \right\}, \end{aligned}$$

$$\forall \ (V1 \geq Fc \cdot Vj) \tag{10}$$

In equations (9) and (10) $F1 = \frac{Vj}{1-M} \left\{ 1 - (1 - Fc)^{1-M} \right\}$, $F2 = (1 - Fc)^{1+M}$, $F3 = 1 - Fc \cdot (1 + M)$, Fc is the coefficient for forward bias depletion capacitance, M is a grading coefficient, Tt is the current carrier transit time, Cj0 is the zero bias diode junction capacitance and Vj is the junction potential. Qucs equation block Eqn2 includes expressions for F1, F2 and F3, simplifying the calculation of Q1 and Q2. An area factor has also been added to diode model in Figure 2, scaling variables Is, Cj0 and diode series resistance Rs by the factors given in equation (11).

$$Is(Area) = Is \cdot Area, \ Cj0(Area) = Cj0 \cdot Area, \ \ Rs(Area) = \frac{Rs}{Area} \tag{11}$$

The test circuit shown in Figure 2 demonstrates how Qucs post simulation processing utilises equations to determine device capacitance and resistance as a function of diode bias voltage; firstly the diode S[1,1] parameter is recorded at a each bias voltage and then converted to Y[1,1], from which the diode capacitance and resistance is easily extracted.

6. MODELLING DIODE TEMPERATURE EFFECTS

The EDD compact diode model shown in Figure 3 employs temperatures Tnom and Temp to determine the temperature dependencies of the model parameters. In Figure 3 EDD diode parameters Is, Vj, and Cj0 are specified as functions of temperature given by equations (12) to (14).

$$Is(T2)=Is(T1)\left\{\frac{T2}{T1}\right\}^{\frac{XTi}{N}}\text{limexp}\left|\frac{-Eg(300)}{vt(T2)}\cdot\left(1-\frac{T2}{T1}\right)\right| \quad (12)$$

$$Vj(T2)=\frac{T2}{T1}\cdot Vj(T1)-2\cdot vt(T2)\ \ln\left(\frac{T2}{T1}\right)^{1.5}-\left\{\frac{T2}{T1}\cdot Eg(T1)-Eg(T2)\right\} \quad (13)$$

$$Cj0(T2)=Cj0(T1)\cdot\left|1+M\cdot\left(400E-6\cdot(T2-T1)-\frac{Vj(T2)-Vj(T1)}{Vj(T1)}\right)\right| \quad (14)$$

Where, T1 = Tnom (the parameter measurement temperature), T2 = Temp (the circuit temperature), $vt(T2)$ is the thermal voltage at T2 Kelvin, XTi is the saturation current temperature exponent and the energy gap temperature dependence is given by equation (15).

$$Eg(T)=EG(0)-\frac{7.02E-4\cdot T^2}{1108+T} \quad (15)$$

Where, T is temperature T1 or T2 Kelvin. The circuit shown in Figure 3 sweeps the temperature of the devices under test over the range 20 to 80 Celsius. The graph inlay illustrates the EDD compact diode current plotted as a function of temperature. Comparison between the simulation results for the Qucs built-in diode model and the EDD compact diode model indicates good agreement in the I-V characteristics over a wide temperature range. Device self-heating effects can be modelled by employing one of the EDD branches to monitor an external signal which is proportional to power dissipation.

7. DEVICE MODELS WITH PACKAGE PARASITIC COMPONENTS

Figure 4 gives a compact device model for a p^+-n^+ tunnel diode [6-7]. Series resistance Rs and inductance Ls model the connection between the diode and the anode lead of the device package. In Figure 4 the tunnel diode current is the sum of EDD branch currents I1, I2 and I3, where I1 is the diode thermal current, I2 is the diode tunnelling current and I3 the diode excess current. Expressions for these currents are given by equations (16) to (18).

$$I1 = Ip \cdot \exp\left\{\frac{-Vpp}{Vt}\right\} \cdot \left\{\exp\left(\frac{V1}{Vt}\right) - 1\right\} \quad (16)$$

$$I2 = Ip \cdot \frac{V1}{Vp} \cdot \exp\left\{1 - \frac{V1}{Vp}\right\} \quad (17)$$

$$I3 = Iv \cdot \exp\{V1 - Vv\} \quad (18)$$

Where, Ip and Vp are the diode peak current and voltage, Iv and Vv are the diode valley current and voltage, Vpp is the projected peak diode voltage and Vt is the thermal voltage at 300 Kelvin. Typical values for the tunnel diode EDD parameters are listed under heading SUB1 in Figure 4. Tunnel diode capacitance is represented by a parallel fixed capacitor Cp. This is embedded in branch one of EDD D1. With this arrangement the value of Cp could be made a function of diode voltage or current if a more accurate nonlinear capacitance model, is required. Figure 4 also shows the modelled tunnel diode I-V characteristic.

8. NONLINEAR PASSIVE COMPONENTS

Nonlinear passive components are sometimes present in compact device models. The model and test circuit illustrated in Figure 5 indicates how Qucs EDD handles such situations. The example demonstrates the use of a gyrator plus an EDD to form a nonlinear inductance of the form implemented in SPICE 2g6 [8]. The EDD model is similar to a SPICE 2g6 nonlinear inductance model with four coefficients. This number can be increased by extending the number of terms in the EDD polynomial expression. The effect of nonlinear inductance on the inductance current is clearly shown in Figure 5 by the difference between currents IL_nonlinear and IL.

9. THREE TERMINAL EDD MODELS

The compact device model schematic drawn in Figure 6 is a level one Curtice model of a MESFET [9]. This example demonstrates how multiple EDD, passive components, Qucs equation blocks and subcircuit parameters can be combined to form a three terminal compact device model. Basic temperature effects are also included. The EDD DC I-V and charge equations for the level one Curtice model are listed in (19) to (26).

$$I1 = -IsT \cdot \left(1 + \exp\left\{\frac{-VBR + V1}{Vt}\right\}\right) + GMIN \cdot V1, \quad \forall\ (V1 < -VBR + 50 \cdot Vt) \quad (19)$$

$$I2 = -IsT + GMIN \cdot V1, \quad \forall\ \left(V1 \geq \{-VBR + 50 \cdot Vt\}\right) \text{ and } (V1 < -5 \cdot Vt) \quad (20)$$

$$I2 = IsT \cdot \left(\exp\left\{\frac{V1}{N \cdot Vt}\right\} - 1\right) + GMIN \cdot V1, \quad \forall\ (V1 \geq -5 \cdot Vt) \quad (21)$$

$$I3 = Beta \cdot (V1 - VT0)^2 \cdot (1 + Lambda \cdot V3) \cdot \tanh\{Alpha \cdot V3\}, \quad \forall\ \left((V1 - VT0) > 0\right) \quad (22)$$

$$IsT = Is \cdot \exp\left\{\frac{XTI}{N} \cdot \ln\{TR\} - \frac{Eg}{N \cdot Vt} \cdot (1 - TR)\right\} \quad (23)$$

$$TR = \frac{TK}{TnK},\ TK = Temp + 273.15,\ TnK = Tnom + 273.15 \quad (24)$$

EDD D2 $Q4 = CGS \cdot V4,\ Q3 = CDS \cdot V3 + TAU \cdot I3,$ (25)

EDD D1 $Q1 = CGD \cdot V1$ (26)

Where, EDD D1 voltage V1 is Vgs, EDD D1 voltage V3 is Vds, EDD D2 voltage V1 is Vgd, current Id is the sum of currents I1, I2 and I3, and the remaining parameters are listed in Table 1. Figure 7 gives a DC test circuit and simulated Id-Vds characterstics for the Curtice level one MESFET. Similarly, Figure 8 shows a typical Qucs S-parameter test circuit and characteristics.

10. CONCLUSIONS

The Qucs EDD is an innovative nonlinear component which allows construction of compact device models via the Qucs graphical user interface. In contrast to conventional linear circuit simulation models, the components modelled by EDD may be nonlinear algebraic functions of EDD branch voltages and currents, making the development of compact devices with complex current, voltage and charge characteristics, straightforward. Equation defined devices encourage prototyping of compact device models as a precursor to translation of model equations into Verilog-A and conversion to C/C++, using for example ADMS [10-12], prior to compilation and permanent linking with Qucs [13]. One of the significant advantages of the EDD style of modelling is that it is interactive, allowing easy experimentation with compact models of any level of complexity. However, one EDD attribute is worth commenting on, namely that complex EDD models can show some loss of simulation speed when compared to more traditional C/C++ hand crafted models. In many instances the convenience provided by EDD interactive model prototyping far out ways this loss of speed, especially when one considers that a high percentage of fully debugged models are likely to be translated into Verilog-A and added to Qucs, at some later stage, using the ADMS compiler and Qucs XML interface. Qucs nonlinear EDD represent a major step forward in the development of the simulator's compact device modelling facilities. The EDD approach should be of interest to anyone designing and testing compact device models.

ACKNOWLEDGEMENTS

A poster of this paper was presented at ESSDERC/ESSCIRC MOS-AK Workshop in Munich 2007 [14] and recommended for further publication in the International Journal of Numerical Modelling: Electronic Networks, Devices and Fields.

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Table 1: Qucs EDD model parameters for the Curtice MESFET

Name	Symbol	Description	Unit	Default
RG	R_G	External gate resistance	Ω	1m
RD	R_D	External drain resistance	Ω	1m
RS	R_S	External source resistance	Ω	1m
VBR	V_{BR}	Gate to source breakdown voltage	V	10^{10}
LG	L_G	External gate lead inductance	H	0
LD	L_D	External drain lead inductance	H	0
LS	L_S	External source lead inductance	H	0
Is	Is	Saturation current	A	10f
N	N	Emission coefficient		1
XTi	XTi	Saturation current temperature coefficient		0
EG	E_G	Energy gap	eV	1.11
TAU	τ	Internal delay from drain to source	s	10p
RIN	R_{IN}	CGS series resistance	Ω	1m
CGS	C_{GS}	Interelectrode gate-source bias-independent capacitance	F	300f
CGD	C_{GD}	Interelectrode gate-drain bias-independent capacitance	F	300f
CDS	C_{DS}	Interelectrode drain-source bias-independent capacitance	F	300f
Tnom	Tnom	Device parameter measurement temperature	^oC	26.85
Temp	T	Device temperature	^oC	26.85
Alpha	α	Coefficient of Vds in tanh function for quadratic model	V^{-1}	0.8
Beta	β	Transconductance parameter	AV^{-2}	3m
Lambda	λ	Channel length modulation parameter	V^{-1}	40m
VTO	VTO	Quadratic model threshold voltage	V	-6

Figure Captions

Figure 1: DC diode model test circuit and characteristics; SUB1 is the EDD model and D1 the Qucs diode model with the same parameters.

Figure 2: Large signal EDD diode model, capacitance and resistance test circuit and characteristics.

Figure 3: EDD diode temperature model, temperature scan test circuit and Id-temperature characteristics.

Figure 4: Tunnel diode EDD model, test circuit and Itd-Vtd characteristic.

Figure 5: SPICE 2g6 style nonlinear inductance model, test circuit and signal waveforms.

Figure 6: An EDD implementation of a level one Curtice model of a MESFET.

Figure 7: MESFET DC test circuit and Ids-Vgs characteristics.

Figure 8: MESFET S parameter test circuit and characteristics.