Original Articles

A Hybrid Verilog-A and Equation-defined Subcircuit Approach to MOS Switched Current Analog Cell Simulation

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Abstract

Conventional modeling and simulation of two-phase switched current MOS-integrated circuits is normally undertaken at semiconductor device level. This allows primary and secondary circuit effects to be studied and characterized. However, with the growing complexity of these circuits, transient domain simulation times can become prohibitively long, restricting the size of circuit that can be easily investigated. Measurable reductions in transient simulation run times can be achieved by modeling part, or all, of a switched current design as a macromodel. This paper introduces a hybrid approach to MOS switched current circuit modeling that combines the primary features of compact device modeling with functional circuit macromodeling. To illustrate the proposed hybrid modeling procedure the properties, and simulation model, of a MOS switched current analog memory cell are described. The material presented also demonstrates how recent trends in "Quite universal circuit simulator" (QUCS) technology promote embedded Verilog-A models and equation-defined subcircuits as integral elements in mixed-mode circuit and system design.

Keywords: Circuit macromodels, Compact semiconductor device models, Equation-defined device modeling, QUCS universal circuit simulator, Switched current analog integrated circuits, Verilog-A