SPICE to QucsStudio via Qucs: An international project to develop a freely available GNU Public Licence circuit simulator with compact device modelling tools, data processing capabilities, manufacturing features and an analogue/RF design environment for engineers.

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- Background: Qucs and QucsStudio development road maps
- Circuit simulation: SPICE and Qucs forms of simulation
- Device and circuit modelling with subcircuits, macromodels, equation-defined devices and Verilog-A compiled models
- QucsStudio compact semiconductor modelling extensions
- The development of a QucsStudio Verilog-A MESFET model
- Simulation output data processing with Octave
- QucsStudio system simulation
- QucsStudio – future directions
- Summary
- References

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Background: Qucs development road map

Date	Release Notes [Highlights]	
Dec. 2003	0.0.1	First public version of simulator - very basic.
Jun. 2004	0.0.2	First MacOS version.
Sep. 2004	0.0.3	Implemented S-parameters and noise analysis. Added microstrip components and BJT and MOSFET devices.
Mar. 2005	0.0.5	Implemented AC analysis and basic transient analysis.
May 2005	0.0.6	Mainly bug fixes and extensions to implemented analysis.
Jul. 2005	0.0.7	Windows ® 32 version. Simulator renamed as Qucs. New device library manager. Added post simulation data processing mathematical functions.
Jan. 2006	0.0.8	Support for pure digital simulation using FreeHDL. Added many new component models. Improved post simulation data plotting features. Added a filter synthesis tool.
May 2006	0.0.9	New functions in equation solver. Harmonic Balance simulation introduced. Many new components added.
Sept. 2006	0.0.10	Qucs converter tool improved. Support for nine-valued VHDL logic. Circuit optimization introduced using ASCO. Added attenuator design tool.
Mar. 2007	0.0.11	Added device parameters to equations and parameters to subcircuits. New models plus improvements to existing models. Using ADMS to translate Verilog-A device models for use in Qucs.
Jun. 2007	0.0.12	Lots of new components, bug fixes and small improvements. Added support for Verilog using Icarus Verilog. Support for symbolically equation-defined devices (EDD). Explicit equations allowed.
Nov. 2007	0.0.13	General improvements plus implementation of immediate vectors and matrices in equations.
Apr. 2008	0.0.14	Implemented multi-port equation-defined RF device (RFEDD) S, Y and Z parameters available. Two-port equation-defined device also supported.
Apr. 2009	0.0.15	Mainly bug fixes, small improvements and the addition of new models.
Mar. 2011	0.0.16	Implemented interactive post simulation data processing using Octave. Again many bug fixes, small improvements and the addition of new models.

Background: QucsStudio development road map

Date	Release Notes [Highlights]	
Feb. 2011	1.0.0	First public version of simulator- features include more than 100 circuit components, DC analysis, AC analysis (including noise analysis and noise distribution analysis), S-parameter analysis (including noise simulation), transient analysis, Harmonic Balance analysis (including noise simulation), system simulation, parameter sweep and optimization of analogue circuits, digital simulation with ICARUS Verilog,PCB layout using KiCAD, numerical data processing using Octave, RF transmission line calculation (coaxial, microstrip, coupled microstrip, coplanar line, stripline, twisted pair rectangular wavequide etc., filter synthesis (LC ladder, stepped-impedance, microstrip, active filters etc., attenuator synthesis, and GPIB control.
Mar. 2011	1.1.0	Added VHDL digital simulation with GHDL plus numerous bug fixes.
Jun. 2011	1.2.0	Many small improvements plus bug fixes.
Nov. 2011	1.3.0	Added compiled C++ and Verilog-A device and circuit models using MinGW and ADMS, more bug fixes and small improvements. Released QucsStudio-light: QucsStudio without Octave and model Compiler.
Feb. 2012	1.3.1	Added large signal AC circuit simulation using Harmonic Balance. Many small improvements plus bug fixes. Range of compact semiconductor device models released: Verilog-A models held in binary C++ library.

SPICE and Qucs basic types of simulation facilities

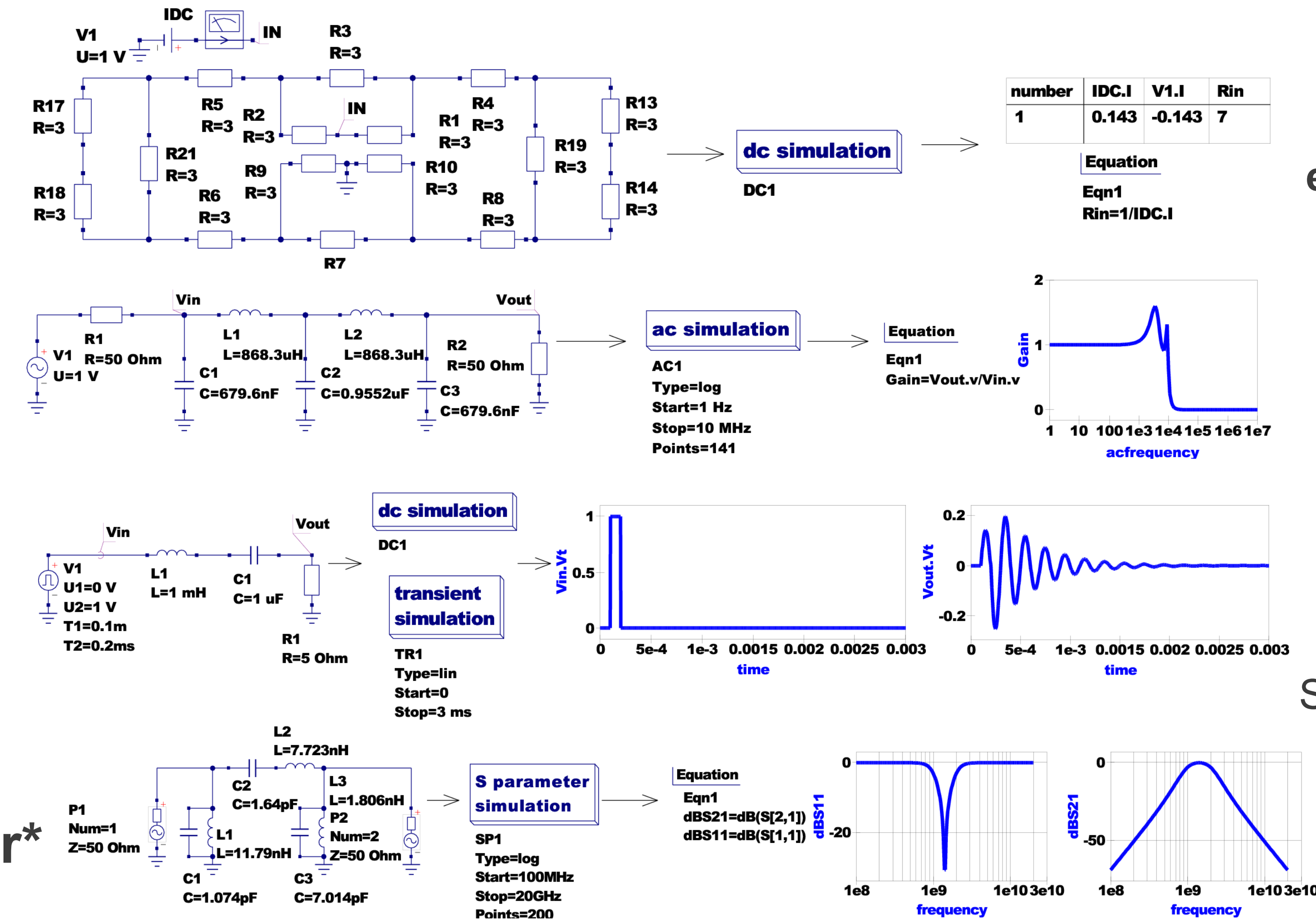
Schematic capture: generates circuit diagram → **Circuit simulation: DC, AC, TRAN, S-parameter, noise and Harmonic Balance** → **Post simulation data processing and visualization**

DC

AC

TRAN

S-parameter*



Circuit encoding

↓

SPICE 2g6 and 3f5 NETLIST

↓

Qucs Schematic diagram

*Implementation 1. Qucs: built-in; 2. SPICE: via RCL networks

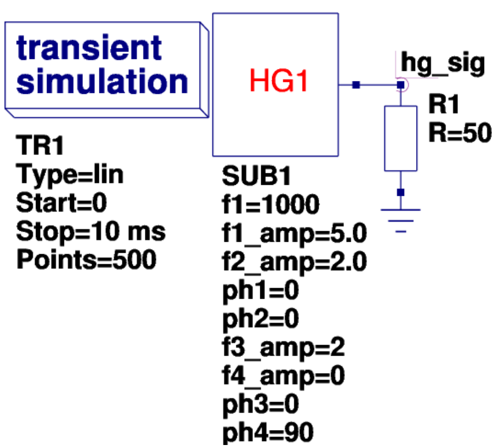
Qucs post-simulation MATLAB®*/Octave** data processing features

Equation blocks + simulation data sets → Data processing → Tables and plots

Constants: i, j, pi, e, kB, q
Immediate: 2.5, 1.4+j5.1, [1, 3, 4, 5, 7], [11, 12; 21, 22]
Ranges: Lo:Hi, :Hi, Lo:, :
Logical operators: !x, x&&y, x||y, x^^y, x?y:z, x==y, x!=y, x<y, x<=y,x>y, x>=y

Number suffixes: E, P, T, G, M, k, m, u, n, p, f, a
Matrices: M, M[2,3], M[:,3]
Arithmetic operators: +x, -x, x+y, x-y, x*y, x/y, x%y, x^y

abs adjoint angle arccos arccosec arccot arcosech arcosh arcoth arcsec arcsin arctan arg arsech arsinh artanh avg besseli0 besselj bessely ceil conj cos cosec cosech cosh cot coth cumavg cumprod cumsum dB dbm dbm2w deg2rad det dft diff erf erfc erfcinv erfinv exp eye fft fix floor Freq2Time GaCircle GpCircle hypot idft ifft imag integrate interpolate inverse kbd limexp linspace ln log10 log2 logspace mag max min Mu Mu2 NoiseCircle norm phase PlotVs polar prod rad2deg random real rms Rollet round rtoswr rtoy rtoz runavg sec sech sign sin sinc sinh sqr sqrt srandom StabCircleL StabCircleS StabFactor StabMeasure stddev step stos stoy stoz sum tan tanh Time2Freq transpose twoport unwrap variance vt w2dbm xvalue ytor ytos ytoz yvalue ztor ztos ztoy

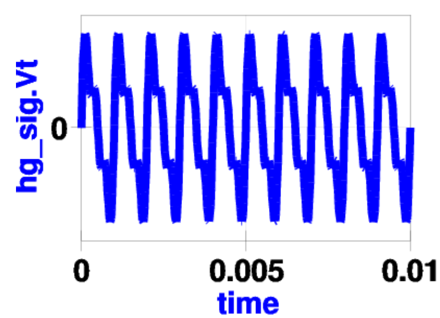


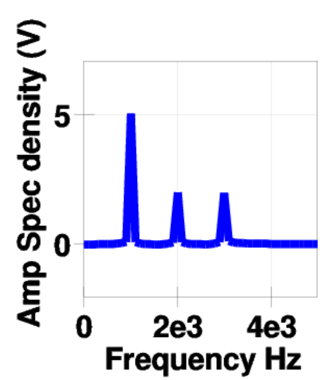
Equation

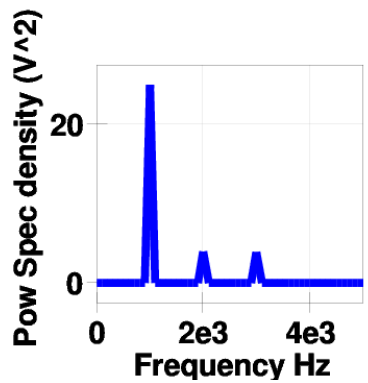
```
Eqn1
ts=(max(time)-min(time))/length(time)
fs=1/ts
Adft=dft(hg_sig.Vt)
LAdft=length(hg_sig.Vt)
Amp2=2*Adft[1:(LAdfto2)-1]
LAdfto2=LAdft/2
Amp_squared=Adft[:LAdfto2]*conj(Adft[:LAdfto2])
Amp=sqrt(Amp_squared)
f_bin=linspace(1, LAdfto2, LAdfto2)
f=(f_bin-1)*fs/LAdft
PLAmp=PlotVs(2*Amp/LAdft,f)
PLPower=PlotVs(4*Amp*Amp/(LAdft*LAdft),f)
```

* MATLAB, Mathworks, http://www.mathworks.com/
** Octave, http://www.gnu.org/software/octave/

Limitations: NO user defined functions or control loops

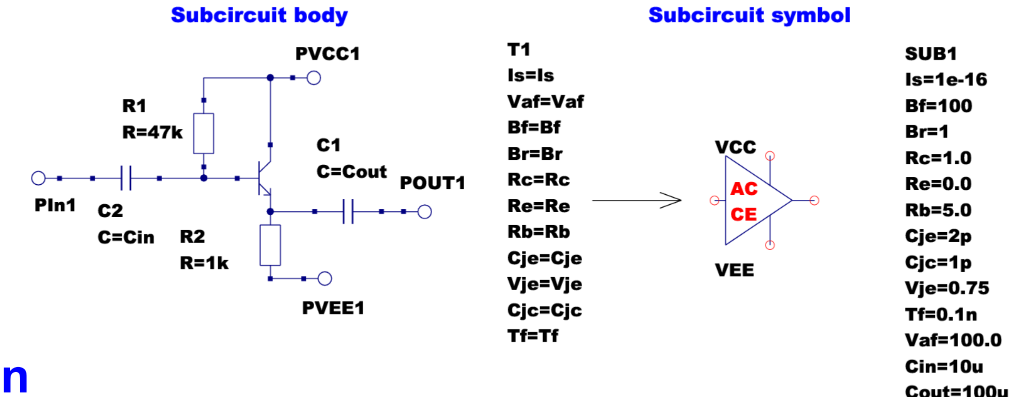




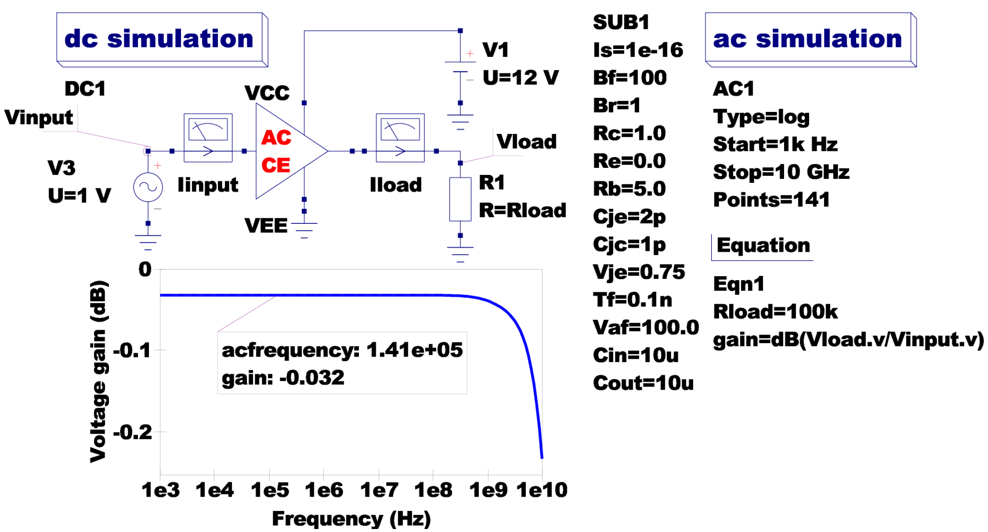


Qucs modelling tools: Subcircuits with parameters

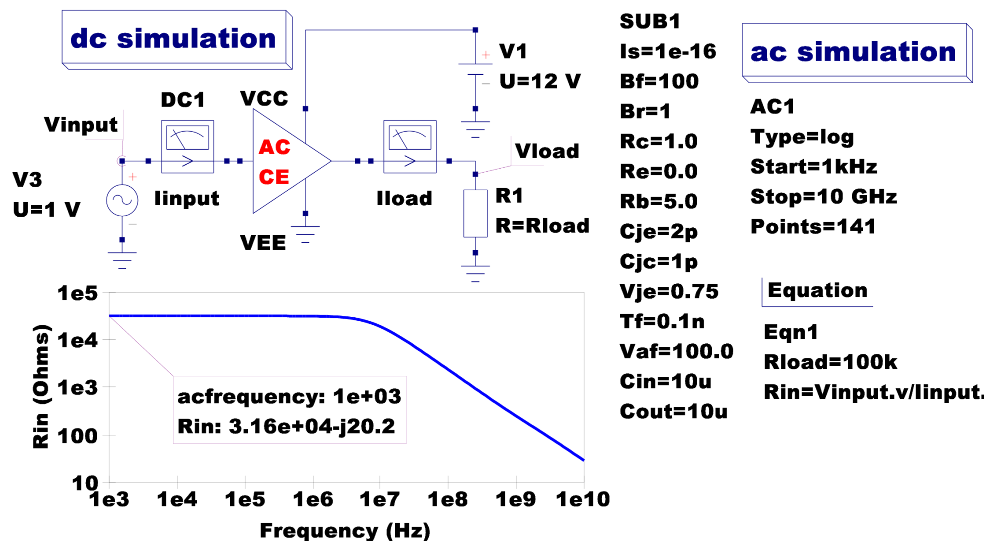
Emitter follower subcircuit



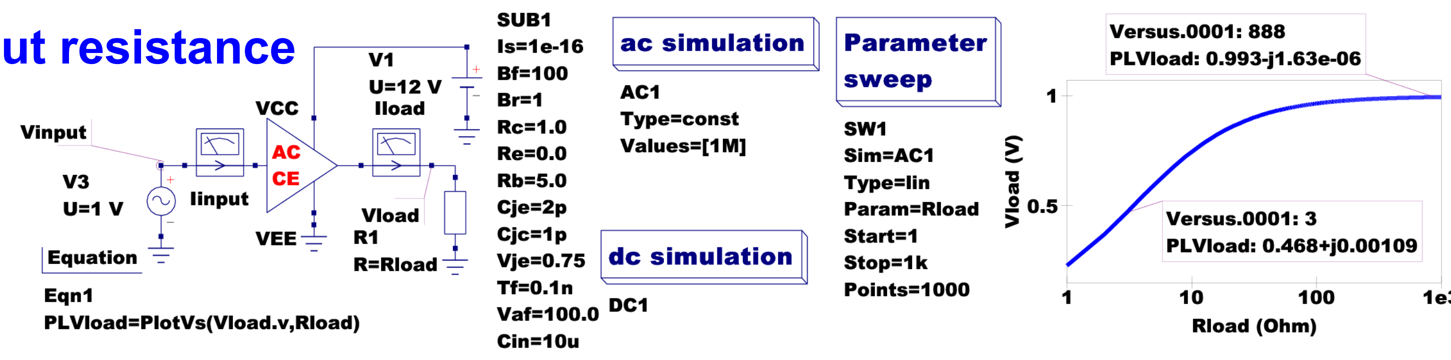
Voltage gain



Input resistance



Output resistance



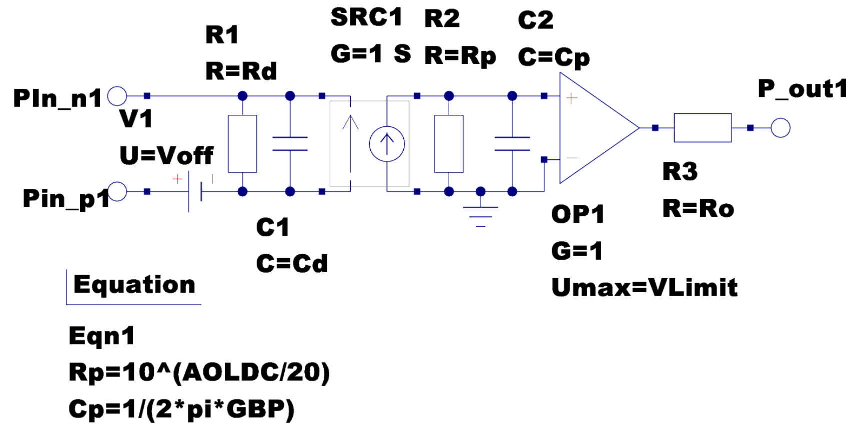
Qucs
Quite Universal Circuit Simulator

Qucs modelling tools: Macromodels with parameters

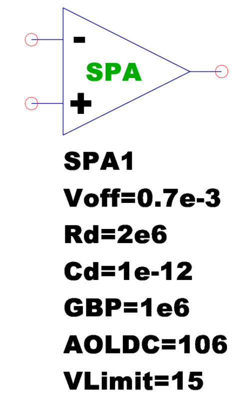
Single pole OP AMP macromodel specification:

Voff = Input offset voltage
Rd = differential input resistance
Cd = differential input capacitance
AOLDC = DC open loop differential voltage gain
GBP = Gain bandwidth product
Vlimit = output voltage saturation limit
Ro = Output resistance

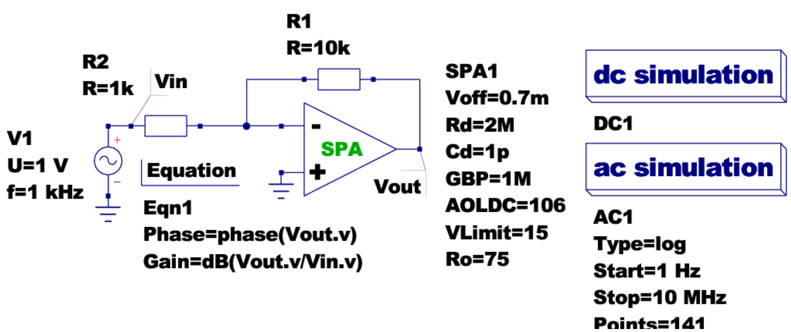
Macromodel body

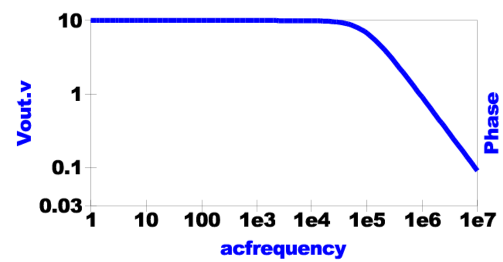


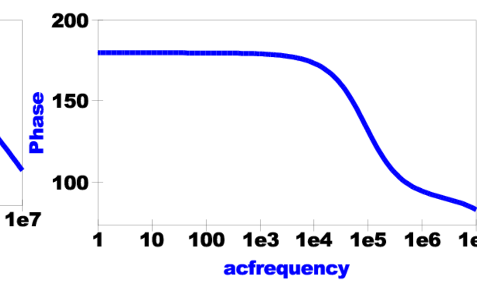
Macromodel symbol



Closed loop amplifier with x10 gain



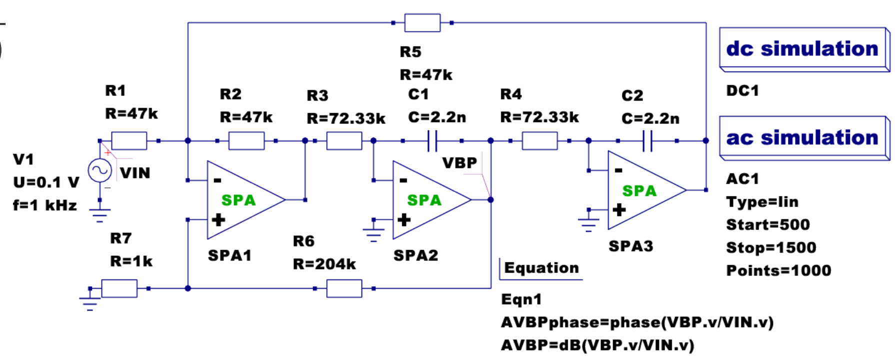


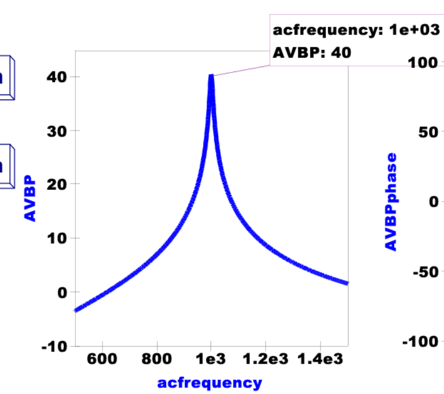


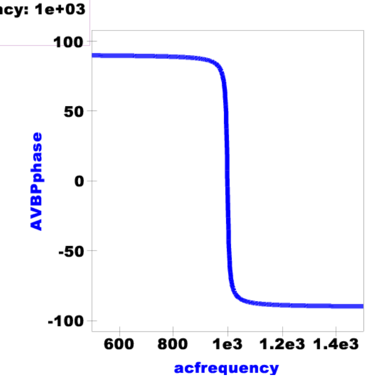
$$VBP = \frac{j\,f/f_0}{1-(f/f_0)^2+(j/Q)(f/f_0)}$$

$$f_0 = \frac{1}{2\pi R_3 C_1} = \frac{1}{2\pi R_4 C_3}$$

$$Q = \frac{1}{3}\left(1+\frac{R_6}{R_7}\right)$$





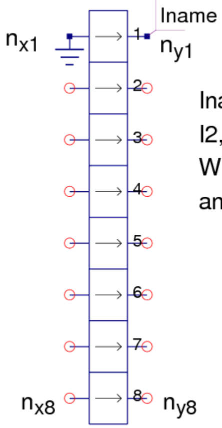
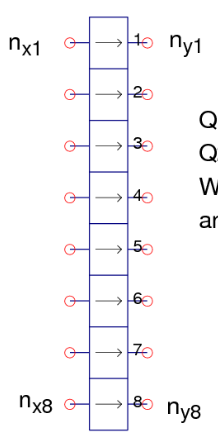


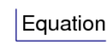
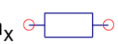
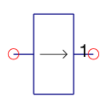
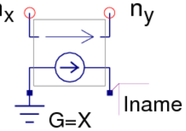
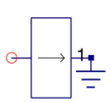
Three OP AMP state variable filter

Qucs modelling tools: Equation-defined device (EDD) modelling

Relationships between Qucs schematic symbols and Verilog-A code fragments

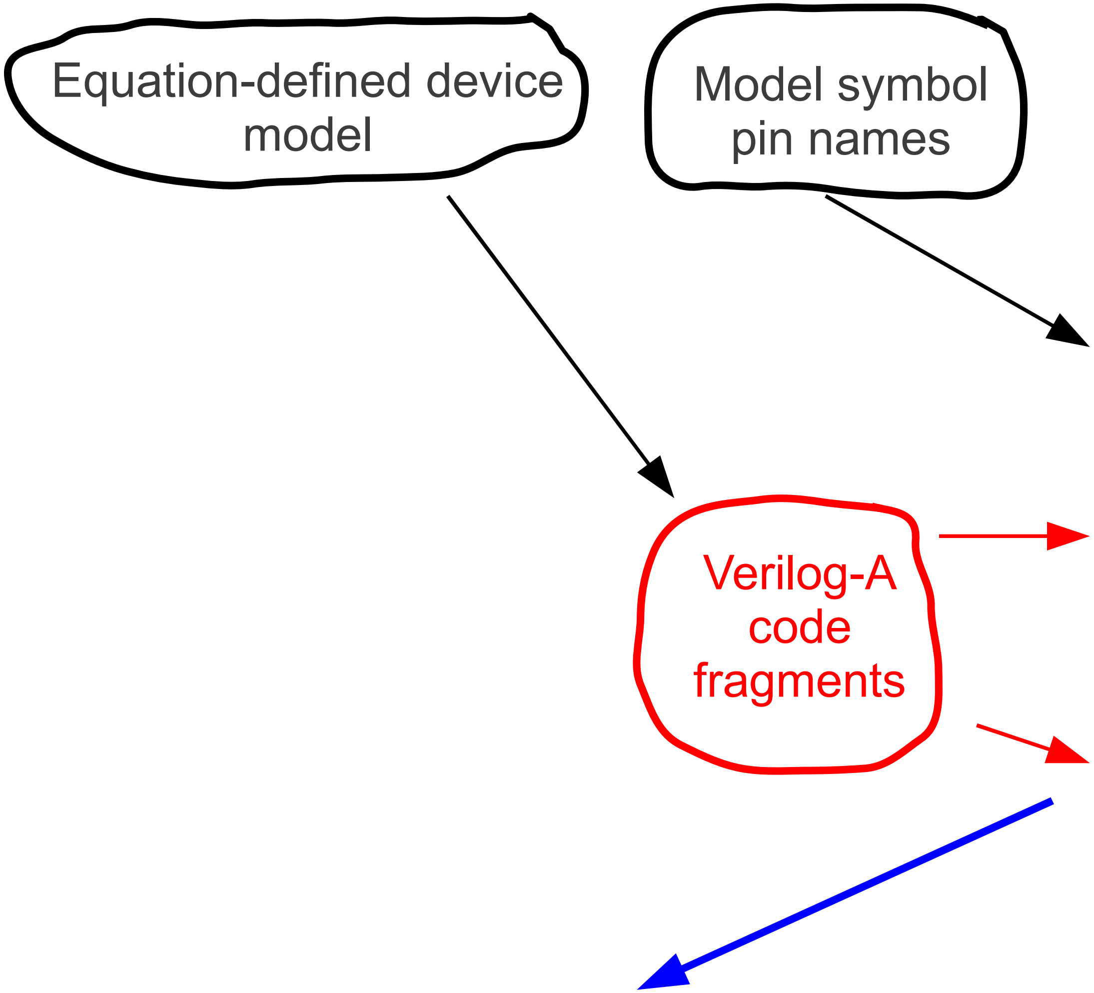
Fundamental EDD blocks

Qucs symbol	Quantity equations	Verilog-A code fragment
	Iname = I1 = f(V2, V3, ... V8) I2, I3, ... I8 = 0 and Q1, Q2, ... Q8 = 0. Where $Vm = V(n_{xm}, n_{ym})$ or $Vm = V(n_{xm})$, and $2 \le m \le 8$.	Iname = f(V2, V3, ... V8); Or Iname <+ f(V2, V3, ... V8);
	Q1 = f(V1, V2, ... V8, I1, I2, ... I8) Q2, ... Q8 = 0. Where $Vm = V(n_{xm}, n_{ym})$ or $Vm = V(n_{xm})$, and $1 \le m \le 8$.	$I(n_{x1}, n_{y1})$ <+ ddt(Q1); Or $I(n_{x1}, n_{y1})$ = ddt(Q1);

	Quantity equations	Verlog-A code fragment
(a) Model initialisation block	 Eqn1 con1= ...... con2= ...... con3=	@(initial_model) begin con1 = ...; con2 = ...; con3 = ...; end
(b) Standard resistors	 n_x n_y R=R	$I(n_x, n_y)$ <+ $V(n_x, n_y)$/R; $I(n_x, n_y)$ <+ white_noise((FourKT/R, "thermal"); Where FourKT = 4.0 · \`P_K · \$temperature, and \`P_K = 1.3806505e-23 K^{-1}, \$temperature is the resistor temperature in Kelvin.
(c) Noise free resistors	 n_x n_y I1 = V1/R = $V(n_x, n_y)$/R	$I(n_x, n_y)$ <+ $V(n_x, n_y)$/R;
(d) Voltage controlled current block	 n_x n_y Iname G=X Iname = X · $V(n_x, n_y)$	Iname = X*$V(n_x, n_y)$;
(e) current to voltage conversion block	 n_x Iname = I1 = V1	Iname = $V(n_x)$;

Qucs modelling tools: Verilog-A compact device modelling

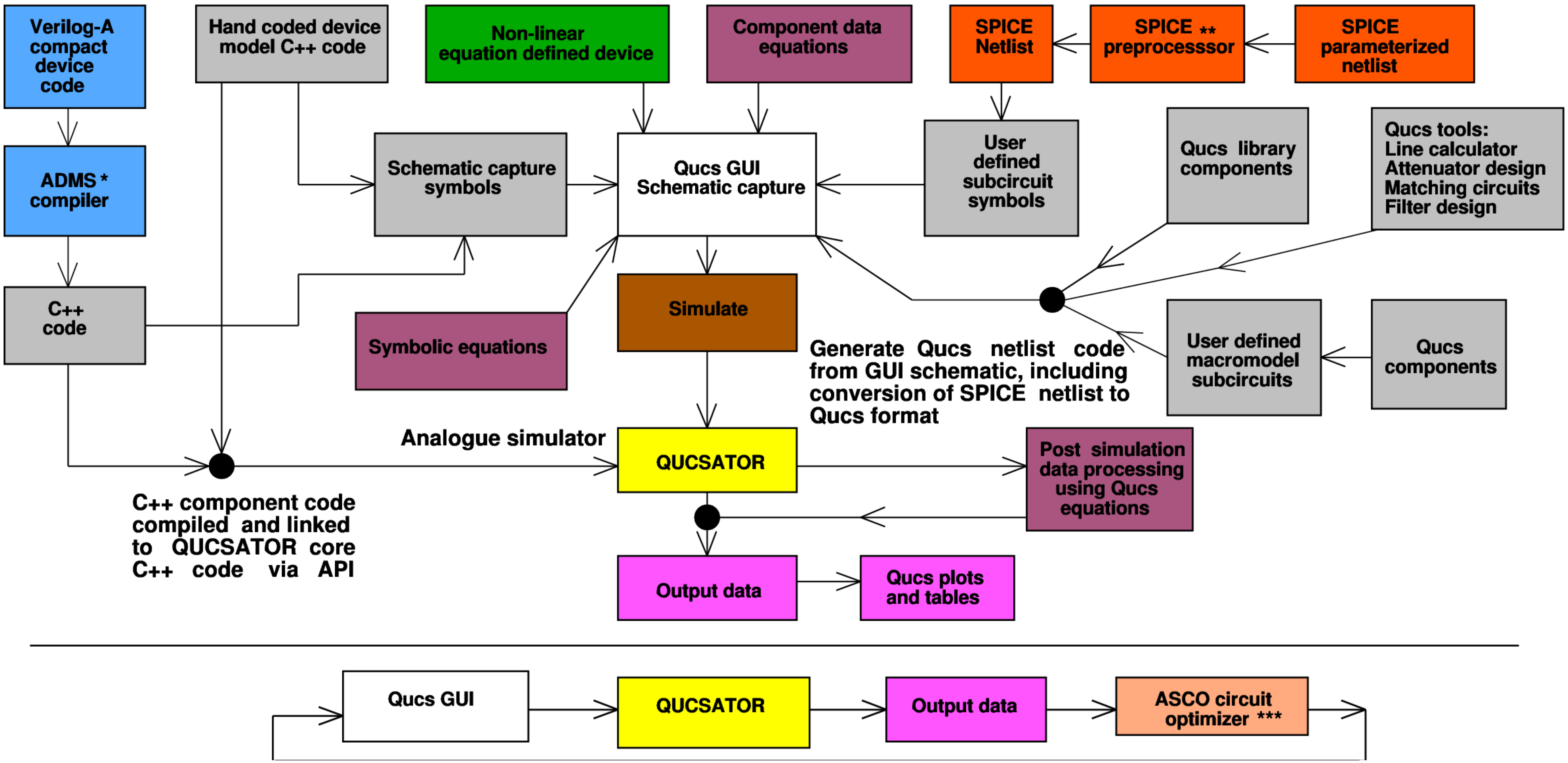
Generating Verilog-A code: From Qucs equation-defined devices via Verilog-A code fragments to a Verilog-A standardised template




```
//Verilog-A model template
`include “disciplines.vams”
`include “constants.vams”
module name (P1, P2, P3, ....... Pn);
inout P1, P2, P3, ....Pn;
electrical P1, P2, P3, ..... Pn;
// Definition of local internal nodes
// Parameter values and descriptions
// Definition of internal variables
analog begin
// Initialisation code
// Quantity equations
// Current contributions
// Noise contributions
end
endmodule
```

1. Compile Verilog-A template code with ADMS
2. Add new model to Qucs by patching C++ code
3. Add new model symbol to Qucs C++ code
4. Compile and link Qucs **static** C++ code to generate new version of Qucs

Qucs: Analogue circuit simulation and device modelling features



QucsStudio changes

- QUCSATOR replaced by new analogue circuit simulator
- Octave simulation output data processing added
- KiCAD PCB layout software added
- Communications system simulation added
- New C++ component added which allows "turn-key" Verilog-A compact model development

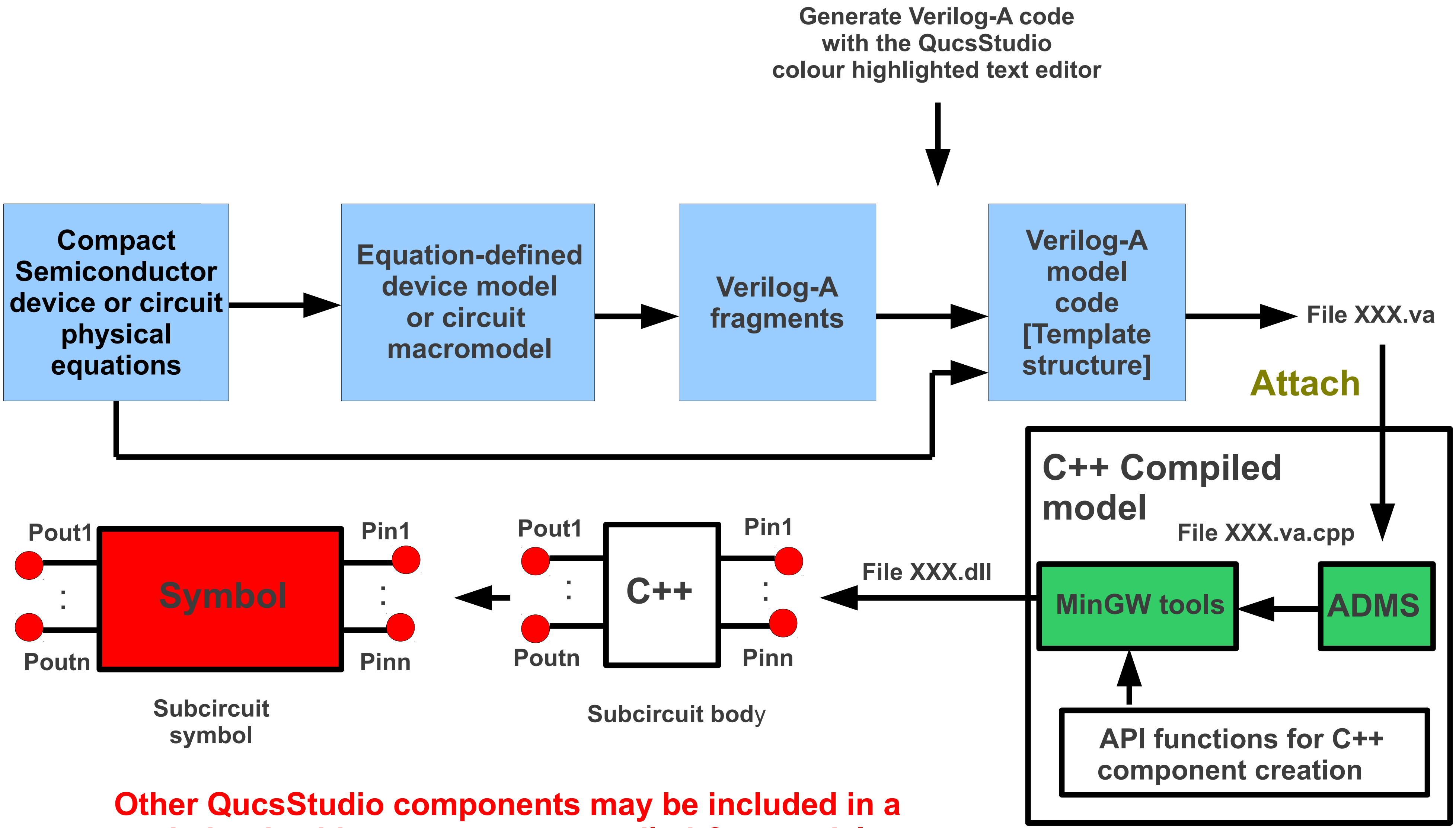
* ADMS – Automatic device model synthesizer, http://sourceforge.net/projects/mot-adms

** PS2SP - SPICE PSpice to SPICE preprocessor, http://members.aon.at/fschmid7/

*** ASCO - A SPICE circuit optimizer, http://asco.sourceforge.net

Qucs and QucsStudio also allow digital simulation with VHDL and Verilog

QucsStudio: Compact semiconductor device and circuit macromodel construction using ADMS and MinGW dynamically linked models



Other QucsStudio components may be included in a subcircuit with one or more compiled C++ models

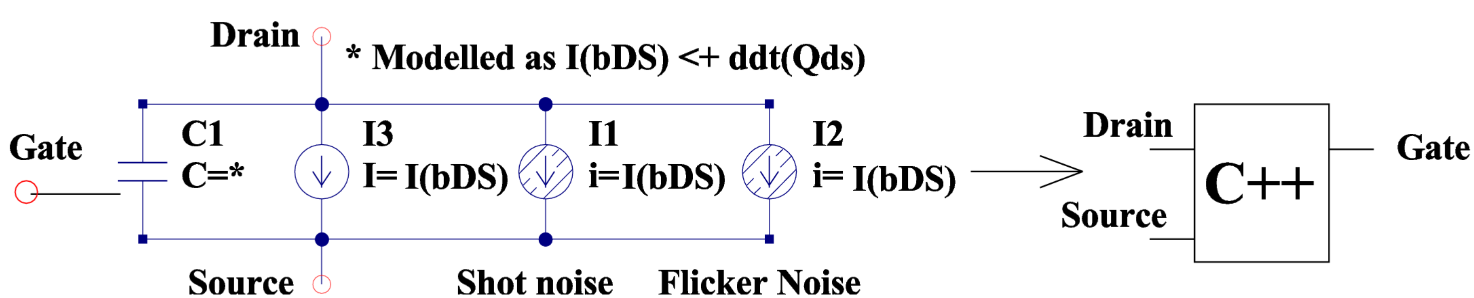
"Turn-Key" Verilog-A compact model development system WHERE the Verilog-A code is automatically recompiled ONLY if it has been changed prior to the start of a simulation

QucsStudio: RF Curtice MESFET compact model
Part 1: Verilog-A code

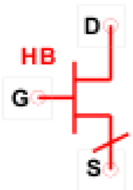
```
//  Verilog-A Curtice MESFET: hyperbolic tangent model
//   with fixed capacitance and noise ; Curtice.va.
//   This is free software; you can redistribute it and/or modify
//   it under the terms of the GNU General Public License as published by
//   the Free Software Foundation; either version 2, or (at your option)
//   any later version.
//
//   Copyright (C), Mike Brinson, mbrin72043@yahoo.co.uk
//                QucsStudio version September 2011.
//
`include "disciplines.vams"
`include "constants.vams"
//
module Curtice(Drain, Gate, Source);
inout Drain, Gate, Source;
electrical Drain, Gate, Source;
//
`define attr(txt) (*txt*)
`define CTOK 273.15
`define K1 7.02e-4
`define K2 1108.0
`define K3 400e-6
`define GMIN 1e-12

//
parameter real Area = 1 from (1 : inf)        `attr(info="area factor" );
parameter real Vto = -1.8 from (-inf : inf)   `attr(info="pinch-off voltage" unit = "V");
parameter real Beta = 3e-3 from [1e-9 : inf)  `attr(info="transconductance parameter" unit = "A/(V*V)");
parameter real Alpha = 2.25 from [1e-9 : inf) `attr(info="saturation voltage parameter" unit="1/V" );
parameter real Lambda = 0.05 from [1e-9 :inf) `attr(info="channel length modulation parameter" unit="1/V");
parameter real Vtotc = 0 from (-inf : inf)    `attr(info="Vto temperature coefficient");
parameter real Betatc = 0 from (-inf : inf)   `attr(info="Beta temperature coefficient" unit = "%/Celsius");
parameter real Alphatc = 0 from (-inf : inf]  `attr(info="Alpha temperature coefficient" unit = "%/Celsius");
parameter real Eg = 1.11 from [1e-6 : inf)    `attr(info="energy gap" unit = "eV");
parameter real Tau = 1e-9 from [1e-20 : inf)  `attr(info="transit time under gate" unit = "s");
parameter real Is = 1e-14 from [1e-20 : inf)  `attr(info="diode saturation current" unit = "I");
parameter real N = 1 from [1e-9 : inf)        `attr(info="diode emission coefficient");
parameter real Xti = 3.0 from [1e-9 : inf)    `attr(info="diode saturation current temperature coefficient");
parameter real Af = 1 from [0 : inf)          `attr(info="flicker noise exponent");
parameter real Kf = 0 from [0 : inf)          `attr(info="flicker noise coefficient");
parameter real Gdsnoi = 1 from [0 : inf)      `attr(info="shot noise coefficient");
parameter real Bv = 1e9 from (-inf : inf)     `attr(info="drain-gate junction reverse bias breakdown voltage" unit = "V" );
parameter real R1 = 1e9 from [1e-9 : inf)     `attr(info="breakdown slope resistance" unit = "Ohms");
parameter real Nsc = 1 from [1e-9 : inf)      `attr(info="subthreshold conductance parameter");
parameter real Temp = 26.85 from [-273 : inf) `attr(info="circuit temperature" unit = "Celsius");
parameter real Tnom = 26.85 from [-273 : inf) `attr(info="parameter measurement temperature" unit = "Celsius");
```

QucsStudio: RF Curtice MESFET compact model
Part 1: Verilog-A code continued

```
real T1, T2, Vt_T2, Vto_T2, Rg_T2, Rd_T2, Rs_T2, Vf, Ah, Beta_T2, Ids;
real Tr, con1, Eg_T1, Eg_T2, Qds;
real Cgs_T2,Cgd_T2, Vbi_T2;      real Igs1, Igs2, Is_T2;
real con2, con3, VfDC;     real fourkt, gm, An, thermal_pwr, flicker_pwr, Alpha_T2;
// Model branches
branch (Drain, Source) bDS;   branch (Gate, Source)  bGS;     branch (Gate, Drain)   bGD;
//
analog begin
 T1=Tnom+`CTOK;     T2 = $temperature;     Tr=T2/T1;      Vt_T2 = $vt;
 Eg_T1=Eg-`K1*T1*T1/(`K2+T1);     Vto_T2=Vto+Vtotc*(T2-T1);
 Beta_T2=Area*Beta*pow(1.01, Betatc*(T2-T1));
 Is_T2=Area*Is*pow( Tr, (Xti/N))*limexp(-(`P_Q*Eg_T1)*(1-Tr)/(`P_K*T2));
 con2 = -5.0*N*Vt_T2;       con3 = 1.0/(N*Vt_T2);  fourkt=Area*4.0*`P_K*T2;
 Alpha_T2=Alpha*( pow( 1.01, Alphatc*(T2-T1)));
// Drain to source current with subthreshold modification
 VfDC = V(bGS)-Vto_T2;     Ah = 1/(2*Vt_T2*Nsc);   Vf = ln(1+exp(Ah*VfDC))/Ah;
 Ids = Beta_T2*Vf*Vf*(1+Lambda*V(bDS))*tanh(Alpha*V(bDS));
// Charge equations
 Qds = Tau*Ids;
// Diode DC equations
 Igs1 = (V(bGS) > con2) ? Is_T2*( limexp(V(bGS)*con3) -1.0) : -Is_T2;
 Igs2 = (V(bGS) < -Bv)  ? (V(bGS)+Bv)/R1 : 0.0;
// Current contributions
 I(bGS) <+ Igs1+Igs2+`GMIN*V(bGS);   I(bDS) <+ Ids;   I(bDS) <+ ddt(Qds);
// Model noise equations
   gm = 2*Ids/VfDC;
                    if ( V(bDS) < 3/Alpha )
                      begin
                        An=1-V(bDS)/VfDC;
                        thermal_pwr= (8*`P_K*T2*gm/3)*((1+An+An*An)/(1+An))*Gdsnoi;
                      end
                    else
                    thermal_pwr=(8*`P_K*T2*gm/3)*Gdsnoi;
                I(bDS) <+ white_noise(thermal_pwr, "thermal");   flicker_pwr = Kf*pow(Ids,Af);
                I(bDS) <+ flicker_noise(flicker_pwr,1.0, "flicker");
end
endmodule
```

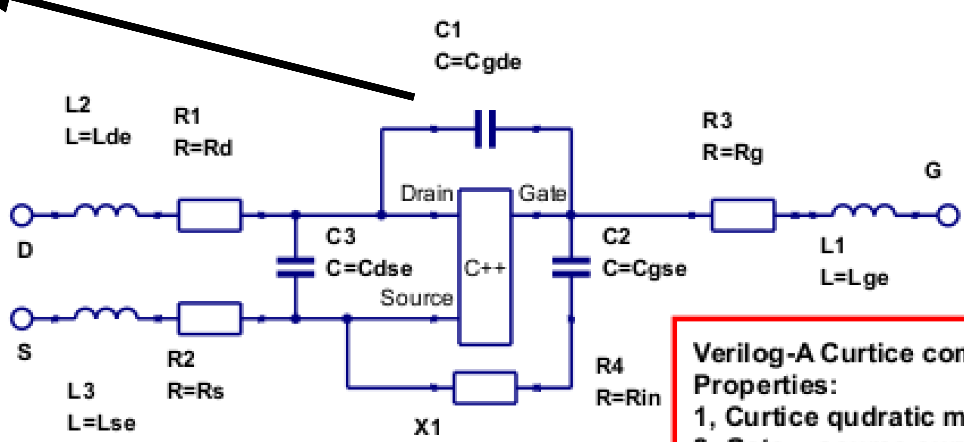


QucsStudio: RF Curtice MESFET compact model
Part 2: Model Schematic



CURTICE
Area=1
Vto=-1.8
Beta=3e-3
Alpha=2.25
Lambda=0.05
Vtotc=0
Betatc=0
Alphatc=0
Eg=1.11
Tau=1e-9
Is=1e-14
N=1
Xti=3.0
Af=1
Kf=0
Gdsnoi=1
Bv=1e9
R1=1e9
Temp=26.85
Tnom=26.85
Cgse=300f
Cgde=30f
Cdse=300f
Lge=0.0
Lde=0.0
Lse=0.0
Nsc=1
Rg=5.1
Rd=1.3
Rs=1.3
Rin=1e-3

MESFET Symbol and parameters



X1
File=Curtice.va
Area=Area
Vto=Vto
Beta=Beta
Alpha=Alpha
Lambda=Lambda
Vtotc=Vtotc
Betatc=Betatc
Alphatc=Alphatc
Eg=Eg
Tau=Tau
Is=Is
N=N
Xti=Xti
Af=Af
Kf=Kf
Gdsnoi=Gdsnoi
Bv=Bv
R1=R1
Nsc=Nsc
Temp=Temp
Tnom=Tnom

MESFET subcircuit body

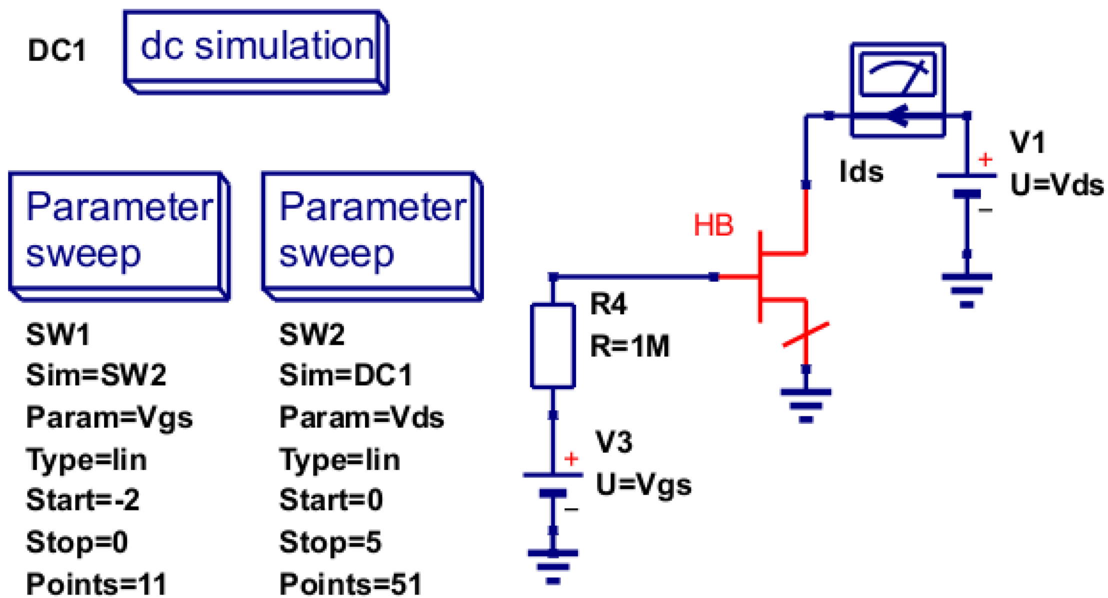
Verilog-A Curtice compact semiconductor device model for an n type MESFET
Properties:
1, Curtice qudratic model - basic plus subthreshold improvement [1]
2. Gate - source current model - exponential diode model plus linear reverse breakdown model.
4. Series terminal resistors Rd, Rg and Rs
5. Thermal noise generated by Rd, Rg and Rs
6. Channel noise
7. Gate noise
8. Flicker noise
9. Bias independant capacitors Cgse, Cgde and Cdse.
10. External inductance: Lge, Lde and Lse.
==

[1] W.R Curtice,"A MESFET model for use in the design of GaAs integrated circuits", IEEE Transactions on Microwave Theory and Techniques, MTT-28, pp. 448-456, 1980.

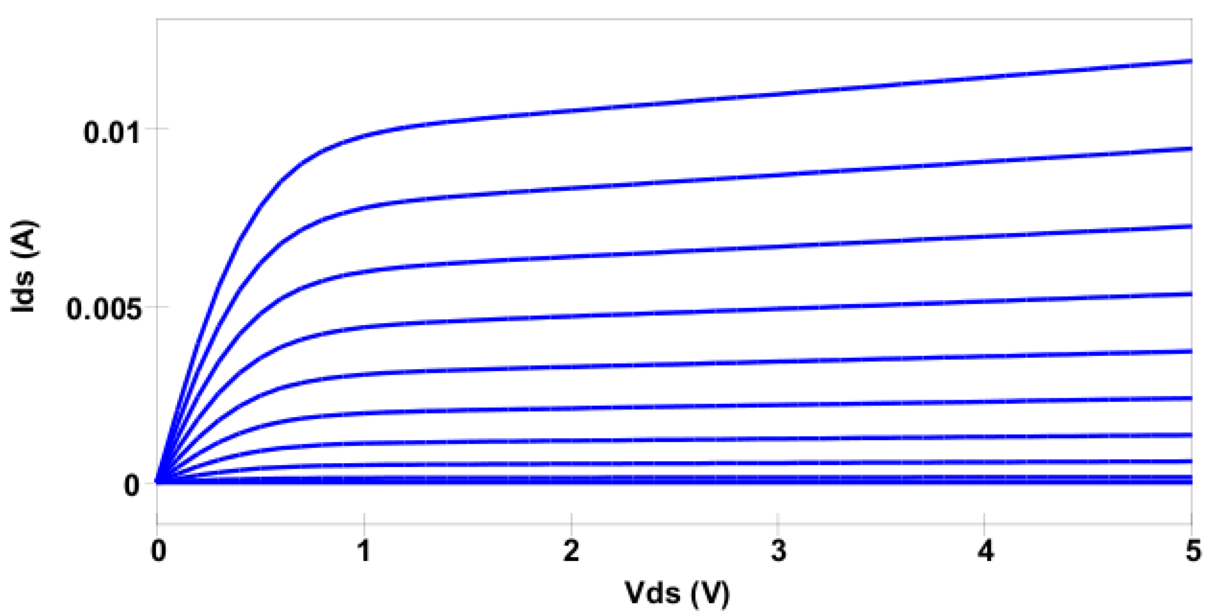
Verilog-A model parameters are listed and described in file Curtice.va.

QucsStudio: RF Curtice MESFET compact model
Part 3: Test simulations

DC

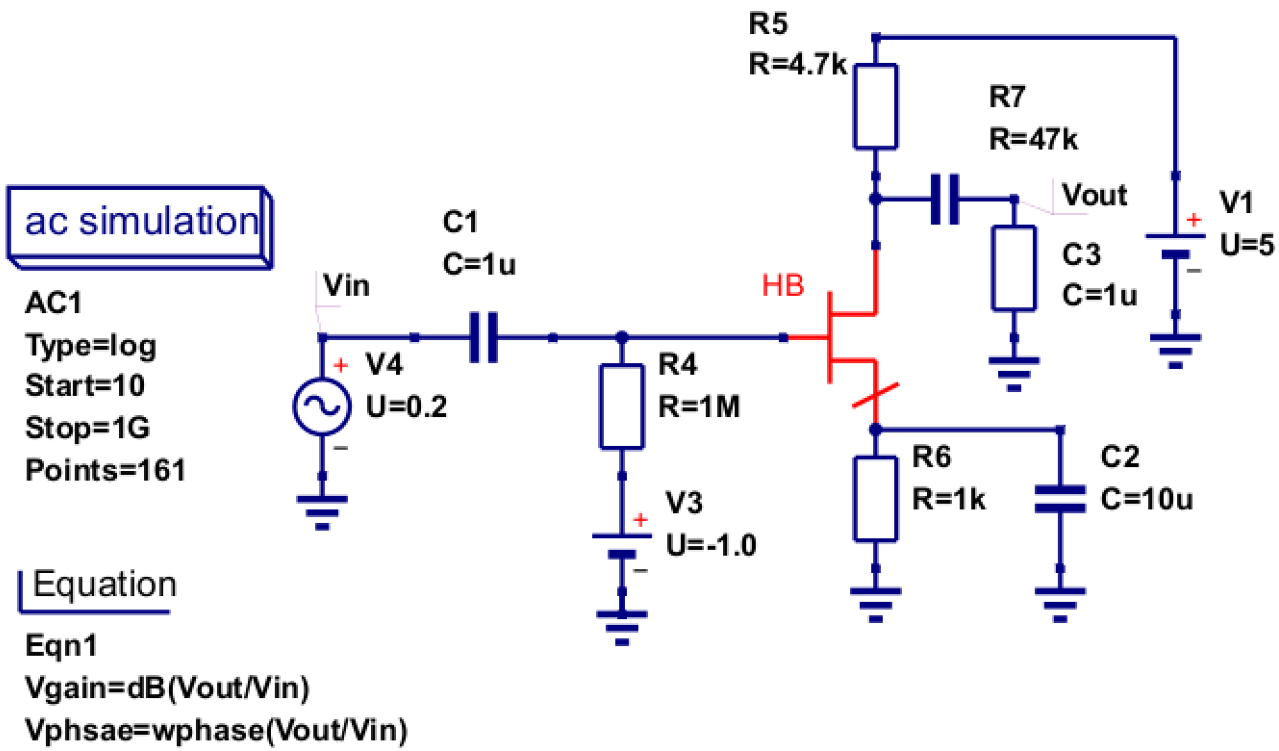


CURTICE1
Area=1
Vto=-1.8
Beta=3e-3
Alpha=2.25
Lambda=0.05
Vtotc=0
Betatc=0
Alphatc=0
Eg=1.11
Tau=1e-9
Is=1e-14
N=1
Xti=3.0
Af=1
Kf=0
Gdsnoi=1
Bv=1e9
R1=1e9
Temp=26.85
Tnom=26.85
Cgse=300f
Cgde=30f
Cdse=300f
Lge=0.0
Lde=0.0
Lse=0.0
Nsc=1
Rg=5.1
Rd=1.3
Rs=1.3
Rin=1e-3

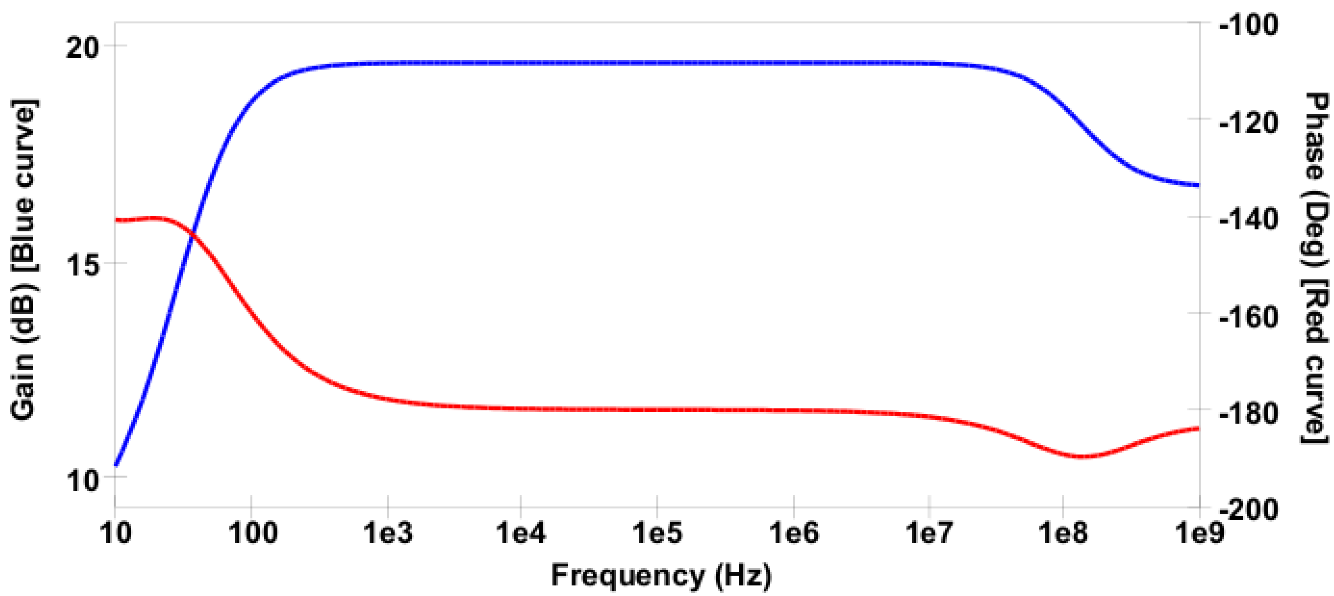


QucsStudio: RF Curtice MESFET compact model
Part 3: Test simulations

AC

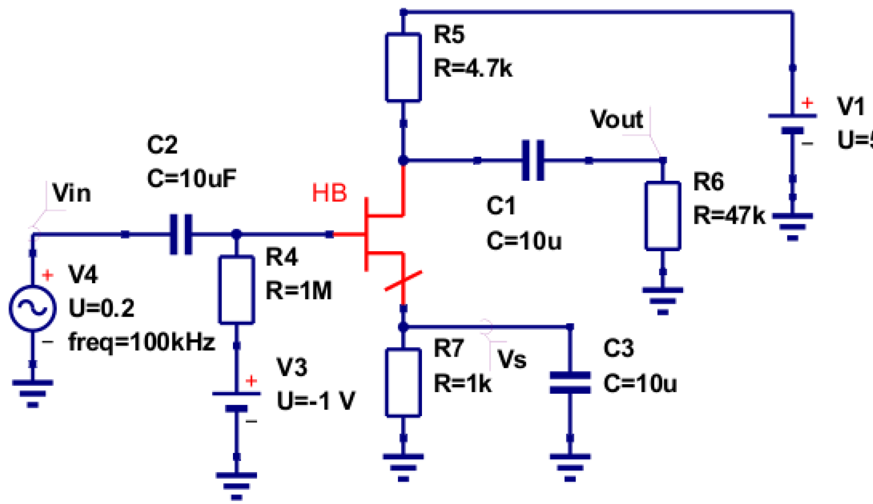


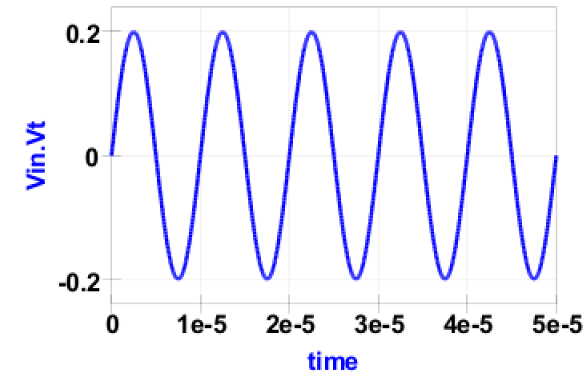
CURTICE1
Area=1
Vto=-1.8
Beta=3e-3
Alpha=2.25
Lambda=0.05
Vtotc=0
Betatc=0
Alphatc=0
Eg=1.11
Tau=1e-9
Is=1e-14
N=1
Xti=3.0
Af=1
Kf=0
Gdsnoi=1
Bv=1e9
R1=1e9
Temp=26.85
Tnom=26.85
Cgse=300f
Cgde=30f
Cdse=300f
Lge=0.0
Lde=0.0
Lse=0.0
Nsc=1
Rg=5.1
Rd=1.3
Rs=1.3
Rin=1e-3

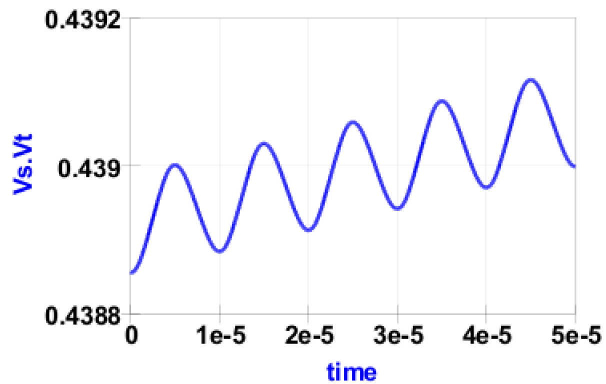


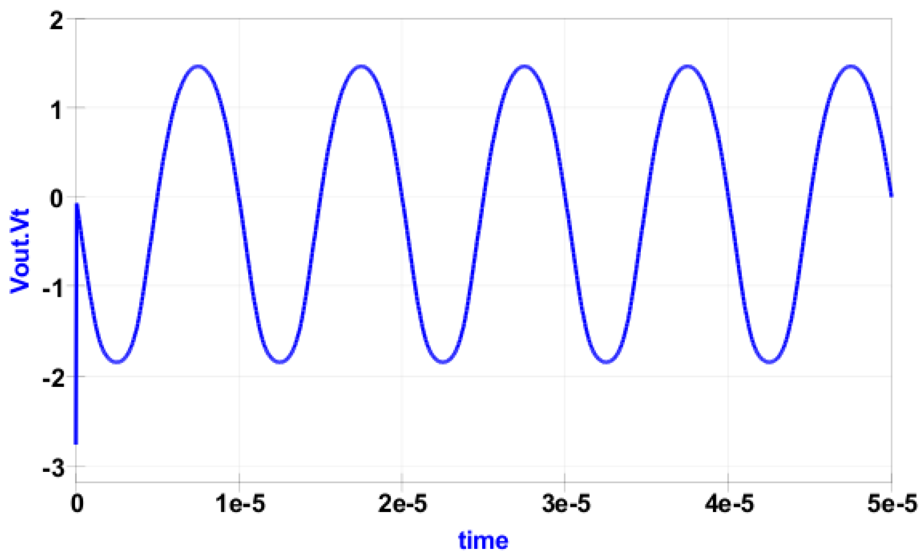
QucsStudio: RF Curtice MESFET compact model
Part 3: Test simulations continued

CURTICE1
Area=1
Vto=-1.8
Beta=3e-3
Alpha=2.25
Lambda=0.05
Vtotc=0
Betatc=0
Alphatc=0
Eg=1.11
Tau=1e-9
Is=1e-14
N=1
Xti=3.0
Af=1
Kf=0
Gdsnoi=1
Bv=1e9
R1=1e9
Temp=26.85
Tnom=26.85
Cgse=300f
Cgde=30f
Cdse=300f
Lge=0.0
Lde=0.0
Lse=0.0
Nsc=1
Rg=5.1
Rd=1.3
Rs=1.3
Rin=1e-3









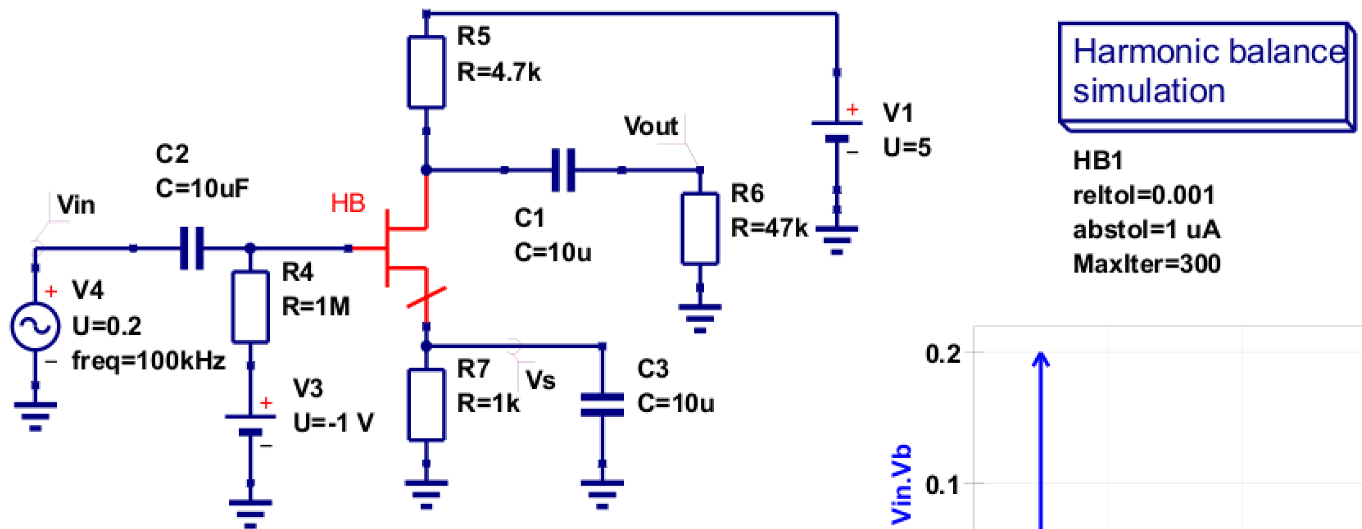
transient simulation

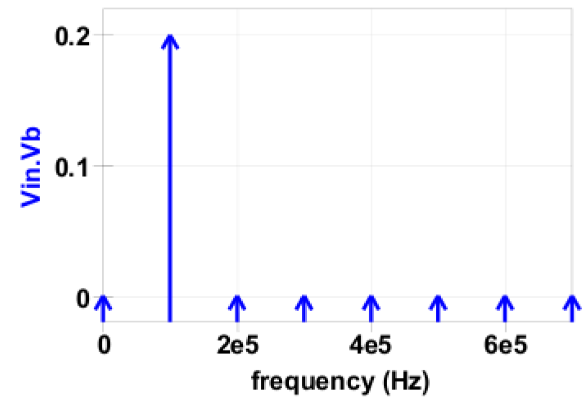
TR1
Stop=50u
Points=1001
method=Gear4
reltol=0.01
abstol=10 µV
initialDC=yes

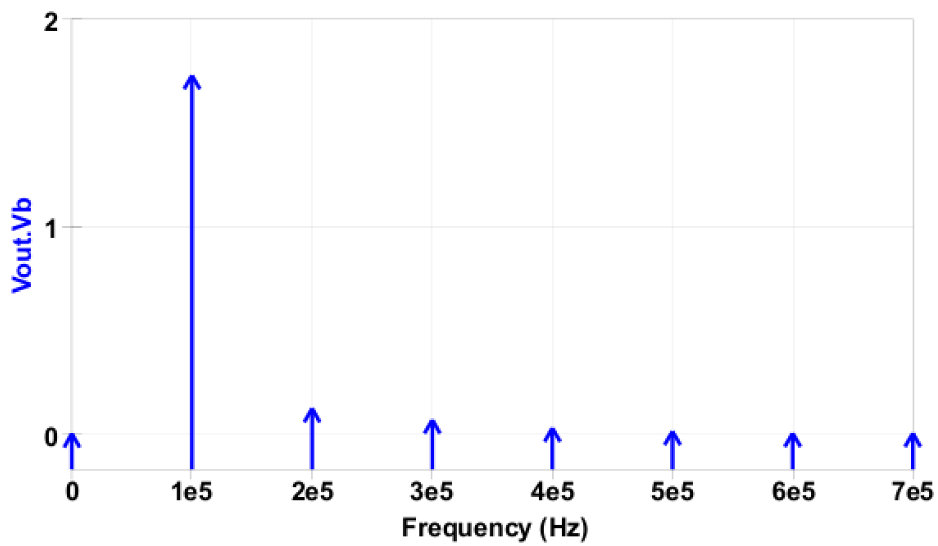
TRAN

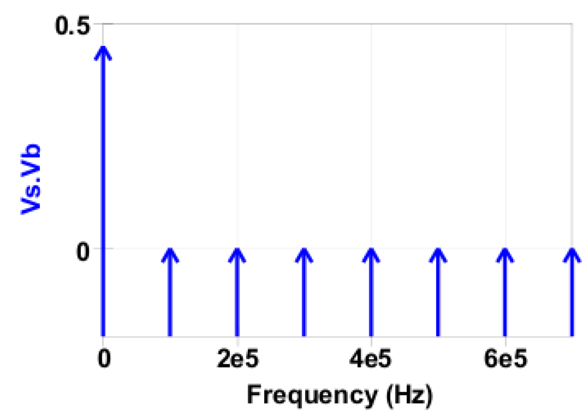
QucsStudio: RF Curtice MESFET compact model
Part 3: Test simulations continued

CURTICE1
Area=1
Vto=-1.8
Beta=3e-3
Alpha=2.25
Lambda=0.05
Vtotc=0
Betatc=0
Alphatc=0
Eg=1.11
Tau=1e-9
Is=1e-14
N=1
Xti=3.0
Af=1
Kf=0
Gdsnoi=1
Bv=1e9
R1=1e9
Temp=26.85
Tnom=26.85
Cgse=300f
Cgde=30f
Cdse=300f
Lge=0.0
Lde=0.0
Lse=0.0
Nsc=1
Rg=5.1
Rd=1.3
Rs=1.3
Rin=1e-3



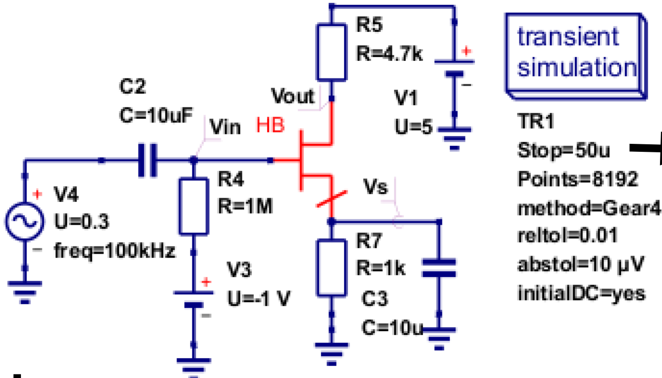


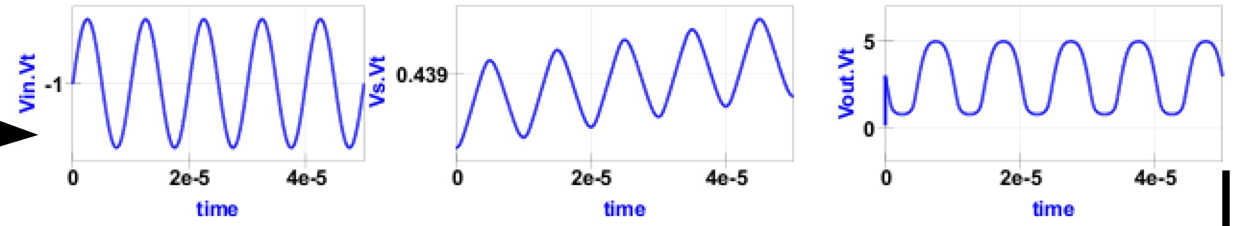




Harmonic Balance

QucsStudio: Octave post-simulation data processing



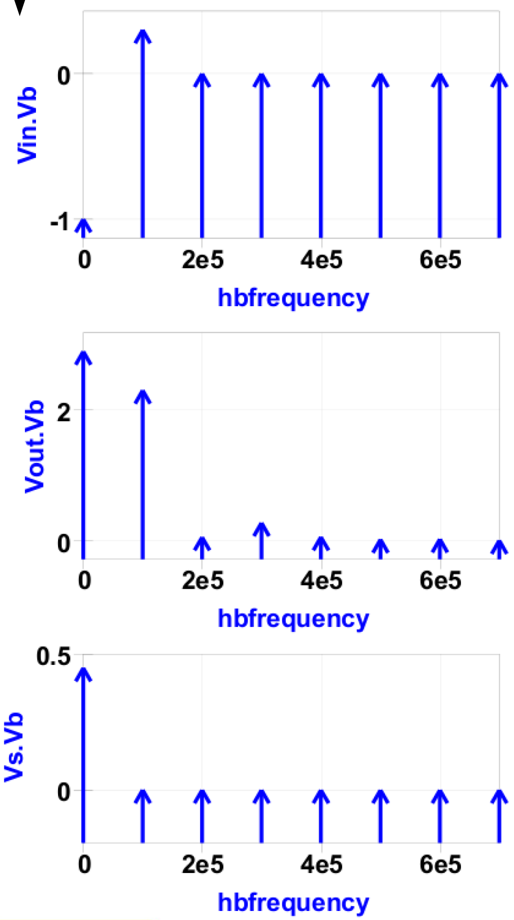



```
% Amp_CurticeTRANOctave.m
% Control file called on completion of transient simulation.
% Calls Octave functions loadQucsVariable and stemfft.
qucsFilename = 'Amp_CurticeTRANOctave.dat';
loadQucsDataset;
whos
[Vout,Dep]=loadQucsVariable("Amp_CurticeTRAN.dat","Vout.Vt");
[Time,Dep1]=loadQucsVariable("Amp_CurticeTran.dat","time");
stemfft(Vout, 8192, 50e-6);
axis([0,1e6]);
grid ON ;
title("Mike first test","fontsize", 16,
    "fontname", "Arial", "fontweight", "bold");
xlabel("Frequency (Hz)", "fontsize", 16,
    "fontname", "Arial", "fontweight", "bold" );
ylabel("Vout amplitude spectrum (V)", "fontsize", 16,
    "fontname", "Arial", "fontweight", "bold");
```

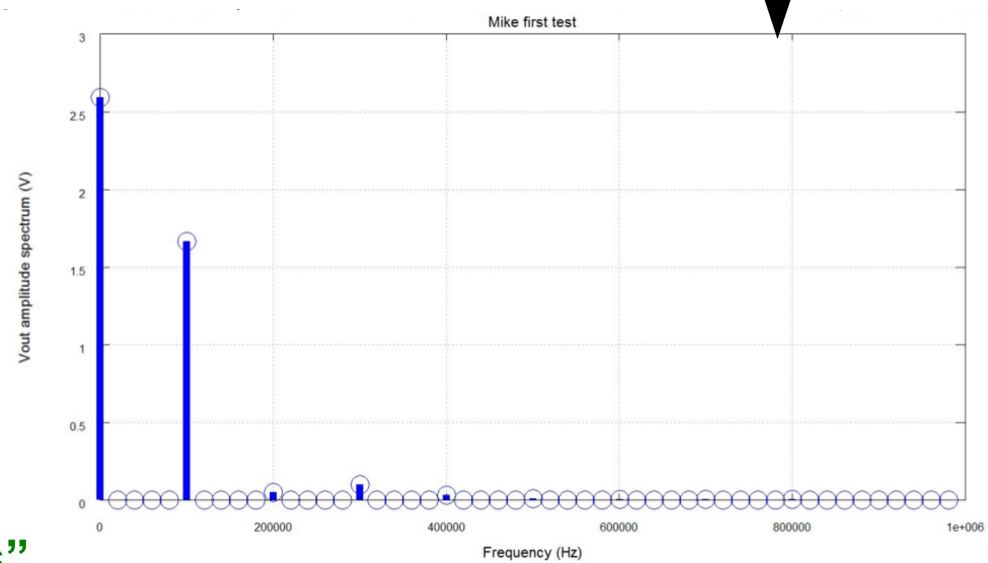
Post-simulation data processing control file

FFT

Harmonic Balance

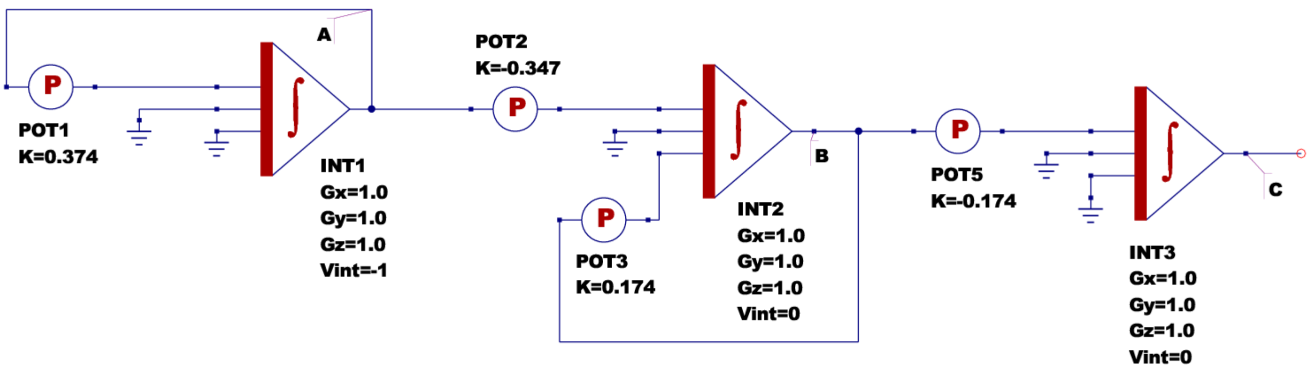


Octave plot of Vout amplitude spectra against frequency



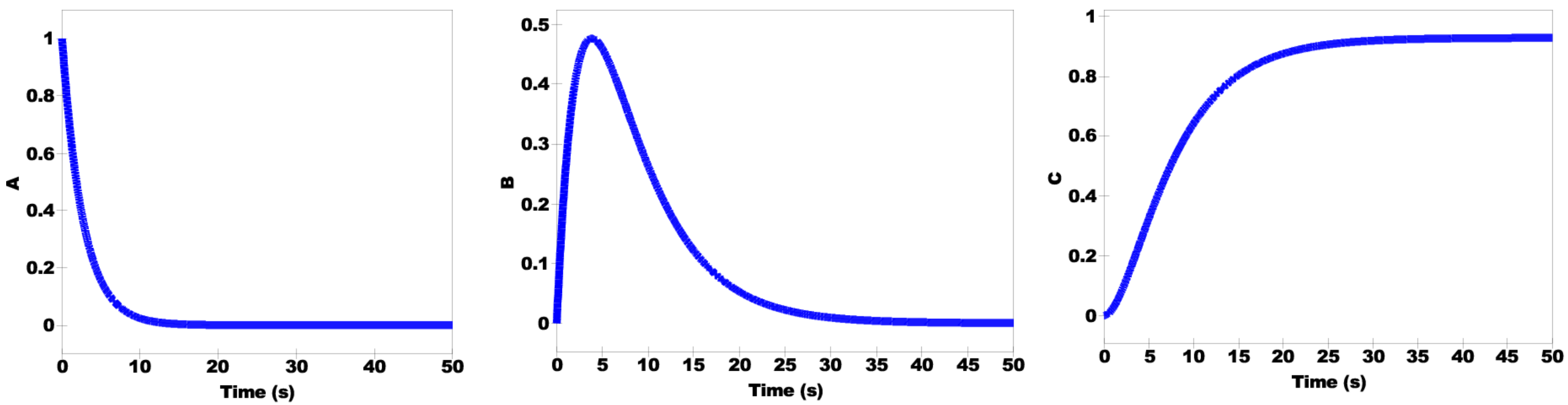
Includes "User defined functions"

Qucs/QucsStudio: Physical System simulation.
Part 1: Continuous systems



transient simulation

TR1
Type=lin
Start=0
Stop=50
Points=2001
IntegrationMethod=Trapezoidal
InitialStep=1 ns
MinStep=1e-16
MaxIter=150
reltol=0.001
abstol=1 pA
vntol=1 uV
Solver=CroutLU



RadioActiveDecay simulation:

$-dA/dt = 0.347 \cdot A$

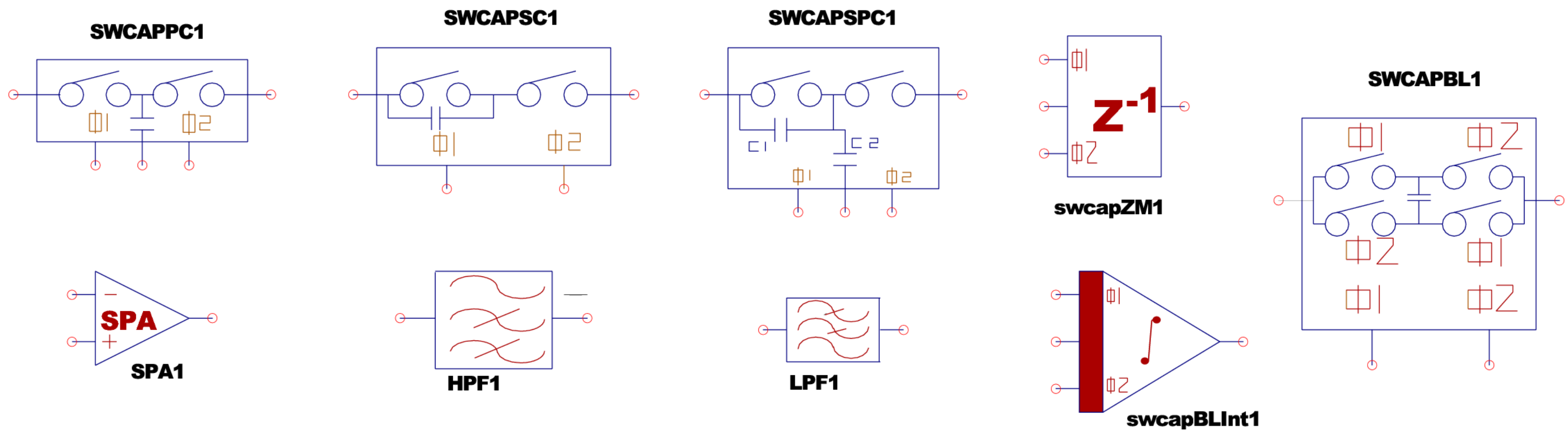
$-dB/dt = -0.347 \cdot A + 0.174 \cdot B$

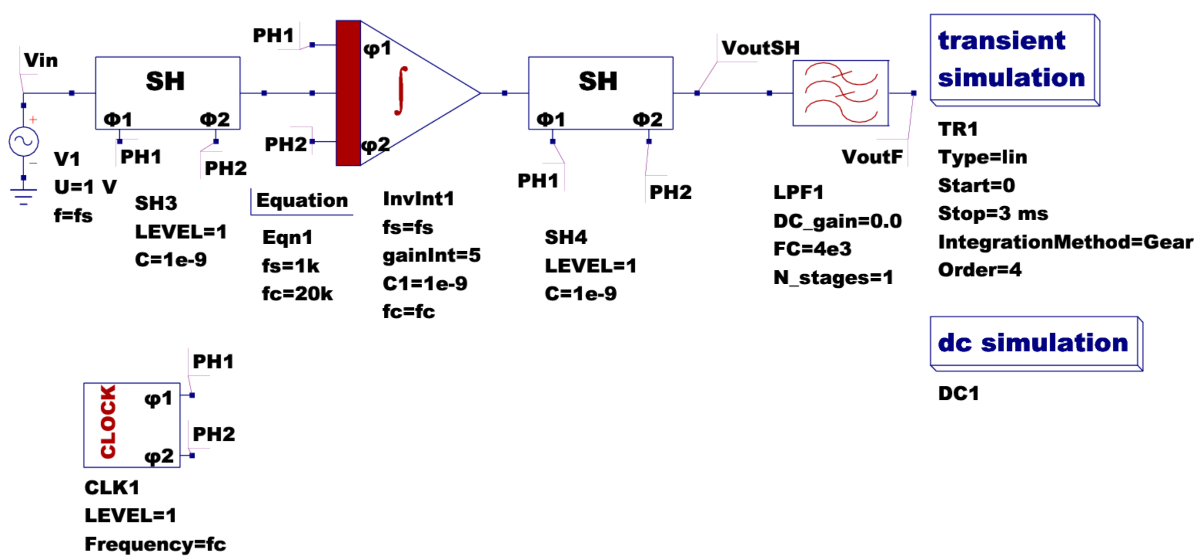
$-dC/dt = -0.174 \cdot B$

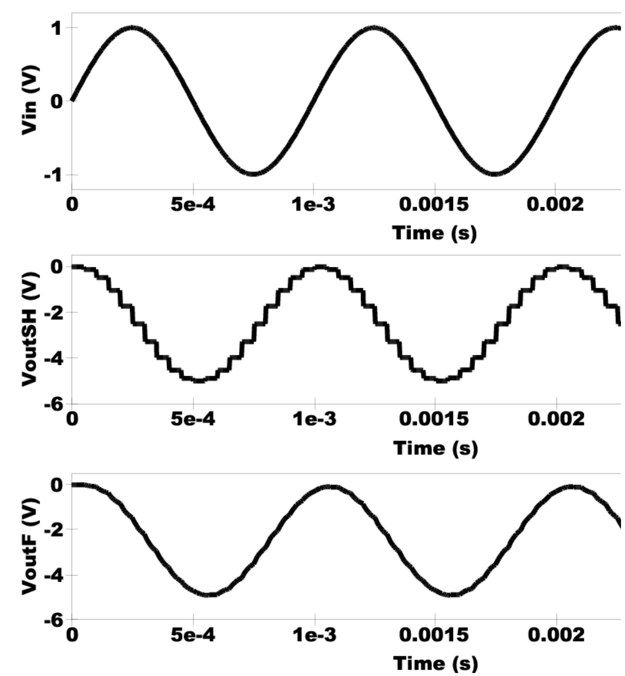
Initial conditions at t = 0 s, A =1, B =0, C =0.

Linear and non-linear continuous system simulation

Qucs/QucsStudio: Physical System simulation.
Part 2: sampled data systems

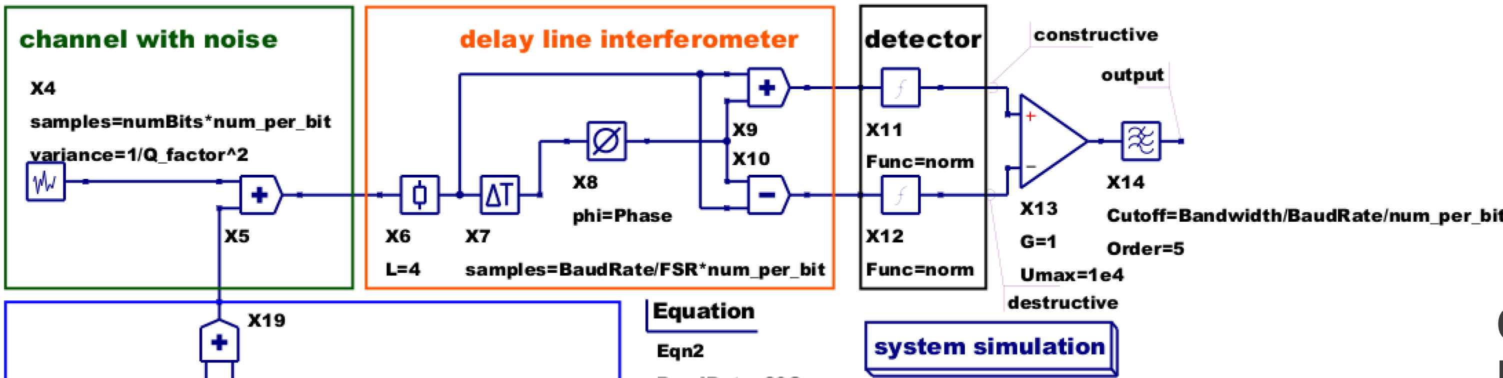


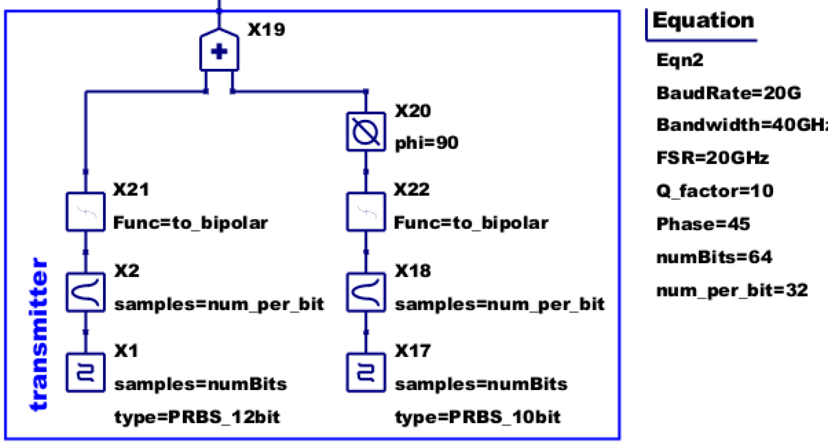




A switched capacitor inverting integrator example

QucsStudio: System simulation. Part 3 communications systems

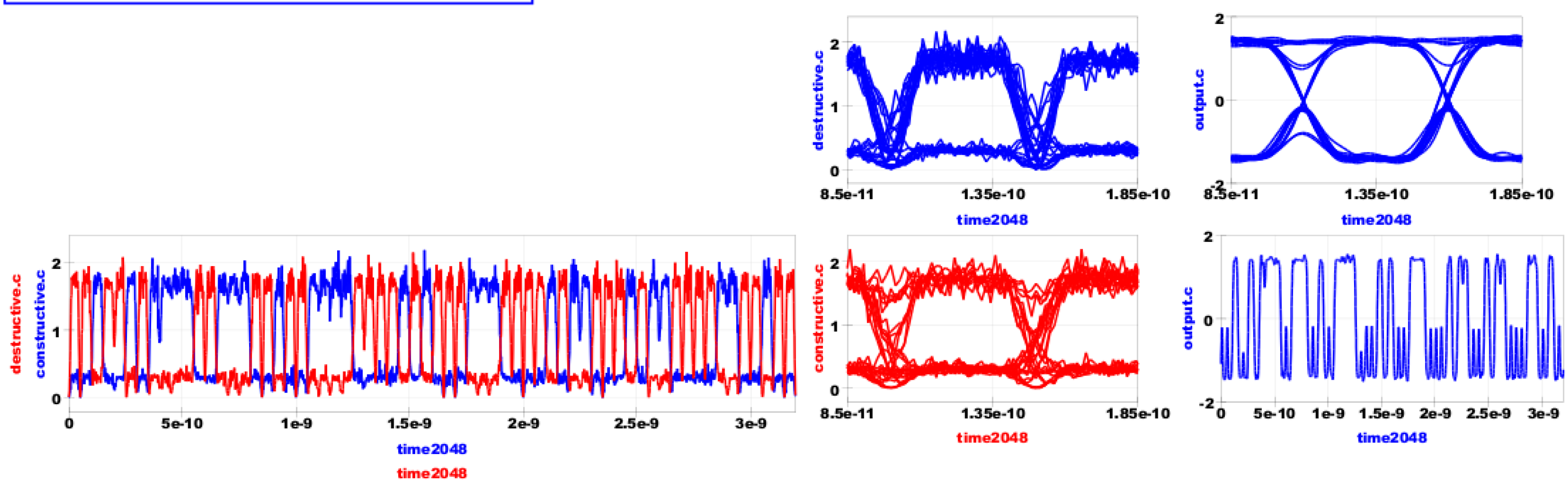




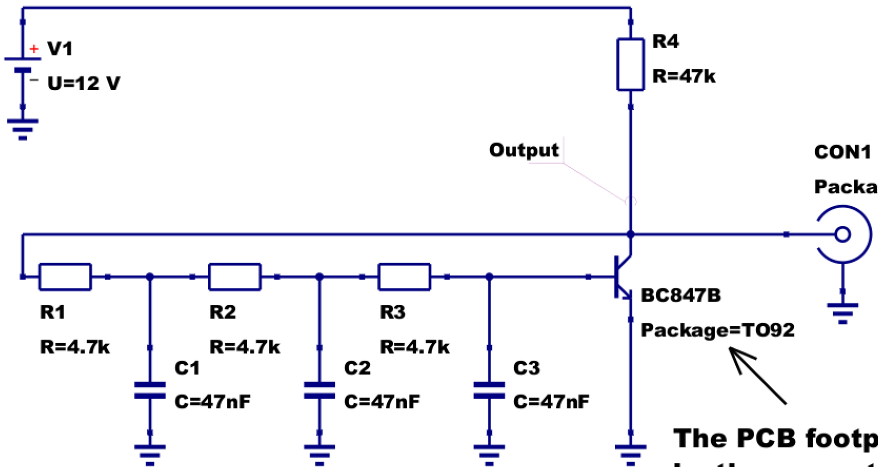
QucsStudio example, Michael Margraf, 2010

NRZ-QPSK transmission as used in optical telecommunication systems.

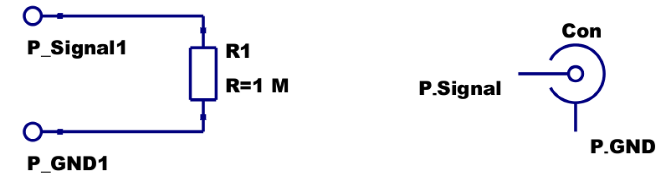
The schematic shows one receiver arm only. A second one with a phase shift of 135° is needed to receive the Q channel.



QucsStudio: System manufacturing printed circuit boards



dummy component to provide PCB footprint of BNC connector



The PCB footprint is determined by the property "Package".

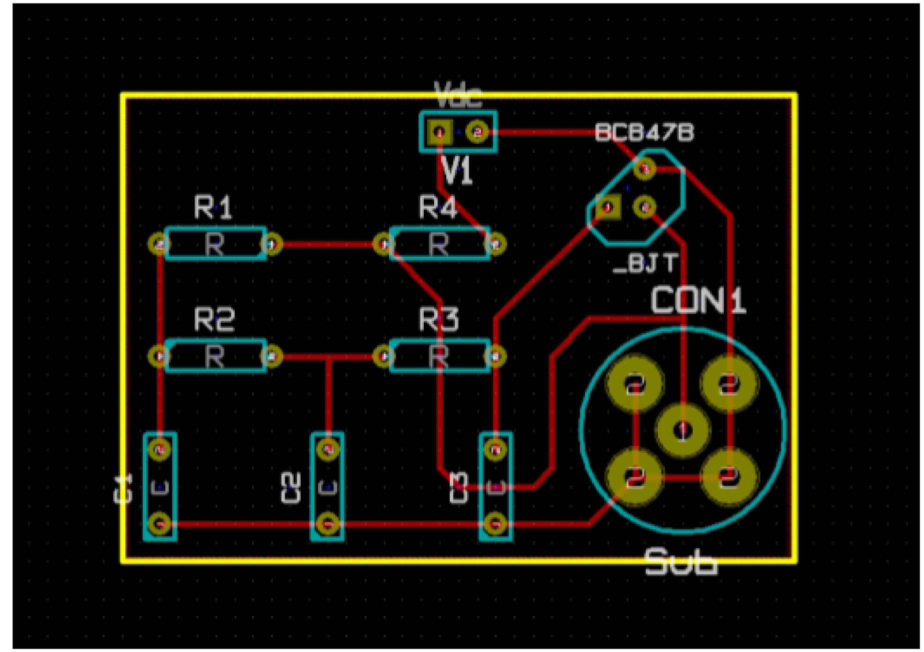
simple 1.8 kHz oscillator

Press F10 (Tools->Create PCB netlist) in order to modify PCB layout.

The Gerber files can be viewed with Tools->Gerber Viewer

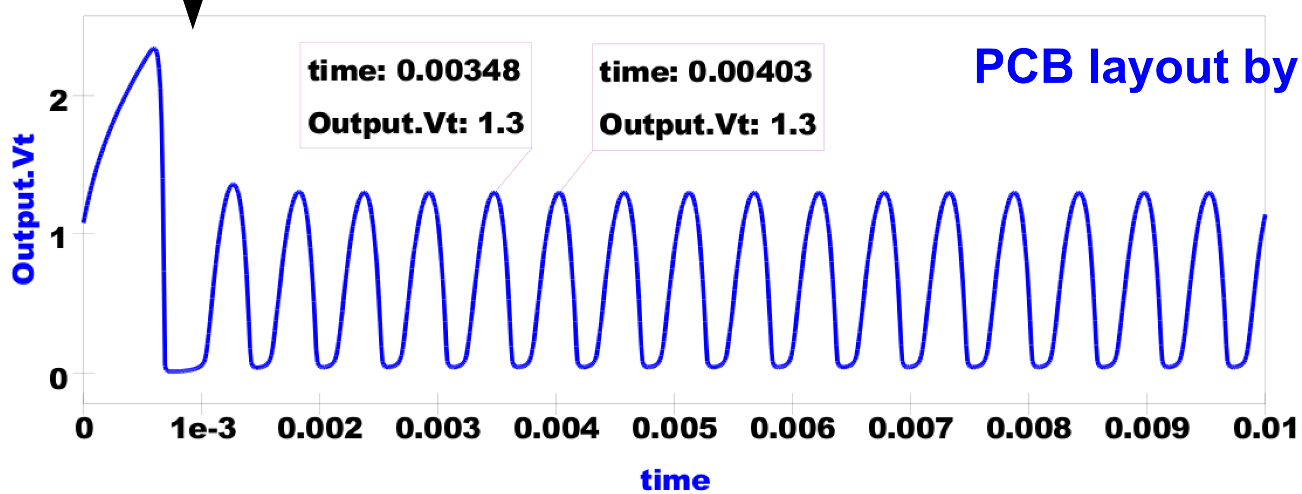
transient simulation

TR1
Type=lin
Start=0
Stop=10 ms
Points=1001
initialDC=no



QucsStudio example, Michael Margraf, 2010

Simulation



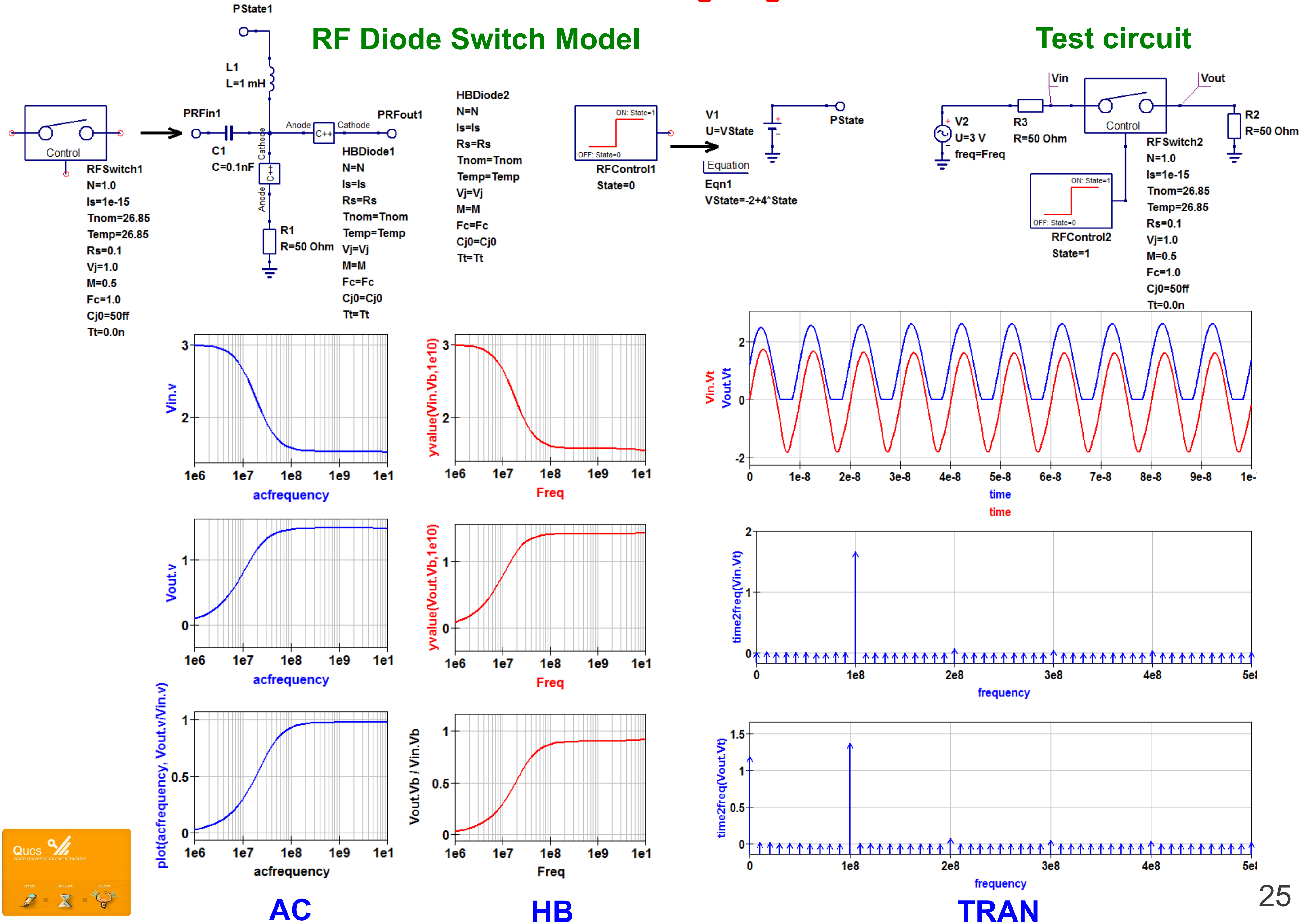
PCB layout by KiCAD

Qucs/QucsStudio: Additional features

Qucs	QucsStudio	Feature	Notes
X	X	Digital simulation: VHDL	Qucs → FreeHDL QucsStudio → GHDL
		: Verilog	Both using ICARUS
X	X	SPICE netlist defined components	
X	X	Small signal AC and S-parameter noise	
	X	Harmonic Balance and noise and noise parameter calculations	
X	X	Tabular two and multiport S-parameter components	
X	X	Tabular voltage and current sources	
X	X	Component libraries	Qucs → User library only QucsStudio → User and binary libraries
X	X	RF components: transmission line, microstrip line and coplanar line	
X	X	Import and export data of different formats	
	X	GPIB device control	
X	X	Create and extract project packages	
X	X	Circuit performance optimization using ASCO	
	X	Templates: Octave function Octave_function.m, S-parameters.sch, skeleton.cpp, skeleton.va, skeleton.vhdl and symbols.sch	
X	X	Design tools:Text editor, Filter synthesis,	
		Line calculations, Matching circuits	Both Qucs and QucsStudio
		Gerber Viewer	QucsStudio only

Qucs and QucsStudio are freely available under the open source General Public Licence
Download from: Qucs version 0.0.16 → http://qucs.sourceforge.net
QucsStudio from http://mydarc.de/DD6UM/QucsStudio/qucsstudio.html
[Currently QucsStudio supports Windows® only: QucsStudio-1.3.1.zip or QucsStudio-1.3.0_light.zip {without Octave and model compiler}]

QucsStudio: Latest additions: Large signal AC simulation



Qucs/QucsStudio: Future changes

The following changes to the QucsStudio software are being actively planned:

- A full range of non-linear semiconductor device models, including EKV, BSIM, HiCUM etc.
- Model improvements for different electrical and physical domains and systems.
- Circuit oscillation simulation by Harmonic Balance analysis.
- Periodic steady state analysis.
- Mixed-mode simulation.
- EM field simulation.
- Upgrade of the QucsStudio GUI to Qt4.
- A range of Octave functions for simulation data analysis and visualisation.
- Many smaller improvements and extensions.

Individuals or groups interested in contributing to the development of QucsStudio should contact Michael Margraf (michael.margraf@alumini.tu-berlin.de) or Mike Brinson (mbrin72043@yahoo.co.uk)

Summary

1. Qucs and QucsStudio are freely available circuit simulators distributed as open source software under the GNU General Public Licence (GPL).

2. This presentation has attempted to outline the history and the fundamental features of the packages, the available components, libraries, built in design aids, analysis types and post-simulation data analysis and visualisation capabilities.

3. The presentation also introduced a number of basic approaches to circuit simulation with Qucs and QucsStudio.

4. A series of slides also showed how the compact semiconductor modelling and circuit macromodeling features implemented in the current QucsStudio release can be used to develop equation-defined component models of established and emerging technology devices.

5. A “turn-key” approach to compact device modelling using the Verilog-A hardware description language was introduced and the proposed modelling system demonstrated via the development of a MESFET RF device simulation model.

6. The final section of the presentation briefly introduced the use of QucsStudio for system simulation and PCB development.

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