A hybrid Verilog-A and equation-defined subcircuit approach to MOS switched current analog cell modeling and simulation in the transient and large signal ac domains

M.E. Brinson
Faculty of Computing
London Metropolitan University
London, UK
mbrin72043@yahoo.co.uk

S.Jahn
Qucs project manager
Munich
Germany
stefan@lkcc.org

H. Nabijou
Faculty of Computing
London Metropolitan University
London, UK
h.nabijou@londonmet.ac.uk

***Abstract*—Conventional modeling and simulation of two phase switched current MOS integrated circuits is normally undertaken at semiconductor device level. This allows primary and secondary circuit effects to be studied and characterised. However, with the growing complexity of this type of circuit, transient domain simulation times can become prohibitively long, restricting the size of circuit that can be easily investigated. Measurable reductions in transient simulation run times can be achieved by modeling part, or all, of a switched current design as a macromodel. This paper introduces a hybrid approach to MOS switched current circuit modeling that combines the primary features of compact device modeling with functional circuit macromodeling. To illustrate the proposed hybrid modeling procedure the properties, and simulation model, of a MOS switched current analog memory cell are described. The material presented also demonstrates how recent trends in Quite universal circuit simulator (Qucs) technology promote embedded Verilog-A models and equation-defined subcircuits as integral elements in mixed-mode circuit and system design.**

***Index Terms*—Switched current analog integrated circuits, compact semiconductor device models, circuit macromodels, Qucs universal circuit simulator (Qucs), equation-defined device modeling, Verilog-A.**

I. Introduction

Mixed-mode circuit simulation is an established technique for investigating the performance of analog and digital integrated circuits. Conventional modeling and transient simulation of emerging semiconductor technologies, for example switched current MOS circuits, is usually undertaken at semiconductor device level, making transient analysis of complex systems particularly lengthy. Moreover, circuit simulators rarely include special purpose simulation engines that are designed to handle emerging technologies at a functional level [1]. This paper presents a hybrid equation-defined subcircuit modeling technique based on a parameterized subcircuit structure plus embedded Verilog-A code for non-linear devices which has been optimized to improve run-time simulation speed. The hybrid modeling procedure has been evaluated using the "Quite universal circuit simulator" (Qucs) [2] and applied in the design of functional switched current memory cell macromodels.

II. First and Second order switched current memory cells

The fundamental circuit underpinning MOS switched current technology [4] is the current memory cell given in Fig.1. As its name implies this circuit represents an input current as an equivalent charge stored on the gate-source capacitance of an MOS transistor. Specific circuitry is included to allow output current to be extracted from the cell at a later time. Two basic forms of memory cell have become popular since the switched current technique was first introduced, namely the first generation current mirror circuit [5] and secondly the second generation single transistor circuit with mirrored current output [6].

III. Computationally efficient Verilog-A code for voltage controlled and switched current MOS transistor models

Efficient numerical simulation models for voltage controlled switches and MOS transistors are an essential prerequisite for transient time domain simulation of switched current circuits. Most circuit simulators provide built-in models for these highly non-linear devices. Unfortunately, predefined models are often not suited for functional mixed-mode simulation, mainly because they include code to cover all possible regions of physical operation rather than being minimized for the high speed computation under specific operating conditions. This section of the paper introduces descriptions and characteristics of a voltage controlled switch model and a MOS transistor model whose properties have been optimised for switched current circuit simulation. Fig. 2 shows a test circuit for determining the series resistance of a voltage controlled switch. Any discontinuities in the resistive characteristics can significantly increase transient simulation run times due to the excessively small time steps required by numerical integration

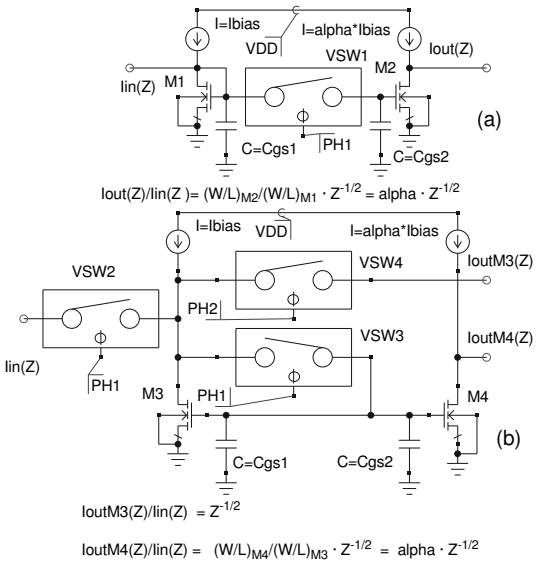

Fig. 1. MOS switched current memory cells: (a) first generation current mirror circuit, (b) second generation circuit with direct and mirrored output. The VSWn components are voltage controlled switches operated by a non-overlapping two phase clock

routines to achieve acceptable voltage and current errors in a region of abrupt resistive change. To overcome this problem switch resistance, and its first and second derivatives, should be a continuous function of input control voltage.

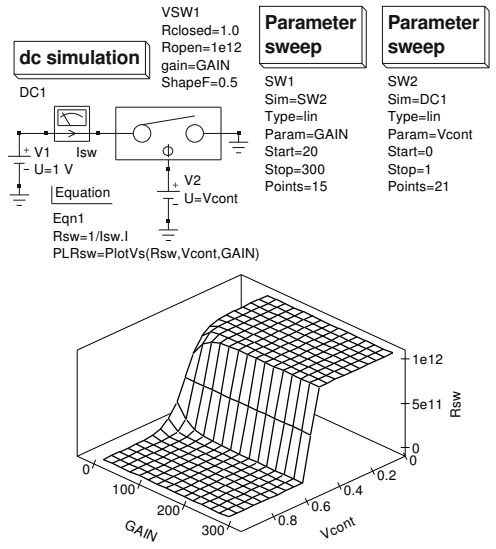

Fig. 2. Voltage controlled switch test circuit and switch resistance plot

The voltage controlled switch given in Fig.2 has a resistive function given by equation 1.

$$R_{sw} = R_{closed} + R_{open} \cdot F1 \tag{1}$$

Which simplifies to equation 2.

$$R_{sw} = R_{closed} + R_{open}/F2 \tag{2}$$

where

$$F1 = 1 - tanh(gain \cdot [VPH - ShapeF \cdot LEVEL]) \tag{3}$$

$$F2 = 1 + limexp(2 \cdot gain \cdot [VPH - ShapeF \cdot LEVEL]) \tag{4}$$

R_{closed} is the closed switch resistance in Ω, R_{open} is the open switch resistance in Ω, *gain* is a scaling parameter, *LEVEL* is the high value of the switch control voltage in V, *VPH* is the switch control voltage in V, *ShapeF* is a switching point scaling factor and *limexp* is the Verilog-A limiting exponential function. Parameter *gain* adjusts the slope of the resistive switching characteristics. Parameter *ShapeF* sets the voltage level between zero and *LEVEL* volts at which switching occurs. The expression for R_{sw} given in equation 2 is similar to one proposed by Giacoletto [7]. Equation 2 is however, in a form which can be implemented simply as a current contribution in a Verilog-A analog module, see Fig. 3.

```
`include "disciplines.vams"
`include "constants.vams"
//
module vswitch(swIN, swOUT, PH);
inout swIN, swOUT, PH;
electrical swIN, swOUT, PH;
`define attr(txt) (*txt*)
parameter real LEVEL   = 1.0   from [1.0  : inf]
   `attr(info = "Switch high level control voltage" unit="V");
parameter real Rclosed  = 1.0   from [1e-9 : inf]
   `attr(info = "Switch closed series resistance" unit = "Ohm");
parameter real Ropen   = 1e12   from [1e-9 : inf]
   `attr(info = "Switch open series resistance" unit = "Ohm");
parameter real gain    = 100.0  from [1e-9 : inf]
   `attr(info = "Switch gain factor");
parameter real ShapeF  = 0.5   from [1e-9 : inf]
   `attr(info = "Switching point scaling factor");
real Vmid;
analog begin
 @(initial_model)
  begin
   Vmid=ShapeF*LEVEL;
  end
 I(swIN, swOUT) <+ V(swIN, swOUT)/(Rclosed +
                    Ropen/(1+limexp(gain*(V(PH)-Vmid))));
end
endmodule
```

Fig. 3. Minimised run time Verilog-A code for a Voltage controlled switch

Fig.4 lists the Verilog-A code for the non-linear dc characteristics of an EPFL-EKV V2.6 long channel nMOS transistor [8]. To minimise the number of numerical computations undertaken each time this code is called during simulation all numerical constants and algebraic constant expressions are grouped within a Verilog-A `@(initial_model)` block [9][10]. This block is called only once prior to the start of a simulation sequence.

IV. A MACROMODEL FOR AN IDEAL SWITCHED CURRENT MEMORY CELL

By combining the Verilog-A voltage controlled switch model introduced previously with linear controlled sources and

```
`include "disciplines.vams"
`include "constants.vams"
//
module EKV26nMOSLCDC (Drain, Gate, Source, Bulk);
inout Drain, Gate, Source, Bulk;   electrical Drain, Gate, Source, Bulk;
`define attr(txt) (*txt*)
parameter real L = 10e-6 from [0.0 : inf]
      `attr(info="length parameter" unit = "m" );
parameter real W = 10e-6 from [0.0 : inf]
      `attr(info="Width parameter" unit = "m");
parameter real VTO = 0.5 from [1e-6 : 2.0]
      `attr(info="long channel threshold voltage" unit="V" );
parameter real GAMMA = 0.7 from [0.0 : 2.0]
      `attr(info="body effect parameter" unit="V**(1/2)");
parameter real PHI = 0.5 from [0.3 : 2.0]
`attr(info="bulk Fermi potential" unit="V");
parameter real KP = 50e-6 from [10e-6 : inf]
      `attr(info="transconductance parameter" unit = "A/V**2");
parameter real THETA = 50e-3 from [0 : inf]
      `attr(info="mobility reduction coefficient" unit = "1/V");
real P1, P2, P3, P4, P5, P6, P7, P8, P9, VGprime, VP, n, Beta, If, Ir;
analog begin
 @(initial_model)
   begin
      P1 = -VTO+PHI+GAMMA*sqrt(PHI); P2 = GAMMA/2;
      P3 = P2*P2; P4 = GAMMA*P2-PHI; P5 = PHI+4*$vt+1e-6;
      P6 = KP*W/L; P7 = 1/(2*$vt); P8 = 2*$vt*$vt; P9 = -PHI;
   end
 VGprime = V(Gate,Bulk)+P1;
if (VGprime > 0.0)
      VP = P4+VGprime-GAMMA*sqrt(VGprime+P3);
else
      VP = P9;
n = 1+P2/sqrt(VP+P5); Beta = P6/(1+THETA*VP);
If = pow(ln(1+limexp((VP-V(Source,Bulk))*P7)), 2);
Ir = pow(ln(1+limexp((VP-V(Drain,Bulk))*P7)), 2);
I(Drain,Source) <+ P8*n*Beta*(If-Ir);
end
endmodule
```

Fig. 4. Optimised dc Verilog-A code for an EPFL-EKV v2.6 long channel nMOS transistor

other linear components a numerically efficient ideal subcircuit model of a switched current memory cell can be synthesized. Fig. 5 shows a subcircuit macromodel of this type. This modeling strategy merges Verilog-A code, which is optimized for specific operating conditions, with the code of other predefined, and tested components, yielding macromodels with improved run time characteristics. In Fig.5 controlled source SCR3 converts input current to voltage. During phase one of the two phase clock cycle capacitor CWL is charged. During phase two the voltage across CWL is converted to current by controlled source SRC2 and output via terminals Ioutfrom and Ioutto. Capacitor CWL represents the value of Cgs of an nMOS transistor with W and L dimensions operating in saturation. Fig. 6 illustrates a typical set of input and output waveforms for the ideal switched current memory cell macromodel. Component SH in Fig. 6 is an ideal sample and hold block. Fig.7 lists the Verilog-A code for this simplified hybrid model. Again in order to minimise the amount of numerical computation all numerical constants and algebraic constant terms are entered within a Verilog-A `@(initial-model)` block.

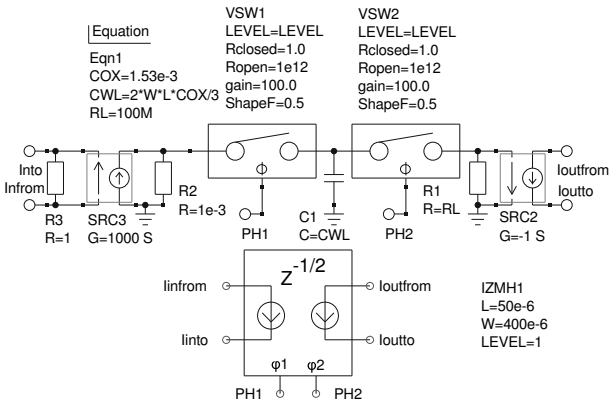

Fig. 5. An ideal macromodel of a switched current memory cell

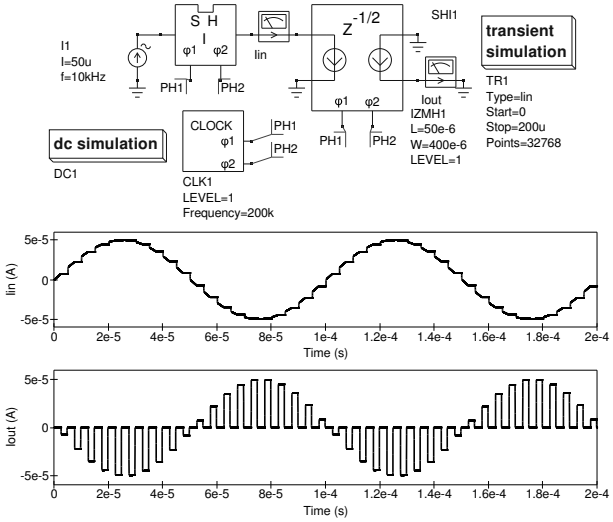

Fig. 6. Ideal switched current memory cell macromodel test circuit and example waveforms: input signal frequency = 10kHz at 50μA peak, two phase clock sampling frequency = 200kHz

V. A HYBRID MACROMODEL FOR A FIRST GENERATION SWITCHED CURRENT MEMORY CELL

The circuit schematic given in Fig. 8 represents a subcircuit macromodel of a first generation switched current cell. Control sources SRC6 and SRC4 and voltage VDCH deal with input and output current interfacing. Controlled source SRC7 allows scaling of the supply voltage VDC to give VDCH. The remaining sections of the macromodel correspond to the schematic given in Fig. 1a. MOS transistors M1 and M2 are modeled by EPFL-EKV v2.6 long channel dc models with their gate to source capacitance represented by capacitors C3 and C2. To minimise numerical computation each time the characteristics of macromodel are computed during each simulation cycle the MOS transistor capacitances are to a first approximation considered to be constant, with value

$$C3 = 2 \cdot W \cdot L \cdot COX/3, \quad C2 = alpha \cdot C3 \qquad (5)$$

Where *COX* is the gate oxide capacitance per unit area and *alpha* is defined in Fig. 1b. Diode D1 in Fig. 8 provides a

```
`include "discipline.vams"
`include "constants.vams"
module idealZMH (Iinfrom, Iinto, Ioutfrom, Ioutto, PH1, PH2);
inout Iinfrom, Iinto, Ioutfrom, Ioutto, PH1, PH2;
electrical Iinfrom, Iinto, Ioutfrom, Ioutto, PH1, PH2;
electrical n1, n2, n3;
`define attr(txt) (*txt*)
parameter real L=10e-6 from [1e-20:inf]
      `attr(info='channel length' unit="m");
parameter real W=20e-6 from [1e-20:inf]
      `attr(info='channel width'  unit="m");
parameter real LEVEL=1.0 from [1.0:inf]
      `attr(info='control voltage high' unit="V");
real Rclosed, Ropen, gain, ShapeF, COX, CWL, RL, Vmid;
analog begin
 @(initial_model)
  begin
     Rclosed=1.0; Ropen=1e12; gain=100.0; ShapeF=0.5; COX=1.5e-3;
     CWL=2*W*L*COX/3; RL=1e8; LEVEL=1.0; Vmid=ShapeF*LEVEL;
  end;
 I(Iinfrom, Iinto) <+  V(Iinfrom, Iinto);
 I(n1) <+  -V(Iinfrom, Iinto)*1000;
 I(n1) <+  V(n1)/1e-3;
 I(n1,n2) <+ V(n1,n2)/(Rclosed+Ropen/(1+limexp(gain*(V(PH1)-Vmid))));
 I(n2) <+ ddt(CWL*V(n2));
 I(n2,n3) <+ V(n2,n3)/(Rclosed+Ropen/(1+limexp(gain*(V(PH2)-Vmid))));
 I(n3) <+ V(n3)/RL;
 I(Ioutfrom, Ioutto) <+ -V(n3);
end
endmodule
```

Fig. 7. Verilog-A code for an ideal switched current memory cell macromodel

dc path for transistor M1 drain to source current. It models, again to a first approximation, the finite output resistance of a pMOS transistor current source. Fig. 9 illustrates a typical set of input and output waveforms for a first generation switched current memory cell macromodel. Fig. 10 lists Verilog-A code for a hybrid macromodel of a first generation switched current memory cell. Optimisation of the model run-time speed is achieved by reducing the number of numerical computations implicit in the Verilog-A code to a mimimum.

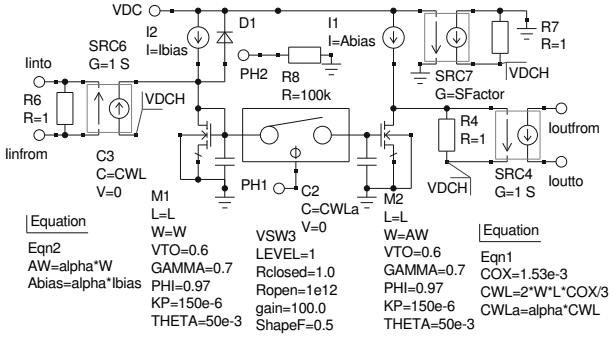

Fig. 8. A hybrid macromodel of a first generation switched current memory cell

VI. A HYBRID MACROMODEL FOR THE SWITCHED CURRENT SECOND GENERATION MEMORY CELL

The schematic in Fig. 11 shows a second generation switched current memory cell. Although it appears more complex than the previously presented diagrams it is in many ways similar to the first generation cell model. Transistor M1

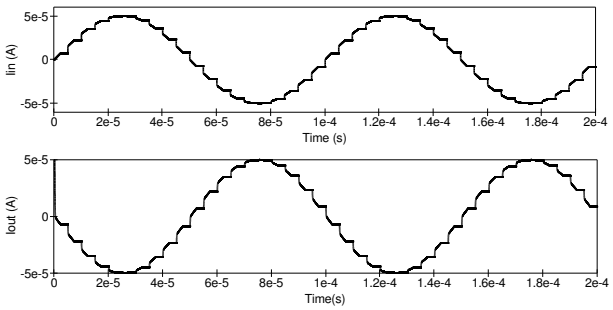

Fig. 9. First generation switched current memory cell simulation waveforms: input signal frequency = 10kHz at 50μA peak, Ibias = 200μA dc, two phase sampling clock frequency = 200kHz

```
`include "discipline.vams"
`include "constants.vams"
module G1TranZMH (Iinfrom, Iinto, Ioutfrom, Ioutto, PH1, PH2, VDC);
inout Iinfrom, Iinto, Ioutfrom, Ioutto, PH1, PH2, VDC;
electrical Iinfrom, Iinto, Ioutfrom, Ioutto, PH1, PH2, VDC;
electrical n1, n2, n3,n4;
`define attr(txt) (*txt*)
parameter real L=10e-6 from [1e-20:inf]
      `attr(info='channel length' unit="m");
parameter real W=20e-6 from [1e-20:inf]
      `attr(info='channel width'  unit="m");
parameter real LEVEL=1.0 from [1.0:inf]
      `attr(info='control voltage high' unit="V");
parameter real alpha=1.0 from [0.01:inf]
      `attr(info='output transistor W/L scale factor');
parameter real SFactor=0.5 from [0:inf]
      `attr(info='Supply voltage scale factor');
parameter real Ibias=50e-6 from [1e-12:inf]
      `attr(info='DC bias current' unit="I");
real Rclosed, Ropen, gain, ShapeF, COX, CWL, CWLa, RL, Vmid, Abias;
real VTO, GAMMA, PHI, KP, THETA, P1, P2, P3, P4, P5, P6, P6a, P7, P8, P9;
real VGprime, VP, n, Beta, If, Ir,  VGprimea, VPa, na, Betaa, Ifa, Ira;
analog begin
 @(initial_model)
  begin
   Rclosed=1.0; Ropen=1e12; gain=100.0; ShapeF=0.5; COX=1.5e-3;
   CWL=2*W*L*COX/3; CWLa=CWL*alpha; Vmid=ShapeF*LEVEL;
   VTO=0.6; GAMMA=0.7; PHI=0.97; KP=150e-6; THETA=50e-3;
   P1 = -VTO+PHI+GAMMA*sqrt(PHI); P2 = GAMMA/2; P3 = P2*P2;
   P4 = GAMMA*P2-PHI; P5 = PHI+4*$vt+1e-6; P6 = KP*W/L; P6a=P6*alpha;
   P7 = 1/(2*$vt); P8 = 2*$vt*$vt; P9 = -PHI; Abias=alpha*Ibias;
  end;
I(Iinfrom, Iinto) <+  V(Iinfrom, Iinto); I(n4,n1) <+ V(Iinfrom, Iinto); I(VDC,n1) <+ Ibias;
I(n1,VDC) <+ 1e-12*(limexp(V(n1,VDC)/$vt)-1.0)+V(n1,VDC)*1e-12; VGprime = V(n1)+P1;
if (VGprime > 0.0)
      VP = P4+VGprime-GAMMA*sqrt(VGprime+P3);   else   VP = P9;
n = 1+P2/sqrt(VP+P5); Beta = P6/(1+THETA*VP); If = pow(ln(1+limexp(VP*P7)), 2);
Ir = pow(ln(1+limexp((VP-V(n1))*P7)), 2); I(n1) <+ P8*n*Beta*(If-Ir);
I(n1) <+ ddt(CWL*V(n1));
I(n1,n2) <+ V(n1,n2)/(Rclosed+Ropen/(1+limexp(gain*(V(PH1)-Vmid))));
I(n2) <+ ddt(CWLa*V(n2));
I(VDC,n3) <+ Abias; VGprimea = V(n2)+P1;
if (VGprimea > 0.0)
      VPa = P4+VGprimea-GAMMA*sqrt(VGprimea+P3);  else  VPa = P9;
na = 1+P2/sqrt(VPa+P5);  Betaa = P6a/(1+THETA*VPa); Ifa = pow(ln(1+limexp(VPa*P7)), 2);
Ira = pow(ln(1+limexp((VP-V(n3))*P7)), 2); I(n3) <+ P8*na*Betaa*(Ifa-Ira);
I(n4,n3) <+ V(n4,n3); I(Ioutfrom, Ioutto) <+ -V(n4,n3);
I(n4) <+ V(n4); I(n4) <+ -SFactor*V(VDC);
end
endmodule
```

Fig. 10. Verilog-A code for a first generation switched current memory cell macromodel

provides the cell functionality with transistor M2 mirroring its current output. Another addition to the second generation model is transistor M1 gate-diffusion overlap capacitance Cgd. Fig. 12 illustrates the input-output behaviour of the second generation cell. Similar to the first generation switched memory model the output currents are a close inverted copy of the input signal delayed by half a clock period. However,

in the case of the second generation memory cell, direct output Iout1 has glitches on the trailing edge of the phase one pulse. These are a direct result of the non-overlapping two phase clock waveform. During periods when the clock phases do not overlap (both outputs at zero volts) transistor M1 drain node impedance changes state from a low to high impedance generating a glitch on the current waveform. This a direct consequence of the additional charge that is needed to charge parasitic capacitance Cgd. Note that glitches are not generated with the first generation model because the drain and gate of transistor M1 are connected together. The hybrid Verilog-A macromodel of the switched current second generation memory cell is very similar to the code given in Fig. 10 after making the obvious node changes and adding additional components. One feature of both the first and second generation switched current macromodels is their ability to model distortion caused by large amplitude input signals. When the peak amplitude of the input signal current exceeds the cell dc bias, current clipping occurs, yielding significant signal distortion, see Fig. 13. Clipping does not occur in the ideal current switching model.

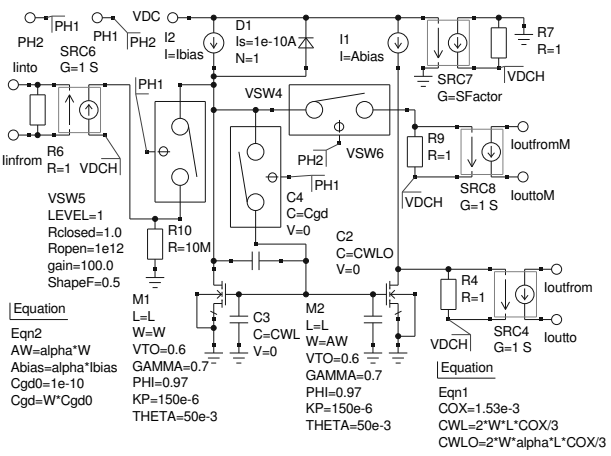

Fig. 11. A hybrid macromodel for a second generation switched current memory cell

VII. A SIMPLE LOW PASS SWITCHED CURRENT FILTER EXAMPLE

This section presents an example simulation of the large signal ac performance of a low pass switched current filter based on the first generation switched current Verilog-A macromodel. The S domain transfer function for a single pole low pass filter is given equation 6. A Z domain discrete approximation of equation 6 can be derived by applying Tustin's [11] method using equation 7 to give equation 8.

$$T(S) = \frac{1}{1 + \frac{S}{\omega_p}} \tag{6}$$

$$S = \frac{2}{T} \cdot \frac{1 - Z^{-1}}{1 + Z^{-1}} \tag{7}$$

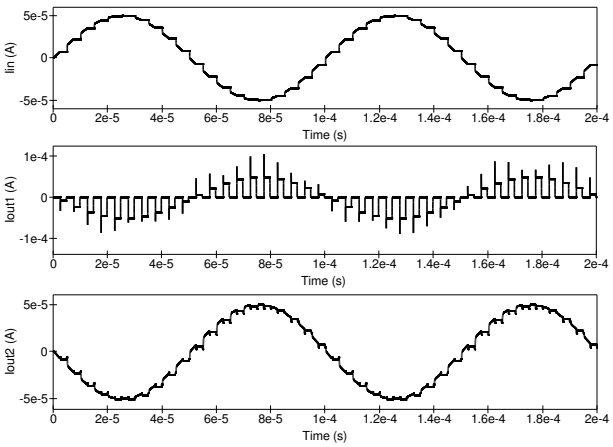

Fig. 12. Second generation switched current memory cell simulation waveforms: input signal frequency = 10kHz at 50μA peak, Ibias = 200μA dc, two phase sampling clock frequency = 200kHz; output signals Iout1 and Iout2 equivalent to IoutM3(Z) and IoutM4(Z) Fig.1b

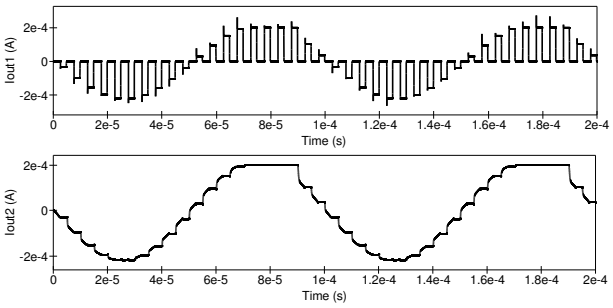

Fig. 13. Second generation switched current memory cell waveforms showing distortion: input signal frequency = 10kHz at 210μA peak, Ibias = 200μA dc, two phase sampling clock frequency = 200kHz; output signals Iout1 and Iout2 equivalent to IoutM3(Z) and IoutM4(Z) Fig.1b

$$Y(Z) = [MA \cdot X(Z) - MB \cdot Y(Z) \cdot] Z^{-1} + MA \cdot X(Z) \tag{8}$$

Where

$$T(Z) = \frac{Y(Z)}{X(Z)}, MA = \frac{\omega_p \cdot T}{\omega_p \cdot T + 2}, MB = \frac{\omega_p \cdot T - 2}{\omega_p \dot{T} + 2} \tag{9}$$

Figure 14 shows a test circuit and example output waveforms for a single pole switched current low pass filter with a cut off frequency of 20kHz. The input test waveforms consists of the addition of a set of single frequency ac signals of peak amplitude Amult and zero phase. The input and output amplitude spectra were determined using fast Fourier techniques where the ratio of the input and output spectra amplitudes, at each frequency, forms a gain envelope which represents the large signal ac transfer function of the filter.

VIII. CONCLUSION

Transient simulation of two phase switched current integrated circuits is often undertaken at semiconductor device level, commonly resulting in long simulation times when analysing the performance of moderate size circuits. This

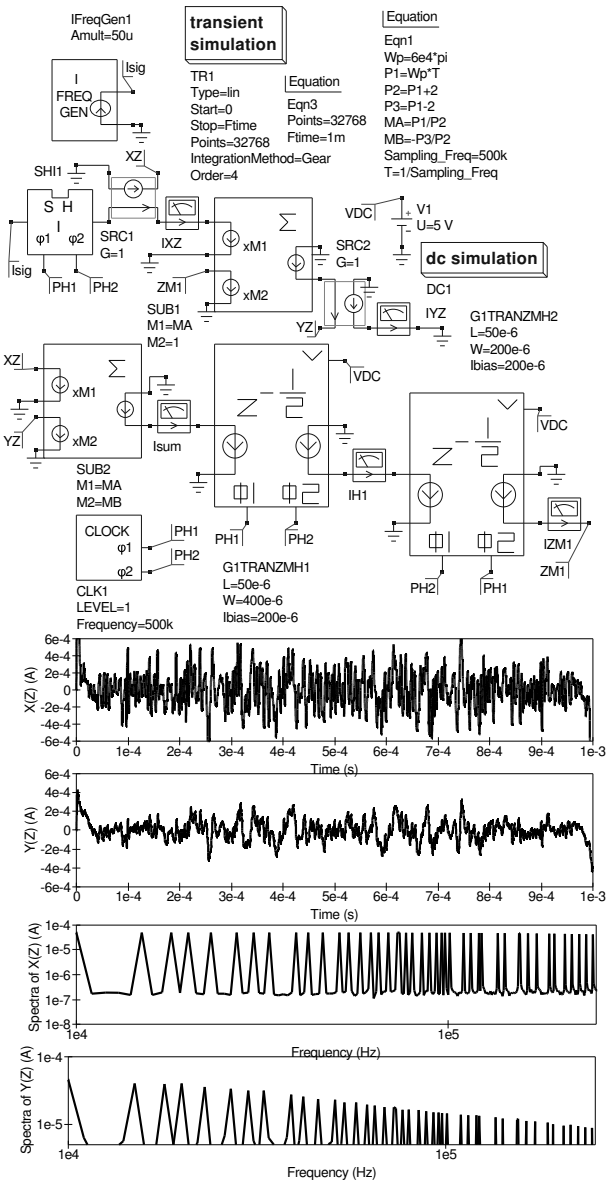

Fig. 14. Large signal ac simulation of single pole first generation switched current low pass filter with fp=20kHz: test circuit, X(Z) and Y(Z) waveforms and corresponding frequency domain amplitude spectra

paper introduces a hybrid subcircuit and Verilog-A modeling technique for the construction of functional behavioural macromodels which have improved run times over device level simulation. Hybrid switched current integrated circuit macromodels are particularly suited for the simulation of mixed-mode electronic systems which include both established analog and digital components plus emerging technology devices and circuits modeled at both functional and semiconductor hierarchical levels.

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