Adaptive EPFL-EKV Long and Short Channel MOS Device Models for Qucs, SPICE and Modelica Circuit Simulation

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***Abstract*—Equation-defined non-linear functional elements are important building blocks in the development of compact semiconductor device models. Current trends in compact device modeling suggest widespread acceptance among the modeling community of Verilog-A, for semiconductor device specification, model exchange and circuit simulation. This paper outlines techniques for the development of adaptive EPFL-EKV long and short channel MOS models which stress user selectable model features and diagnostic capabilities. Adaptive EPFL-EKV nMOS models based on Verilog-A and Modelica are introduced and their performance compared with simulation data obtained using the "Quite universal circuit simulator" (Qucs), SPICE and the Modelica simulation environment.**

***Index Terms*—Adaptive MOS models, Qucs, SPICE, Modelica, equation-defined device modeling, Verilog-A, EPFL-EKV MOSFET model, parameter and equation monitoring.**

I. Introduction

Compact semiconductor model development has in recent years advanced significantly through the use of equation-defined non-linear functional elements [1] and the adoption of Verilog-A as the hardware description language of preference for model construction and model interchange between different circuit simulators [2]. The standardization of Verilog-A [3] has also accelerated its acceptance as the modeling tool of choice among the compact device modeling community. In many respects Verilog-A is a hardware description language which has arrived on the modeling scene at the right time, bringing to the art of compact modeling an array of positive features which greatly aid in the construction of complex models. Such models appear to be characterized by an ever increasing number of parameters, particularly when compared to the number associated with the SPICE legacy devices [4]. These parameters, plus built-in model equations, allow accurate modeling of I-V, dynamic and noise characteristics for devices with sub-micron feature sizes. However, with current semiconductor device sub-micron feature sizes, model functionality is often achieved at the expense of model complexity [15]. Previous and current generations of circuit simulator normally allow users to select semiconductor device model types through the use of a LEVEL parameter. Similarly, in some instances, model complexity can be controlled by setting one or more second order physical parameters to zero [5]. Unfortunately when the model code is not published, both these approaches do not give a clear indication as to the calculation overhead incurred by a given model, or a restricted subset model, making it difficult to minimize circuit simulation run times for a specific model hierarchical level. This paper outlines techniques for the development of adaptive long and short channel nMOS models which stress user selectable model features and promote diagnostic features through the addition of signal probes to model interfaces. Adaptive EPFL-EKV nMOS models based on Verilog-A and Modelica are introduced and their performance compared using simulation data obtained with Qucs [6] and the Modelica simulation environment [7], [8].

II. The Basic Long Channel EPFL-EKV MOS model

Qucs equation-defined device (EDD) models and Verilog-A hardware description language models for long channel EPFL-EKV 2.6 nMOS transistors [9] can be found in recently published literature [10]. A set of typical long channel nMOS I-V characteristics obtained by Qucs circuit simulation are presented in Fig. 1. As expected, both the Qucs EDD and the Verilog-A model simulation output data give identical results. However, one important difference between the performance of the two models is observed from the I-V simulation tests, namely the model simulation speed. The EDD model, being an interpretive model, tends to be slower than the Verilog-A model after its code has been translated to the C/C++ language, compiled and linked to the other sections of a circuit simulators C/C++ code. Qucs is not the only simulator which allows compact semiconductor device models to be constructed with equation-defined components. Shown in Fig. 2 is the SPICE code for an EPFL-EKV long channel nMOS transistor based on the SPICE extensions implemented in LTspice IV ® [11]. Unfortunately, at this time, there appears to be little standardization of the format for SPICE 3 extensions among the freely available General Public License (GPL) [12],[13] and commercial versions of SPICE, implying

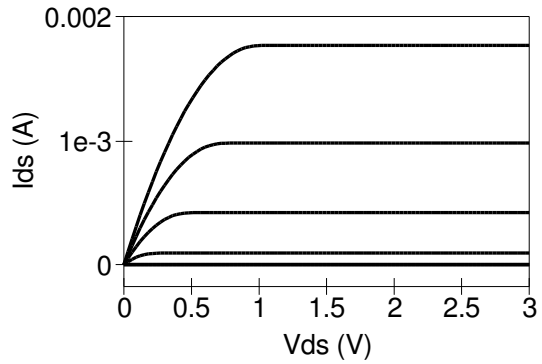

Fig. 1. I-V output characteristic for a long channel EPFL-EKV 2.6 nMOS model with: L=0.5e-6m, W=10e-6m, VTO=0.6V, GAMMA=0.7$\sqrt{V}$, PHI=0.97V, KP=150e-6A/V^2, THETA = 50e-3V^{-1} and TEMP = 26.86 Celsius.

that the code shown in Fig. 2 would probably need some modification when run on a different SPICE simulator. It is also possible to develop a version of the EPFL-EKV 2.6 long channel nMOS transistor model using the Modelica simulation language. Fig. 3 presents the Modelica code for such a model. Like Verilog-A most implementations of the Modelica modeling environment are compiled, rather than interpretive, which results in fast circuit simulation speeds. Note how similar in many respects the Modelica language is to Verilog-A hardware description language.

III. Adding intrinsic charge storage effects to the long channel EPFL-EKV 2.6 MOS model

To be able to simulate the dynamic performance of MOS transistors a model for the device intrinsic stored charge or capacitance must be added to a DC MOS model. In the case of the EPFL-EKV 2.6 MOS model the stored charge is represented by equations (69) to (78) given in publication [9]. Fig. 4 presents the Verilog-A code for a long channel nMOS transistor with additional charge equation code. Device control parameter CHARGESWITCH is set to one if the charge calculation code is to be included in a simulation, otherwise it is set to zero and the charge code is ignored. The use of this type of switch allows a model to be adapted to fit the needs of a given simulation, for example at DC or very low frequencies the stored charge calculations can be removed from the model without loss of accuracy. The approach adopted in this paper ensures that switched out sections of Verilog-A code are not evaluated during simulation and hence improves the overall simulation speed of a model. It is also worth noting that the proposed code selection technique is ideal in the sense that it only adds a simulation speed penalty equivalent to the run time associated with a C/C++ "if-then-else" statement and a simple variable assignment statement. The test circuit and simulation results shown in Fig.5 indicate firstly how capacitance values can be extracted from a Qucs model, either the equation-defined device or Verilog-A forms, using S parameter simulation techniques, and secondly how Qucs visualization procedures can be used to plot device intrinsic capacitance

```
*
.subckt EKV26nMOSLC 1 2 3 4  L=0.5e-6 W=10e-6 VTO=0.6 GAMMA=0.7
+                    PHI=0.97 KP=150e-6 THETA=50e-3
+                    TEMP=26.85
* Node order -->   gate drain source bulk
* Initialisation code
.param P1={-VTO+PHI+GAMMA*sqrt(PHI)},  P2={GAMMA/2}, P3={P2*P2}
.param PK=1.3806503e-23, PQ=1.602176472e-19, T2={TEMP+273.15}
.param VTT2={PK*T2/PQ}, P5={PHI+4*VTT2+1e-12}, P6={KP*W/L}
.param P7={1/(2*VTT2)}, P8={2*VTT2*VTT2}
*End initialisation code
*Current contributions representing model equations
Bvgprime 0 5 I=V(1,4)+P1
Rvgprime 5 0 1
Bvp 0 6 I=if(V(5) >= 0.0, V(5)-PHI-GAMMA*(sqrt(V(5)+P3)-P2), -PHI)
Rvp 6 0 1
Bn  0 7  I=1+P2/sqrt(V(6)+P5)
Rn  7 0 1
Bbeta  0 8 I=P6/(1+THETA*V(6))
Rbeta  8 0 1
Biff1 0 9 I=ln(1+exp((V(6)-V(3,4))*P7))
Riff1 9 0 1
Bir   0 10 I=ln(1+exp((V(6)-V(2,4))*P7))
Rir 10 0 1
Bids 2 3 I=P8*V(7)*V(8)*(V(9)*V(9)-V(10)*V(10))
* End current contributions
.ends
* nMOS long channel I-V characteristics test circuit
Vgs 1 0 dc 1
Vds 99 0 dc 1
Vm  99 2 dc 0
X1 1 2 0 0 EKV26nMOSLC  L=0.5e-6 W=10e-6 VTO=0.6 GAMMA=0.7
+                    PHI=0.97 KP=150e-6 THETA=50e-3
+                    TEMP=26.85
.op
.dc  Vds 5 0 -0.05 Vgs 0 3 0.5
.end
```

Fig. 2. LTspice IV equation-defined non-linear subcircuit and I-V test circuit netlist for a long channel EPFL-EKV 2.6 nMOS model with identical parameters to those listed in Fig. 1.

```
model EKV26nMOSLC
  Modelica.Electrical.Analog.Interfaces.Pin D;
  Modelica.Electrical.Analog.Interfaces.Pin G;
  Modelica.Electrical.Analog.Interfaces.Pin S;
  Modelica.Electrical.Analog.Interfaces.Pin B;
// Initialisation code
  parameter Real L=5e-07; parameter Real W=1e-05;
  parameter Real VTO=0.6; parameter Real PHI=0.97;
  parameter Real GAMMA=0.71; parameter Real KP=150e-6;
  parameter Real THETA=0.05; parameter Real TEMP=26.85;
  constant Real PQ=1.602176462e-19; constant Real PK=1.3806503e-23;
  parameter Real P1=-VTO+PHI+GAMMA*sqrt(PHI);
  parameter Real P2=GAMMA/2; parameter Real P3=P2*P2;
  parameter Real T2=TEMP+273.15; parameter Real VTT2=(PK*T2)/PQ ;
  parameter Real P5=PHI+4*VTT2; parameter Real P6=(KP*W)/L;
  parameter Real P7=1/(2*VTT2); parameter Real P8=2*VTT2*VTT2;

  Real vgprime,vp, n, beta, iff1, iff, ir1, ir, Id;
// Model equations and current contributions
equation
  vgprime = G.v + P1;
  vp=if gprime>0.0 then vgprime-PHI-GAMMA*(sqrt(vgprime+P3)-P2) else -PHI;
  n = 1 + P2 / sqrt(vp + P5);
  iff1 = log(1 + exp((vp - S.v) * P7));  iff = iff1 * iff1;
  ir1 = log(1 + exp((vp-D.v) * P7));     ir = ir1 * ir1;
  beta= P6/(1+THETA*vp); Id = P8 * n * beta * (iff - ir);
  G.i = 0; D.i = Id; S.i = -Id; B.i = 0;
end EKV26nMOSLC;
```

Fig. 3. Modelica equation-defined non-linear model for a long channel EPFL-EKV 2.6 nMOS model with identical parameters to those listed in Fig. 1.

$Cg = Cgs + Cgd + Cgb$ as a function of voltage Vgs. The same basic procedure can be adopted when developing a Mod-

elica version of the EPFL-EKV 2.6 model. Presented in Fig.6 is the Modelica code equivalent to the Verilog-A version of the compact semiconductor device shown in Fig.4. In contrast to the Verilog-A model the Modelica model includes code for the device capacitance rather than device charge: equations 79 to 85 cited in publication [9]. Although the code for the two different hardware description languages looks similar a number of points are worth commenting on. Firstly, in the Verilog-A code the $=$ and $<+$ operators represent different forms of assignment statement. However, in the Modelica code the $=$ operator is equivalent to the "equals" found in the notation for a mathematical equation. Secondly, again in the case of Modelica, the number of equations and the number of variables must balance for the code to simulate without error. This implies that there must only be one equation for each variable in a model. In the Modelica code given in Fig. 6 Verilog-A control variable CHARGESWITCH is replaced by CAPSWITCH and the Verilog-A time differential operator ddt by the equivalent Modelica operator der. Presented in Fig.7 is an example plot of a set of nMOS transistor intrinsic capacitances Cgs, Cgd, Cdb and Csb versus Vds obtained by Modelica simulation.

```
`include "disciplines.vams"
`include "constants.vams"
module EKV26nMOSSC1(drain,gate,source,bulk);
inout drain,gate,source,bulk; electrical drain,gate,source,bulk;
parameter real L=0.5e-6 from [1e-20:inf];
parameter real W=10e-6 from [1e-20:inf];
parameter real VTO=0.6 from [1e-20:2.0];
parameter real GAMMA=0.71 from [0:2.0];
parameter real PHI=0.97 from [0.3:2.0];
parameter real KP=150e-6 from [1e-20:inf];
parameter real THETA=50e-3 from [0:inf];
parameter real DW=-0.02e-6 from [-5e-6:0];
parameter real DL=-0.05e-6 from [-5e-6:0];
parameter real COX=3.45e-3 from [1e-20:inf];
parameter real TEMP=26.85 from [-100: 100];
parameter integer CHARGESWITCH=0 from [0:1];
parameter real Xpart=0.4 from [0:1];
real P1,P2,P3,P5,P6,P7,P8,P9, P10; real vgprime,vp,n,beta,iff1,ir1,iff,ir, weff, leff;
real nq,P21,xf,xr,qi,qb,qg,coxide,Qi,Qb,Qg,Spart;
branch (gate,bulk) Bgb; branch (source,bulk) Bsb; branch (drain,bulk) Bdb;
branch (drain,source) Bds; branch (gate, drain) Bgd; branch (gate,source) Bgs;
analog begin
@(initial_model) begin
 P1=-VTO+PHI+GAMMA*sqrt(PHI); P2=GAMMA/2; P3=P2*P2;  P10=4*$vt;
 P5=PHI+4*$vt+1e-12; P6=KP*W/L; P7=1/(2*$vt); P8=2*$vt*$vt;
 weff=W+DW; leff=L+DL; P21=PHI+1e-6;
 Spart=1-Xpart; coxide=COX*weff*leff;
end
vgprime=V(Bgb)+P1;
if (vgprime>0.0) vp=vgprime-PHI-GAMMA*(sqrt(vgprime+P3)-P2); else vp=-PHI;
n=1+P2/sqrt(vp+P5);
iff1=ln(1+limexp((vp-V(Bsb))*P7)); iff=iff1*iff1;
ir1=ln(1+limexp((vp-V(Bdb))*P7));  ir=ir1*ir1;
// Charge equations
if ((CHARGESWITCH==1)  begin
 nq=1+GAMMA/(2*sqrt(vp+P21)); xf=sqrt(0.25+iff); xr=sqrt(0.25+ir);
 qi=-nq*(1.333333*(xf*xf+xf*xr+xr*xr)/(xf+xr+1e-20)-1);
 if (vgprime > 0) qb=(-GAMMA*sqrt(vp+P21))/$vt-((nq-1)/nq)*qi;
 else qb=-vgprime/$vt;
 qg=-qi-qb;
end
if (CHARGESWITCH==1) begin
 Qi=coxide*$vt*qi; Qb=coxide*$vt*qb; Qg=coxide*$vt*qg;
 I(Bgd) <+ Spart*ddt(Qg); I(Bgs) <+ Xpart*ddt(Qg);
I(Bdb) <+ Spart*ddt(Qb);  I(Bsb) <+ Xpart*ddt(Qb);
end;
vpdash=0.5*(vp+sqrt(vp*vp+P8)); beta=P6/(1+THETA*vpdash);
I(Bds) <+ P8*n*beta*(iff-ir);
end
endmodule
```

Fig. 4. Verilog-A non-linear long channel EPFL-EKV 2.6 nMOS DC model plus device intrinsic capacitance modeled as intrinsic, gate and bulk charge: default device parameters are listed in the initial section of the model

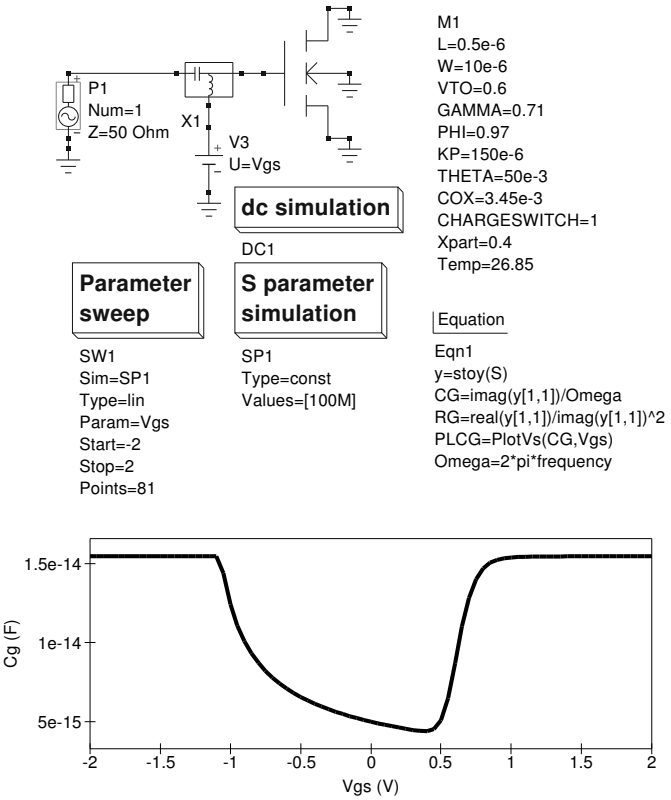

Fig. 5. Gate capacitance extraction test circuit with device drain, source and bulk terminals connected to ground and waveform Cg = Cgs+Cgd+Cgb (F) plotted against Vgs (V) at a test frequency of 100MHz and -2V $<=$ Vgs $<=$ 2V.

IV. Extending the Verilog-A and Modelica versions of the EPFL-EKV 2.6 MOS model to include short channel effects

Verilog-A and Modelica short channel versions of the long channel EPFL-EKV 2.6 MOS model previously described are introduced in this section. The proposed short channel model includes the four switches listed in Table I. The purpose of these switches is to select the short channel effects that are to be included in the model during simulation: when the switches are set to one the corresponding short channel effect is active. The reverse is true when the switches are set to zero. Using the Verilog-A and Modelica code presented in Fig.4 and Fig.6 as a template allows short channel MOS models to be easily constructed from the equations listed in the reference cited in Table I. The set of nMOS transistor output curves drawn in Fig. 8 and Fig. 9 give an indication of the effects that adding short channel features to the EPFL-EKV 2.6 MOS model have on nMOS I-V output characteristics. The data shown in Fig. 8 and Fig. 9 applies to both the Verilog-A and Modelica short channel EPFL-EKV 2.6 models. Figure 8 shows the effect channel-length modulation has on the nMOS I-V output characteristics where the relative channel length reduction depends on the pinch-off point at the MOSFET channel drain end of the device. In the EPFL-EKV 2.6 model the channel-length modulation effect is modeled by

```
model EKV26nMOSCap
Modelica.Electrical.Analog.Interfaces.Pin D;
Modelica.Electrical.Analog.Interfaces.Pin G;
Modelica.Electrical.Analog.Interfaces.Pin S; Modelica.
Electrical.Analog.Interfaces.Pin B;
parameter Real L = 5e-07; parameter Real W = 1e-05;
parameter Real VTO = 0.6; parameter Real PHI = 0.97;
parameter Real GAMMA = 0.71;
parameter Real KP = 0.00015;
parameter Real THETA = 0.05; parameter Real DW = -2e-08;
parameter Real DL = -5e-08; parameter Real COX = 0.00345;
parameter Real TEMP = 26.85; parameter Real Xpart = 0.4;
parameter Integer CAPSWITCH = 0;
constant Real PQ = 1.602176462e-19; constant Real PK = 1.3806503e-23;
parameter Real P1 = -VTO + PHI + GAMMA * sqrt(PHI);
parameter Real P2 = GAMMA / 2; parameter Real P3 = P2 * P2;
parameter Real T2 = TEMP + 273.15; parameter Real VTT2 = (PK * T2) / PQ;
parameter Real P5 = PHI + 4 * VTT2; parameter Real P6 = (KP * W) / L;
parameter Real P7 = 1 / (2 * VTT2); parameter Real P8 = 2 * VTT2 * VTT2;
parameter Real P21 = PHI + 1e-06; parameter Real weff = W+DW;
parameter Real leff = L+DL; parameter Real P31 = COX*weff*leff;
parameter Real Spart = 1.0 - Xpart;
Real vgprime,vp,n,beta,iff1,iff,ir1,ir,Id, nq,xf,xr,qi,qg,qb,cgs,cgd,cdb,Px,csb,vpdash;
equation
vgprime = G.v + P1;
vp = if vgprime > 0.0 then
        vgprime - PHI - GAMMA * (sqrt(vgprime + P3) – P2)
      else -PHI;
n = 1 + P2 / sqrt(vp + P5); iff1 = log(1 + exp((vp - S.v) * P7));  iff = iff1 * iff1;
ir1 = log(1 + exp((vp - D.v) * P7)); ir = ir1 * ir1;
if CAPSWITCH == 1 then
 nq = 1 + GAMMA / (2 * sqrt(vp + P21)); xf = sqrt(0.25 + iff);  xr = sqrt(0.25 + ir);
 qi = nq * ((1.333333 * (xf * xf + xf * xr + xr * xr)) / (xr + xf) - 1.0);
if   vgprime > 0.0 then qb = (-GAMMA * sqrt(vp + P21)) / VTT2 - (nq - 1) / nq * qi;
else qb = -vgprime / VTT2;
end if;
qg = -qi - qb;
else
 nq = 0.0; xf = 0.0; xr = 0.0; qi = 0.0; qb = 0.0; qg = 0.0;
end if;
if CAPSWITCH == 1 then
Px = (xf + xr) * (xf + xr) + 1e-20;  cgs = P31 * 0.666666 * (1 - (xr * xr + xr + 0.5 * xf) / Px);
cgd = P31 * 0.666666 * (1 - (xf * xf + xf + 0.5 * xr) / Px);
csb = (nq - 1) * cgs; cdb = (nq - 1) * cgd;
else
 Px = 0.0; cgs = 0.0; cgd = 0.0; csb = 0.0; cdb = 0.0;
end if;
vpdash = 0.5 * vp + sqrt(vp * vp + P8); beta = P6 / (1 + THETA * vpdash);
Id = P8 * n * beta * (iff – ir); G.i = cgs * der(G.v - S.v) + cgd * der(G.v - D.v);
D.i = Id - cgd * der(G.v - D.v) + cdb * der(D.v - B.v);
S.i = -Id - cgs * der(G.v - S.v) + csb * der(S.v - B.v);
B.i = 0.0 - cdb * der(D.v - B.v) - csb * der(S.v - B.v);
end EKV26nMOSCap;
```

Fig. 6. Modelica non-linear long channel EPFL-EKV 2.6 nMOS DC model plus device intrinsic capacitances Cgs, Cgd, Cdb and Csb: default device parameters are listed in the initialization section of the model

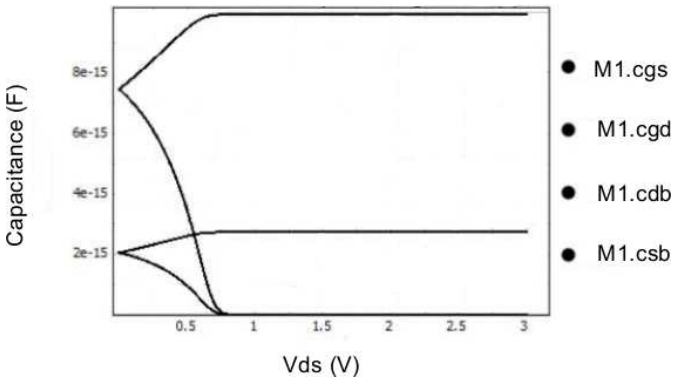

Fig. 7. Individual values for Modelica simulated nMOS intrinsic capacitances Cgs, Cgd, Cdb and Csb plotted as a function of Vds over the range 0 <= Vds <= 3V: default device parameters as listed in the initialization section of the model given in Fig.6

the depletion length coefficient parameter LAMBDA. Fig. 9 presents the I-V output characteristics for a device where all the short channel model effects have been include by setting all the model control switches to one. Although the differences between the curves shown in Fig. 8 and Fig. 9 appear small they can have a significant effect on device performance at very high frequencies. With reduced device feature sizes, compared to the parameters given in Fig. 1, inclusion of short channel effect becomes essential for accurate circuit simulation.

TABLE I
CONTROL SWITCHES FOR SELECTING SHORT CHANNEL EFFECTS

Switch	Short channel effect	Equations (in publication[9])
CLMSWITCH	Channel length modulation	58 to 62
TFMRSWITCH	Transconductance factor and mobility reduction due to vertical field	46, 48 to 55
CHSHSWITCH	Charge sharing for short narrow channels	34 to 38
RSCESWITCH	Reverse short channel effect	30 to32

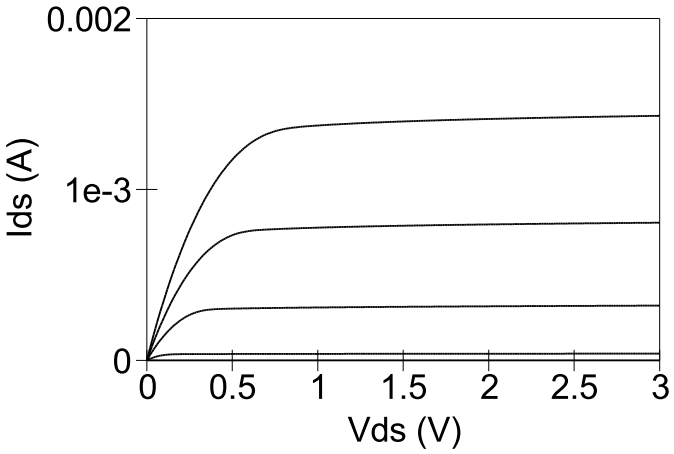

Fig. 8. Typical nMOS transistor output characteristics showing the effects caused by setting short channel control switches: CLMSWITCH=1, TFRMRSWITCH=0, CHSHSWITCH=0, RSCESWITCH=0 and CHARGESWITCH or CAPSWITCH=0

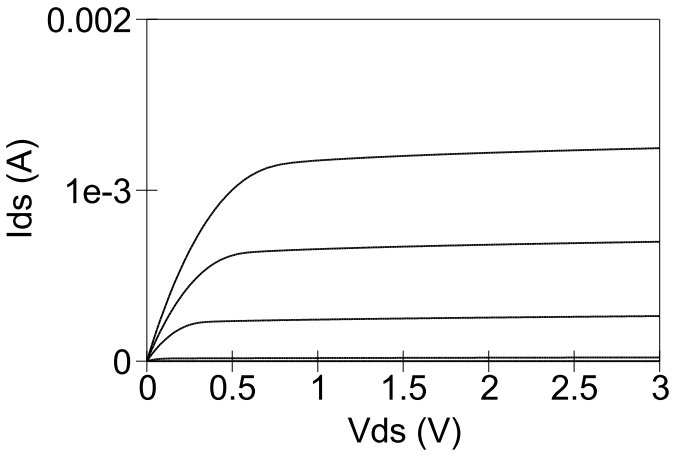

Fig. 9. Typical nMOS transistor output characteristics showing the effects caused by setting short channel control switches: CLMSWITCH=1, TFRMRSWITCH=1, CHSHSWITCH=1, RSCESWITCH=1 and CHARGESWITCH or CAPSWITCH=0

V. Adding probes to Verilog-A compact semiconductors for monitoring device performance during simulation

One of the most striking differences between Verilog-A and current implementations of the Modelica hardware description language is the ability of the latter to automatically record, during simulation, values for all the variables that contribute to a set of model equations. This allows a complete post simulation analysis of the performance of a model to be undertaken easily as part of a model validation sequence. One approach with Verilog-A to obtain values for model internal signals, equations and variables is to add extra signal nets to a model interface as part of the Verilog-A module statement. These nets act as data highways for internal model probes. Two obvious types of signal probe structure can be built into Verilog-A compact device models: firstly parallel signal probes with one probe per signal or internal variable, and secondly serial signal probes which can be switched to monitor specific signals by setting the value of a control variable prior to simulation. In practice, a combination of both parallel and serial probes are often employed to give coverage of a range of internal device signals and variable values, with priority signals connected to parallel probes. Figure 10 illustrates a typical combined parallel and series model probe configuration, here different line styles are employed to indicate the parallel and serial probes. Fig. 11 shows the Verilog-A code for the parallel and serial probe signal highways and the internal model quantities being monitored. Notice that setting variable SBUSSWITCH to zero disables the serial monitoring bus and setting CHARGESWITCH to zero also disables the parallel monitoring bus. Fig. 12 shows a typical group of internal model signals obtained from transistor output characteristic simulation tests.

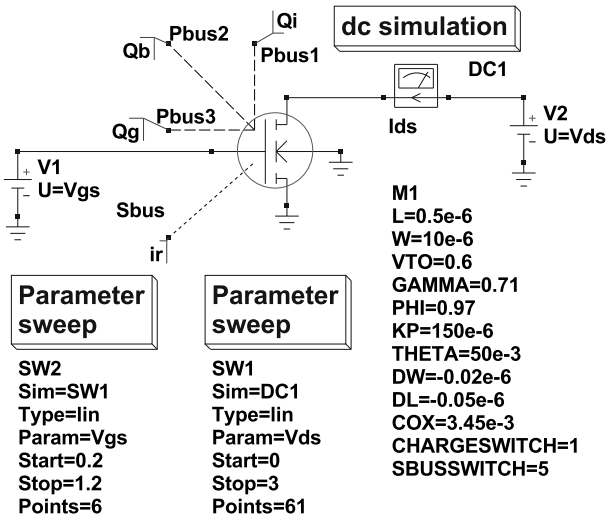

Fig. 10. EPFL-EKV 2.6 nMOS transistor I-V output characteristic test circuit with parallel and serial data monitoring bus structures

```
`include "disciplines.vams"
`include "constants.vams"
module EKV26nMOSProbe(drain,gate,source,bulk,
                      Sbus,Pbus1,Pbus2,Pbus3);
inout drain,gate,source,bulk,Sbus,Pbus1,Pbus2,Pbus3;
electrical drain,gate,source,bulk,Sbus,Pbus1,Pbus2,Pbus3;
                  :
                  :
paremeter integer CHARGESWITCH=0 from [0:1];
parameter integer SBUSSWITCH=0 from [0:5];
                  :
                  :
real nq,P21,xf,xr,qi,qb,qg,coxide,Qi,Qb,Qg,Spart,I_Sbus,vpdash;
                  :
                  :
if  (SBUSSWITCH==1) I_Sbus=vp;
else if  (SBUSSWITCH==2) I_Sbus=n;
else if  (SBUSSWITCH==3) I_Sbus=beta;
else if  (SBUSSWITCH==4) I_Sbus=iff;
else if  (SBUSSWITCH==5) I_Sbus=ir;
else I_Sbus=0.0;
I(Sbus)   <+ -I_Sbus;
I(Sbus)   <+ V(Sbus);
I(Pbus1) <+ -CHARGESWITCH*Qi;
I(Pbus1) <+ V(Pbus1);
I(Pbus2) <+ -CHARGESWITCH*Qb;
I(Pbus2) <+ V(Pbus2);
I(Pbus3) <+ -CHARGESWITCH*Qg;
I(Pbus3) <+ V(Pbus3);
end
endmodule
```

Fig. 11. Serial and Parallel signal monitoring Verilog-A code for a long channel EPFL-EKV 2.6 nMOS transistor model: Only those lines of code which need to be modified or added to the Verilog-A code given in Fig. 4 are listed

VI. Conclusion

Adaptive versions of complex compact semiconductor models promote simplified device modeling via user selective equation-defined model structures. This type of compact model provides users with the opportunity to select device features which are "custom built" to meet the requirements of specific types of circuit simulation. In reality, when selecting model features, there is a trade off between model complexity and simulation speed, which in turn encourages users to select a model with minimum complexity that offers improved simulation speed. This paper outlines the adaptation of the well known EPFL-EKV 2.6 MOS model as a structured semiconductor device model, while simultaneously presenting Verilog-A and Modelica simulation data which illustrates some of properties, and advantages, of modular compact device models.

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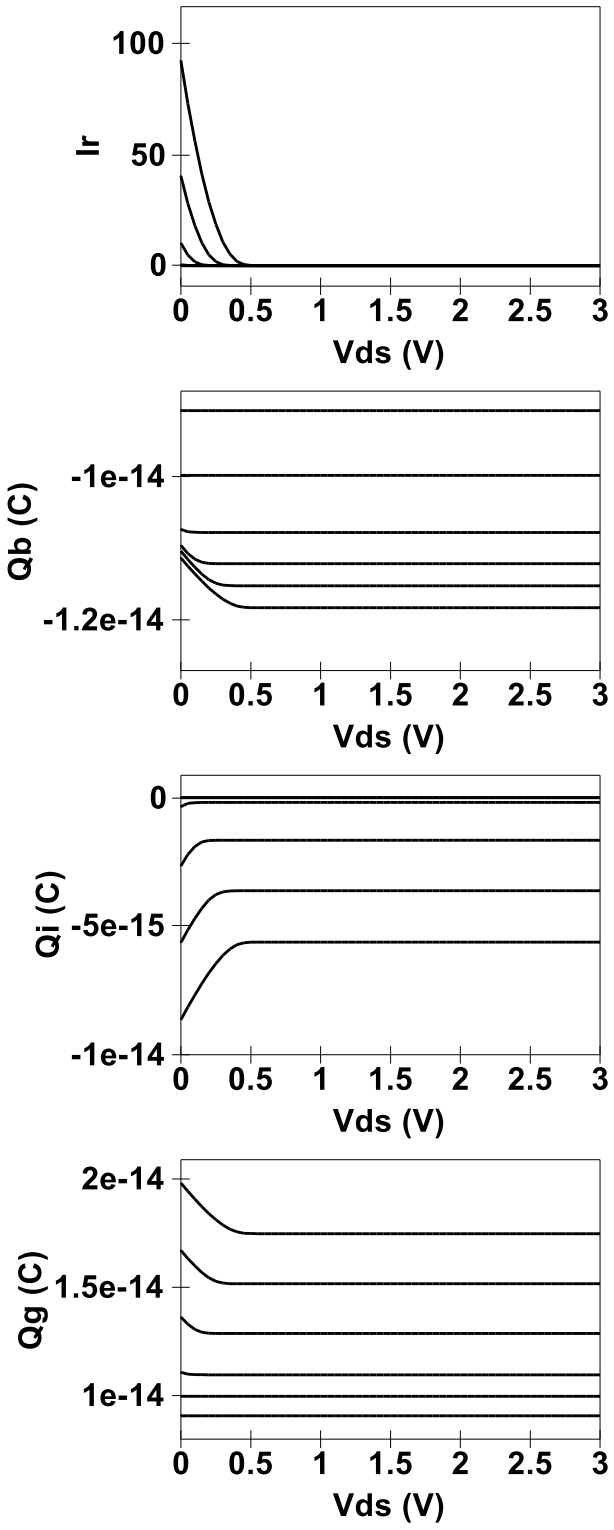

Fig. 12. A typical set of serial and parallel monitoring bus signals plotted as a function of Vds: SBUSSWITCH=5, CHARGESWITCH=1 and other parameters the same as those given in Fig. 10

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