FOSS Compact Model Prototyping with Verilog-A Equation-Defined Devices (VAEDD)

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***Abstract*—Equation-Defined Device models (EDD) have become very popular for behavioural modelling of semiconductor and other non-linear devices. Two feature that makes them particularly attractive are their interactive nature and easy testing during the model development process. However, they are less suited for operation as production level models due to their slow simulation performance. This paper presents a new extension to the EDD that offers C++ model performance coupled with the convenience of EDD modelling. The extended form of the EDD is called a Verilog-A EDD or VAEDD for short. It has the same structure as the standard EDD but is built around compiled Verilog-A module code, which in turn is translated to C++ code and dynamically linked to the main body of the simulator code. Essentially a VAEDD is a tiny Verilog-A module with a standardised internal code structure. To demonstrate the interactive approach to compact model building with VAEDD components the design and testing of a high power SiC Schottky barrier diode is included in the main body of the text.**

***Index Terms*—Qucs, Qucs-S, QucsStudio, WRSPICE, Xyce, compact device modelling, Equation-Defined Devices (EDD), Verilog-A Equation-Defined Devices (VAEDD), SPICE B sources, SiC Schottky barrier diodes.**

I. INTRODUCTION

The conventional approach to adding new compact semiconductor device models to circuit simulators involves two radically different methods. Firstly, device models can be written in either C++ or C code, compiled and finally linked to the main circuit simulator, or secondly, they can be constructed from pre-defined non-linear and linear simulation components to form a behavioural model. Both of these techniques have their good and bad points. For example, in the first case, writing a low level C++ or C model requires a detailed understanding of simulator code structure and operation, plus an ability to manually code the model current and charge partial differentials that are needed for non-linear circuit simulation. Although the resulting C++ or C model can be highly optimized in terms of run time performance, development times are often long with a high probability of errors occurring during model construction due to the complexity of the task, making the method suitable primarily for specialist developers. Recently, the Verilog-A hardware description language has been adopted as a standard for compact semiconductor modelling [1], making the process of constructing C++ model code more straightforward, especially through the use of computer generated partial derivatives. In contrast to the use C++ code, or indeed Verilog-A module code for large models, building behavioural models using predefined simulation components is a highly interactive process that does not require developers to write, compile and link C++ or Verilog-A module code. One of its most important features of this process is testability where individual sections of a model can be built and tested as a model is evolved from a set of compact model equations and other data, making the process of debugging a model relatively straightforward. As behavioural device models are interpreted this can lead to excessively long simulation times. SPICE 3f5 uses a B type non-linear controlled voltage and current sources for modelling equation-derived device static I/V characteristics. However, the B style SPICE source does not include any charge storage features, forcing these sources to be combined with C and L components to represent, for example, capacitor current as $Icap = ddt(Qcap)$. The introduction of an advanced form of Equation-Defined Device (EDD) [2] [3] in the Qucs [4], Qucs-S [5] and QucsStudio [6] circuit simulators improved the lack of SPICE charge handling capabilities. Modelling with EDD is still an interactive interpretive process that does not however, increase circuit simulation computational speed. For small models this is not significant. However, with increasing behavioural model size it does become significant. This paper introduces a new advanced form of the Qucs EDD that allows individual EDD, to be replaced by a Verilog-A module called a VAEDD or by an XSPICE CodeModel equivalent [13]. The new VAEDD component consists of a C++ code block compiled from a Verilog-A module with the same function as the original EDD block. Depending on the overall improvement in circuit simulation speed required, one or more EDD can be replaced by VAEDD. This process is outlined diagrammatically in Fig. 1. To explain the structure and use of the new VAEDD component the construction of a SiC Schottky diode model is introduced and its simulation performance discussed.

II. SIC SCHOTTKY BARRIER DIODE CHARACTERISTICS

When compared to Si, SiC offers much improved properties for high power device design, including wide band gap (3.23 eV for 4H SiC compared to 1.1 eV for Si), the ability to operate at much higher temperatures (600 Celsius or better), larger saturation electron drift mobility (1450 cm^2/V against 900 cm^2/V), greater thermal conductivity (5 W/cm^2K against 1.5

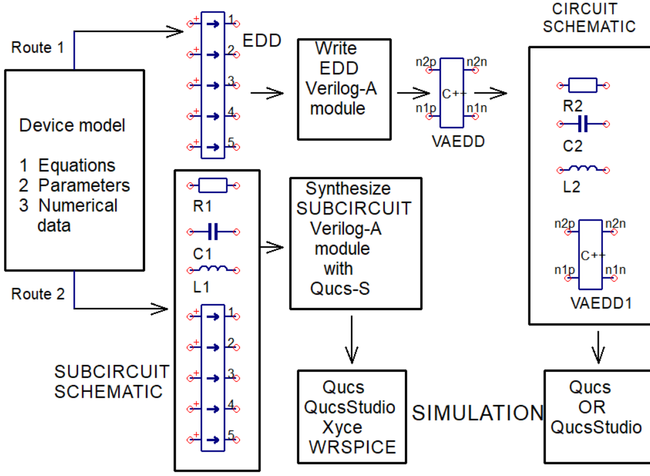


Fig. 1. A simplified block diagram outlining Verilog-A EDD (VAEDD) module development: Route 1 - single or multiple small VAEDD linked with other components; Route 2 - synthesis of Qucs/Qucs-S subcircuits.

W/cm^2K) and a very high breakdown field (roughly 10 times Si), making SiC a prime candidate for the next generation of power devices. The SiC Schottky barrier diode has emerged as an important semiconductor device for high power and frequency switching circuits. A number of SPICE analogue behavioural macromodels for SiC Schottky diodes have been reported in the published literature, including [7], [8], [9], [10]. A cross sectional diagram and equivalent circuit of a SiC Schottky barrier diode compact model similar to those previously published is shown in Fig. 2.

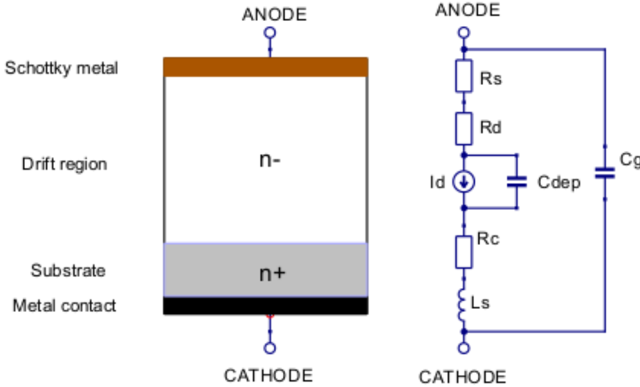


Fig. 2. Basic structure and equivalent circuit for a SiC Schottky barrier diode: Rs is the resistance of the Schottky metal contact, Rd is the resistance of the drift region, Id is the diode d.c. current at bias voltage Vd, Rc is the cathode metal contact resistance, $Cdep$ is the drift region depletion capacitance, Ls is the diode series inductance, and Cg is a small parallel capacitance whose value depends on the geometry of the device. Normally, the device contacts are considered to be ohmic with Rs and Rc in the range 1e-6 to 1e-4 Ω.

This diagram illustrates a SiC Schottky diode fabricated on an n^+ substrate with a metal ohmic cathode contact, an n^- drift region and a Schottky barrier metal ohmic anode contact. The diode current $I_d(T)$ and drift resistance $R_d(T)$ are given by

$$I_d(T) = Is(T) \cdot \left[exp\left(\frac{q \cdot V_d(T)}{n \cdot k \cdot T}\right) - 1.0 \right] \quad (1)$$

$$R_d(T) = Rd0 \cdot [1.0 + \triangle T \cdot (a_1 + a_2 \cdot \triangle T \cdot)] \quad (2)$$

where

$$T = TempK + K_t \cdot I_d(T) \cdot V_d(T) \quad (3)$$

$$\triangle T = (T - TempK) \quad (4)$$

$$I_s(T) = Is0 \cdot \left[\frac{T}{TempK}\right]^D \cdot exp\left(\frac{T}{TempK}\right) \quad (5)$$

Table I lists the SiC Schottky diode model parameters, outlines their meaning, and gives a set of default parameter values for a SiC "Zero Recovery Rectifier" type CSD01060 [11]. Symbols q and k have their usual meaning. $V_d(T)$ and $I_d(T)$ are the voltage across, and the current through, the equivalent circuit generator I_d at temperature T Kelvin. For diodes with a non-zero value of parameter kt thermal feedback occurs inducing a device temperature rise proportional to the power dissipated by a diode at high currents. The value of parameter $k1$ is critically dependent on the effective thermal resistance from the diode active region to the outside ambient environment via any installed heat sinks.

TABLE I
SiC SCHOTTKY BARRIER DIODE MODEL PARAMETER VALUES

Name	Description	Unit	Default
N	Emission coefficient		1.15
Is	Saturation current at Temp	A	3e-15
Rd0	Drift region resistance at Temp	Ω	0.42
Kt	Thermal resistance	K/W	6,4
a1	Rd linear temperature coefficient	$1/K$	0.0072
a2	Rd quadratic temperature coefficient	$1/(K*K)$	4.65e-5
D	Is temperature coefficient		2.95
Temp	Diode temperature	Celsius	27
Rs	Schottky metal resistance	Ω	0.0
Rc	Contact metal resistance	Ω	0.0
Cj0	Depletion capacitance at $V_d(T)$ = 0V	F	80e-12
Cg	Parallel capacitance	F	10e-15
Ls	Lead inductance	H	1e-11

III. PROTOTYPING THE SiC SCHOTTKY BARRIER DIODE COMPACT MODEL WITH EDD

A Qucs/Qucs-S subcircuit for the SiC Schottky diode illustrated in Fig. 2 is shown in Fig. 3. Equations (1) to (5) are calculated by the four EDD embedded in the SiC Schottky diode subcircuit, where EDD:D3:I1 represents term $K_t{\cdot}I_d(T){\cdot}V_d(T)$ in equation (3), EDD:D1:I1 represents $R_d(T)$ in equation (2), EDD:D2:I1 represents $I_d(T)$ in equation (1) and EDD:D4:I1 represents $I_s(T)$ in equation (5). Note the EDD currents I_2 and I_3 are ether set as I_n=0.0 or I_n = V_n. In the case where I_n=0.0 the EDD branch acts as a voltage probe. Similarly, when I_n = V_n the EDD branch acts as a current to voltage converter. Although Qucs, Qucs-S and QucsStudio EDD have their maximum number of branches per EDD set to 20 it is often simpler to model a device with multiple small EDD rather than a single large EDD. Figure 4 introduces a basic test bench for simulating the forward characteristics of

a series of Schottky diodes operating at different temperatures with thermal feedback. A plot of the simulation data recorded with the test bench shown in Fig. 4 is given in Fig.5. These curves are very similar to published manufacturers data [11].

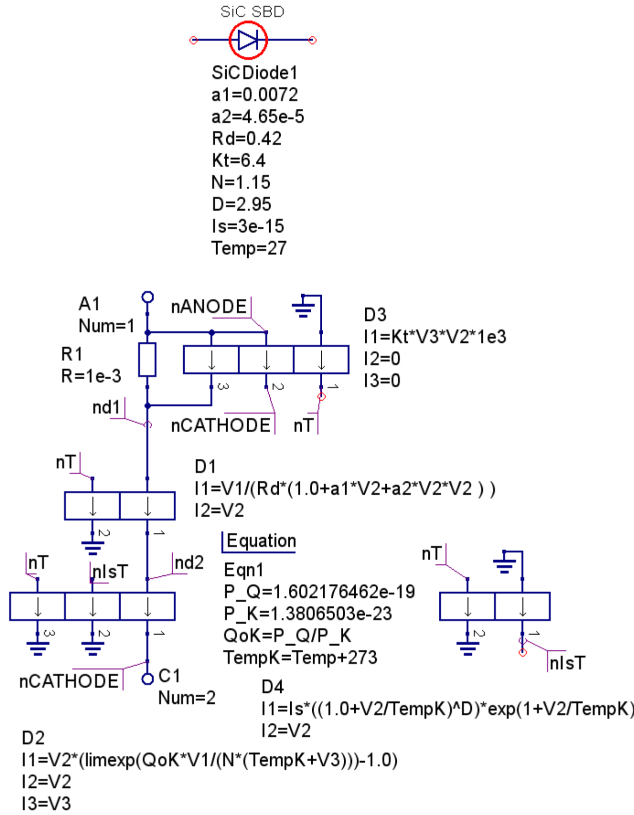


Fig. 3. An EDD subcircuit prototype of a SiC Schottky barrier diode: D1 - $Rd(T)$ equation (2); D2 - $Id(T)$ equation (1); D3 - part of equation (3); D4 - equation (5). Ls and Cg are not included and both Rs and Rc are considered small compared to Rd and therefore their effects have been neglected.

IV. Definition of VAEDD - the extended version of EDD

In the context of the style of compact modelling presented in this paper the new non-linear multi-terminal modelling component named VAEDD is structurally and functionally the same as the EDD it replaces, except that the body of the component consists of compiled C++ code rather than a set of instructions for interpreting its function during simulation, making it computationally more efficient when compared to the equivalent EDD. The VAEDD c++ can be generated using a Verilog-A to C++ module code compiler, for example the Automatic Device Model Synthesizer (ADMS) [12], the XSPICE C CodeModel development tools, using Qucs-S/Ngspice, or the Xyce [14] and RWSPICE [15] built-in versions of ADMS. The following sections explain the steps involved, concentrating on construction of VAEDD with the Qucs/Qucs-S and QucsStudio software. The other software tools are left for readers to experiment with.

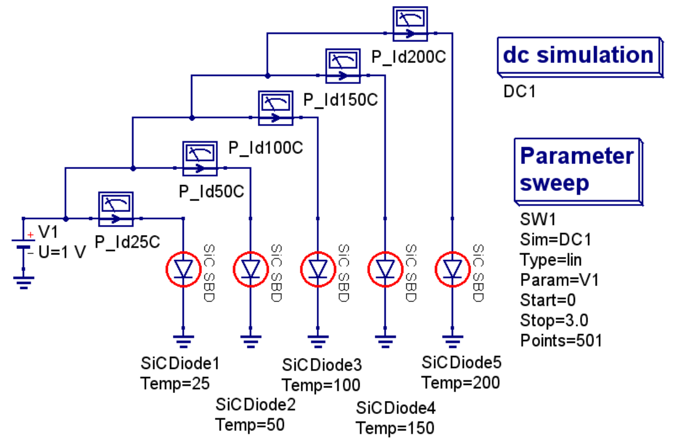


Fig. 4. Zero recovery SiC CSD01060 forward characteristics test bench circuit: with Kt = 6.4 (K/W) and the device temperature Temp in the range 75 to 200 degrees Celsius respectively.

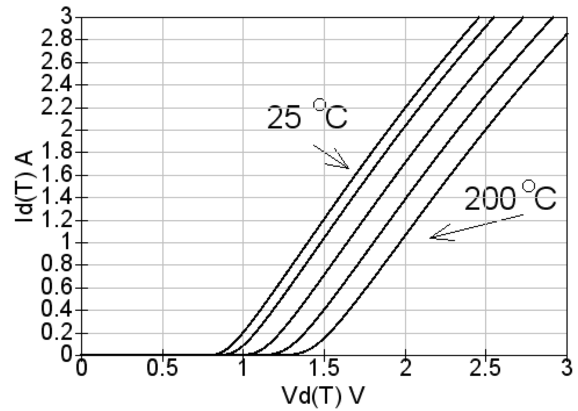


Fig. 5. Zero recovery SiC CSD01060 forwrd characteristics with parameter kt set at 6.4 K/W.

V. Prototyping the SiC Schottky barrier diode model with VAEDD

The process of building a VAEDD is essentially very simple. Firstly, an EDD for a given specification is constructed and tested, see Fig. 3. When it is working without bugs the Verilog-A equivalent module code is written, compiled to C++ code and attached to a suitable component symbol. Figure 6 is identical to Fig. 3 except that EDD:D3 and EDD:D4 have been replaced by manually written Verilog-A modules VAEDD1 and VAEDD2 respectively, compiled by QucsStudio, and labelled with component type code X. The Verilog-A module code for the two replaced EDD are given in the inserts in Fig. 6 (here EDD:D3 becomes VAEDD:X5 and EDD:D4 becomes VAEDD:X1). These are very similar in structure varying only by the number of device pins and I_n entries. Notice the use of the Verilog-A branch statement to simplify the module code. This is considered good practice and is recommended. The compiled C++ VAEDD blocks can be easily generated using QucsStudio by simulating the EDD Verilog-A module code.

This process also links the compiled C++ module code to a software generated VAEDD symbol. Passing higher level parameter values down the model hierarchy to VAEDD is done by equating parameter names to themselves in a VAEDD:Xn specification (for example D=D in VAEDD2 Fig. 6). Figure 7 gives d.c. data similar to the set shown in Fig. 5 except that the have been generated with the VAEDD version of the SiC Schottky barrier diode model with parameter Kt set to 0.0 K/W. The differences between the two sets of plotted data imply that there are measurable variations in the diode d.c. characteristics with and without thermal feedback.

VI. Adding dynamic charge properties to the SiC Schottky barrier diode model with VAEDD

The SiC Schottky barrier diode is a majority carrier device that offers much improved switching speeds when compared to a p-n junction device where currents are removed by extracting minority carries through diffusion or recombination processes. In a p-n junction diffusion capacitance dominates the forward characteristics of a diode. In a Schottky barrier diode the diffusion capacitance is either zero or very small. This is signified by assuming that the Schottky barrier diode transit time (SPICE diode parameter TT) can be set to zero seconds. Hence the switching characteristics of the Schottky barrier diode are largely determined by depletion capacitance $Cdep$ and drift resistance $Rd(T)$, where $Rd(T)$ is given by equation (2) and

$$Cdep = \frac{dQ_{dep}}{dVd(T)} = Area \cdot Cj0 \cdot \left(1.0 - \frac{Vd(T)}{Vj}\right)^{-M} \quad (6)$$

For the operating voltage range $Vd(T) < Fc \cdot Vj$ let the diode stored charge Qdep1 equal

$$Qdep1 = Cd \cdot \int_0^{Vd(T)} \left(1.0 - \frac{V}{Vj}\right)^{-M} dV \quad (7)$$

$$= \frac{Cd \cdot Vj}{1 - M} \cdot \left[1.0 - \left(1.0 - \frac{Vd(T)}{Vj}\right)^{1-M}\right] \quad (8)$$

Similarly, for the voltage operating range $Vd(T) >= Fc \cdot Vj$ let the diode stored charge Qdep2 equal

$$Qdep2 = Cd \cdot \left[F1 + \frac{1}{F2} \int_{Fc \cdot Vj}^{Vd(T)} \left(F3 + \frac{M \cdot V}{Vj}\right) dV\right] \quad (9)$$

$$= Cd\left[F1 + \frac{1}{F2} \cdot Z1\right] \quad (10)$$

$$Cd = Area \cdot CJ0 \quad (11)$$

$$Z1 = (F3 \cdot (Vd(T) - Fc \cdot Vj) + F4 \cdot Z0) \quad (12)$$

$$Z0 = (Vd(T) \cdot Vd(T) - F5 \cdot F5) \quad (13)$$

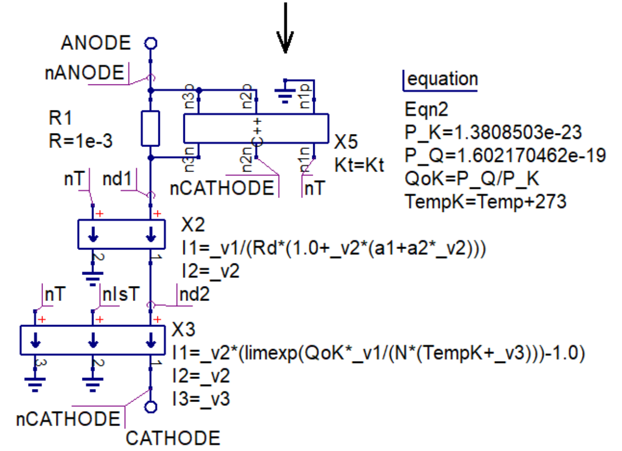
$$F1 = \frac{Vj}{1 - M} \cdot \left[1.0 - (1 - Fc)^{1-M)}\right) \quad (14)$$

$$F2 = (1 - Fc)^{1-M} \quad (15)$$

$$F3 = 1 - Fc \cdot (1 + M)) \quad (16)$$

$$F4 = \frac{M}{2 \cdot Vj} \quad (17)$$

```
`include "disciplines.vams"
`include "constants.vams"
module VAEDD1(n3p, n3n, n2p, n2n, n1p, n1n);
inout n3p, n3n, n1p, n2p, n1n, n2n;
electrical n1p, n1n, n2p, n2n, n3p, n3n;
parameter real Kt = 6.4;
branch (n1p, n1n) B1;
branch (n2p, n2n) B2;
branch (n3p, n3n) B3;
analog begin
I(B1) <+ Kt*V(B3)*V(B2)*1e3;
end
endmodule
```




```
`include "disciplines.vams"
`include "constants.vams"
module VAEDD2(n2p, n2n, n1p, n1n);
inout n1p, n2p, n1n, n2n;
electrical n1p, n1n, n2p, n2n;
parameter real Is = 3e-15;
parameter  real D = 2.95;
parameter real TempK = 300.0;
branch (n1p, n1n) B1;
branch (n2p, n2n) B2;
analog begin
I(B1) <+ Is*(pow(1.0+V(B2)/TempK, D));
I(B2) <+ V(B2);
end
endmodule
```

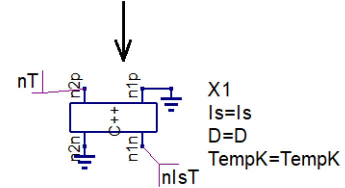


Fig. 6. SiC Schottky diode model with EDD blocks D3 and D4 each replaced by a separate VAEDD

$$F5 = Fc \cdot Vj \quad (18)$$

Where M is a grading coefficient, $CJ0$ is the zero d.c. bias diode depletion capacitance, Vj is the junction potential and $Area$ is the relative device area. The Verilog-A code for VAEDD4 is given in Fig. 8. In VAEDD4 depletion capacitor equations $Qdep1$ and $Qdep2$ are accessed and combined by a Verilog-A if-else statement. The S parameter test bench shown in Fig. 9 is capable of determining $S[1,1]$ from simulation and

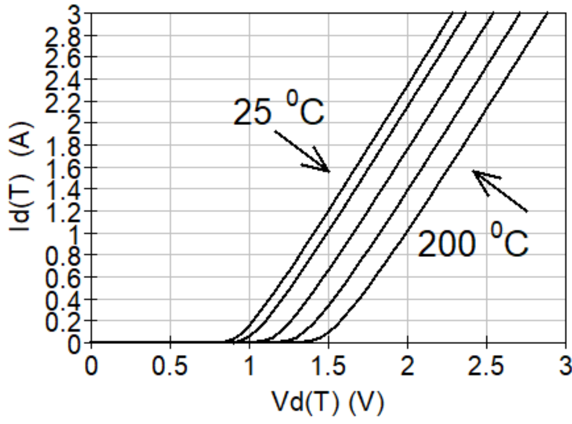


Fig. 7. Zero recovery SiC CSD01060 forward characteristics with parameter kt set at 0.0 K/W

extracting diode equivalent circuit parameters Rd and $Cj0$ at temperature $TempK$ K. The d.c. bias voltage Vdc is also swept over the range -100 V to 0 V in order to check the variation of $Cdep$ and Rd. The -100V to 0V bias voltage range ensures that the SiC Schottky barrier diode is reverse biased and that its small signal a.c. equivalent circuit simplifies to an impedance, where $z = Rd - j/(2 \cdot pi \cdot frequency \cdot Cdep)$. Hence, after converting $S[1,1]$ to impedance z, Rd can be found from $real(z)$ and $Cdep$ from $-1/(imag(z) \cdot 2 \cdot pi \cdot frequency)$.

VII. Simulation of a SiC Schottky diode forward recovery time.

The final test circuit in this paper is given in Fig .10. In this test bench the SiC Schottky barrier diode, plus parasitic components Ls and Cg is turned from an ON state (2 A d.c forward bias) to an OFF state (0 V d.c bias) in a fraction of a nano second. With the device transit time set at zero seconds the observed diode recovery time should also approach zero seconds, being determined by the residual charge stored by $Cdep$. With $Cdep \approx$ 100pF and $Rd \approx$ 0.4 Ω the turn-off time constant is roughly 40 ps, confirming the order of magnitude suggested by th Id.It versus time(s) curve illustrated in Fig. 10.

VIII. Conclusion

It is slightly over ten years since the EDD was introduced into the compact modelling repertoire. Although the EDD has been a very successful new modelling component, being widely used as a straightforward non-linear interactive prototyping element, it is characterised by slow simulation speed when compared to compiled C++ compact device models. This paper introduces a new extension to the EDD called a VAEDD that largely overcomes the EDD speed limitations. The VAEDD extension has an identical structure to the EDD but replaces its internal interpreted code with a Verilog-A module synthesized to C++, compiled and dynamically linked to the nain body of circuit simulation code. In most respects

```
`include "disciplines.vams"
`include "constants.vams"
module VAEDD4(n1p, n1n);
inout n1p, n1n;
electrical n1p, n1n;
parameter real Cj0=111.88e-12;
parameter real M=0.39264;
parameter real Vj=0.54581;
parameter real Fc=0.5;
parameter real Area=1.0;
real F1, F2, F3;
branch (n1p, n1n) B1;
analog begin
@(initial_model)
begin
F1=(Vj/(1-M))*(1-pow(1-Fc,(1-M)));
F2=pow(1-Fc,(1+M));
F3=1-Fc*(1+M);
end
if (V(B1)<Fc*Vj)
 begin
  I(B1)<+ddt((Area*Cj0*Vj/(1-M))*(1-pow(1-V(B1)/Vj,
        (1-M))));
 end
else
 begin
  I(B1)<+ddt(Area*Cj0*F1+(Area*Cj0/F2)*(F3*(V(B1)-Fc*Vj)+
          (M/(2*Vj))*(V(B1)*V(B1)-Fc*Fc*Vj*Vj)));
 end
end
endmodule
```

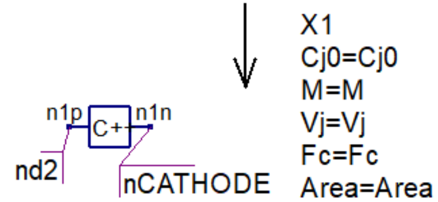


Fig. 8. SiC Schottky diode depletion capacitance modelled by a two terminal VAEDD: pins labelled nd2 (n1p) and nCATHODE (n1n) connect to the same named pins in Fig. 6. The $Cdep(T)$ VAEDD evaluates diode depletion capacitance at different d.c. voltage bias values and temperature $T = TempK$.

a VAEDD can be considered to be a very small Verilog-A compact model that is built around the EDD pin layout and a prescribed internal code template. By adopting this arrangement for the VAEDD extension to the EDD it becomes possible to develop a new compact device model using EDD, and indeed other simulation components, then to replace one or more EDD with an equivalent number of VAEDD if better overall model performance is required. An interesting side effect of the new VAEDD block is that different VAEDD can be developed and arranged as a library for future reuse. A good example of such an element is the VAEDD4 block introduced in the text for modelling depletion capacitance. A number of exampl VAEDD have been introduced to demonstrate the construction of a compact model for a SiC Schottky barrier diode.

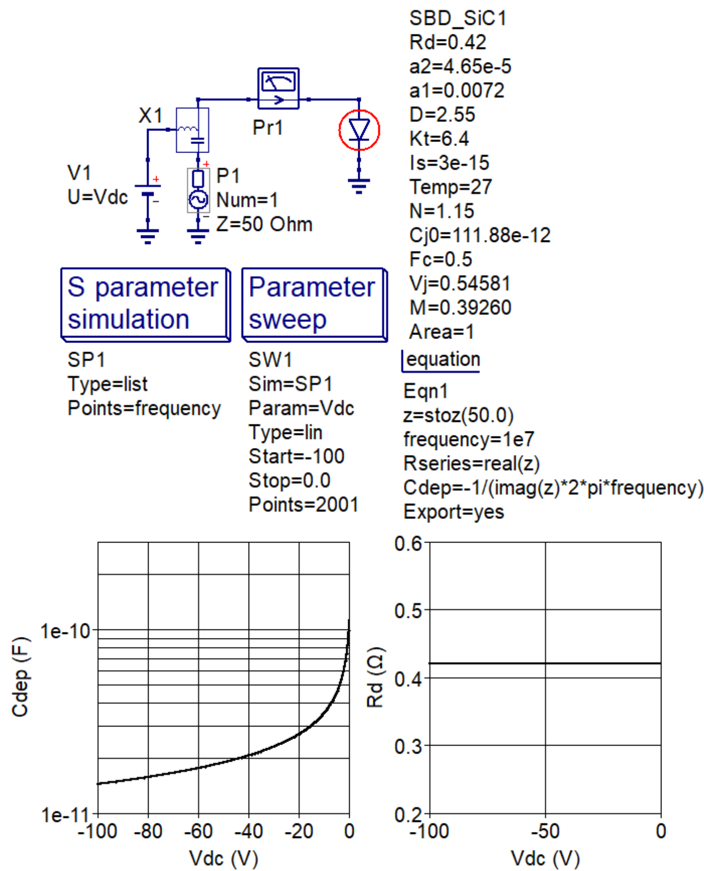


Fig. 9. S parameter test bench for extracting SiC Schottky barrier diode parameters from small signal a.c. simulation.

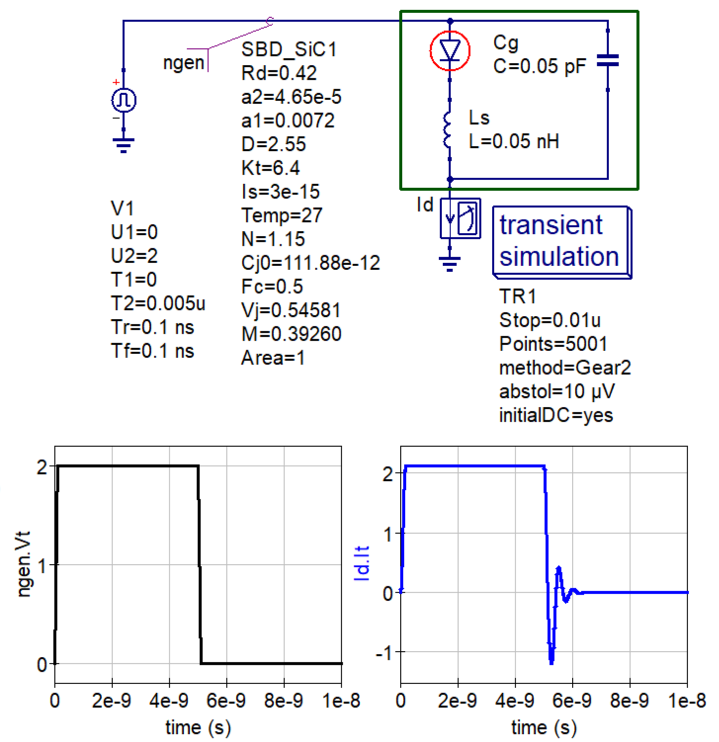


Fig. 10. SiC Schottky barrier diode test bench for estimating zero forward recovery time from simulation data: the Schottky barrier diode is modelled with the compact model introduced in Fig. 6 plus the $Cdep$ VAEDD shown in Fig.8.

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