FOSS Compact Model Prototyping with Verilog-A Equation-Defined Devices (VAEDD)

Mike Brinson
Centre for Communications Technology,
London Metropolitan University, UK
Email: mbrin72043@yahoo.co.uk

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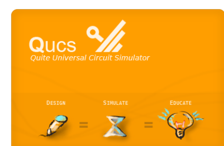

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FOSS Compact Model Prototyping with Verilog-A Equation-Defined Devices (VAEDD): Introduction

- The conventional approach to adding new compact semi-conductor device models to circuit simulators involves two radically different methods: C++ or C code models or pre-defined non-linear and linear simulation components arranged as a behavioural model. Both of these techniques have their good and bad points.
- For example, in the first case, writing a low level C++ or C model requires a detailed understanding of simulator code structure and operation, plus an ability to manually code the model current and charge partial differentials that are needed for non-linear circuit simulation.
- Although the resulting C++ or C model can be highly optimized in terms of run time performance,development times are often long with a high probability of errors occurring during model construction due to the complexity of the task, making the method suitable primarily for specialist developers.
- Recently, the Verilog-A hardware description language has been adopted as a standard for compact semiconductor modelling, making the process of constructing C++ model code more straightforward, especially through the use of computer generated partial derivatives.
- In contrast to the use C++ code, or indeed Verilog-A module code for large models, building behavioural models using predefined simulation components is a highly interactive process that does not require developers to write, compile and link C++ or Verilog-A module code.
- One of its most important features of this process is testability where individual sections of a model can be built and tested as a model is evolved from a set of compact model equations and other data, making the process of debugging a model relatively straightforward.

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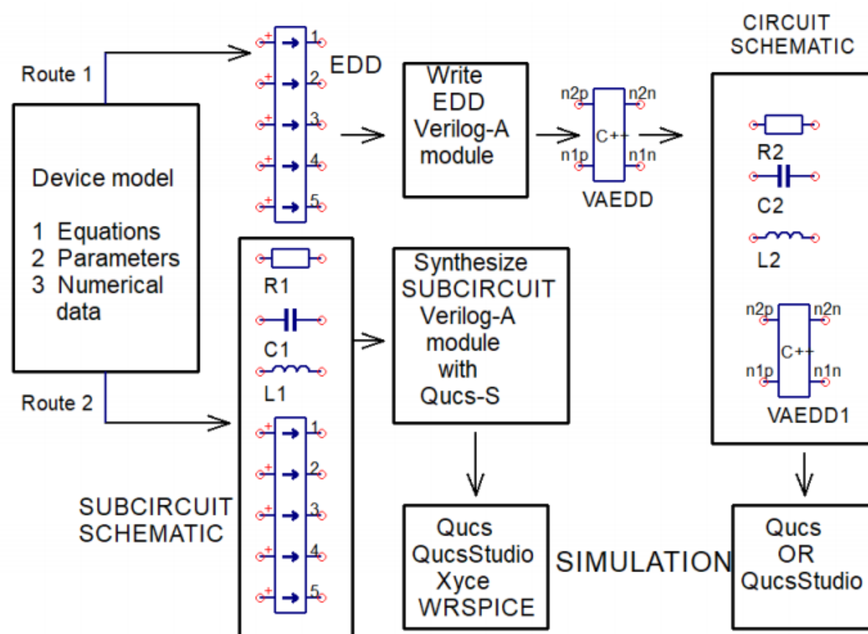
• As behavioural device models are interpreted this can lead to excessively long simulation times. SPICE 3f5 uses a B type non-linear controlled voltage and current sources for modelling equation-derived device static I/V characteristics. However, the B style SPICE source does not include any charge storage features, forcing these sources to be combined with C and L components to Represent, for example, capacitor current as *Icap = ddt(Qcap)*.

• The introduction of an advanced form of Equation-Defined Device (EDD) improved the lack of SPICE charge handling capabilities. Modelling with EDD is still an interactive interpretive process that does not however, increase circuit simulation computational speed.

• This paper introduces a new advanced form of the Qucs EDD that allows individual EDD, to be replaced by a Verilog-A module called a VAEDD. The new VAEDD component consists of a C++ code block compiled from a Verilog-A module with the same function as the original EDD block. Depending on the overall improvement in circuit simulation speed required, one or more EDD can be replaced by VAEDD.



A simplified block diagram outlining Verilog-A EDD (VAEDD) module development:

Route 1 - single or multiple small VAEDD linked with other components;

Route 2 - synthesis of Qucs/Qucs-S subcircuits.

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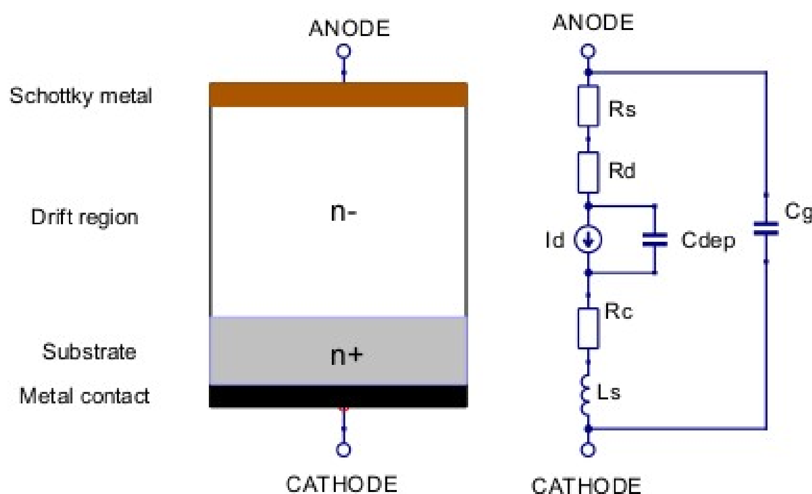
FOSS Compact Model Pototyping with Verilog-A Equation-Defined Devices (VAEDD): SiC Schottky barrier diode characteristics

Fundamental material properties

When compared to Si, SiC offers much improved properties, including
(1) wide band gap (3.23 eV for 4H SiC compared to 1.1 eV for Si),
(2) the ability to operate at much higher temperatures (600 Celsius or better),
(3) larger saturation electron drift mobility (1450 cm^2 /V against 900 cm^2 /V),
(4) greater thermal conductivity (5 W/cm^2 K against 1.5 W/cm^2 K),
(5) a very high breakdown field (roughly 10 times Si), making SiC a prime candidate for the next generation of power devices.



Basic structure and equivalent circuit for a SiC Schottky barrier diode:
Rs is the resistance of the Schottky metal contact,
Rd is the resistance of the drift region,
Id is the diode d.c. current at bias voltage *Vd*,
Rc is the cathode metal contact resistance,
Cdep is the drift region depletion capacitance,
Ls is the diode series inductance, and
Cg is a small parallel capacitance whose value depends on the geometry of the device.

Normally, the device contacts are considered to be ohmic with *Rs* and *Rc* in the range 1e-6 to 1e-4 Ω.

This diagram illustrates a SiC Schottky diode fabricated on an n + substrate with a metal ohmic cathode contact, an n − drift region and a Schottky barrier metal ohmic anode contact.

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The diode current *Id (T)* and drift resistance *Rd (T)* are given by:

$$I_d(T) = Is(T) \cdot \left[exp\left(\frac{q \cdot V_d(T)}{n \cdot k \cdot T} \right) - 1.0 \right]$$

$$R_d(T) = Rd0 \cdot [1.0 + \triangle T \cdot (a_1 + a_2 \cdot \triangle T \cdot)]$$

where

$$T = TempK + K_t \cdot I_d(T) \cdot V_d(T)$$

$$\triangle T = (T - TempK)$$

$$I_s(T) = Is0 \cdot \left[\frac{T}{TempK} \right]^D \cdot exp\left(\frac{T}{TempK} \right)$$

SiC Schottky barrier diode model parameter values

Name	Description	Unit	Default
N	Emission coefficient		1.15
Is	Saturation current at Temp	A	3e-15
Rd0	Drift region resistance at Temp	Ω	0.42
Kt	Thermal resistance	K/W	6,4
a1	Rd linear temperature coefficient	$1/K$	0.0072
a2	Rd quadratic temperature coefficient	$1/(K * K)$	4.65e-5
D	Is temperature coefficient		2.95
Temp	Diode temperature	Celsius	27
Rs	Schottky metal resistance	Ω	0.0
Rc	Contact metal resistance	Ω	0.0
Cj0	Depletion capacitance at $V_d(T)$ = 0V	F	80e-12
Cg	Parallel capacitance	F	10e-15
Ls	Lead inductance	H	1e-11

The Table lists the SiC Schottky diode model parameters, outlines their meaning, and gives a set of default parameter values for a SiC "Zero Recovery Rectifier" type CSD01060. Symbols *q* and k have their usual meaning. *Vd (T)* and *Id (T)* are the voltage across, and the current through, the equivalent circuit generator *Id* at temperature *T* Kelvin. For diodes with a non-zero value of parameter *kt* thermal feedback occurs inducing a device temperature rise proportional to the power dissipated by a diode at high currents. The value of parameter *Kt* Is critically dependent on the effective thermal resistance from the diode active region to the outside ambient environment via any installed heat sinks.

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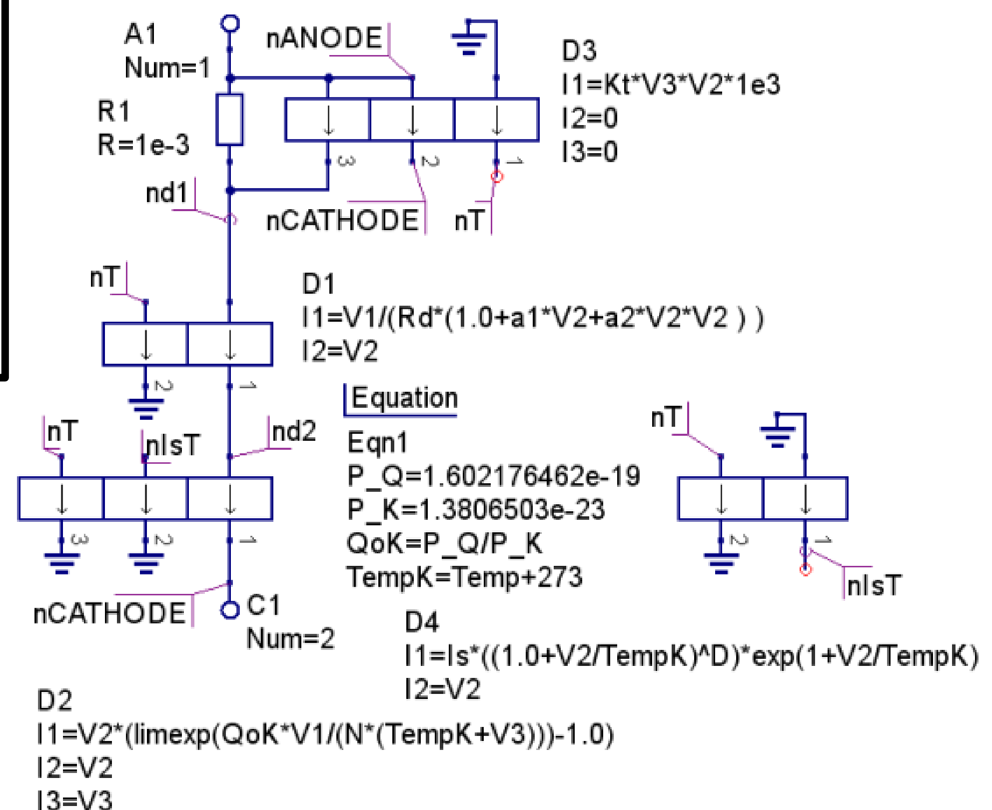
SiCDiode1
a1=0.0072
a2=4.65e-5
Rd=0.42
Kt=6.4
N=1.15
D=2.95
Is=3e-15
Temp=27

A Qucs/Qucs-S subcircuit for the SiC Schottky diode. Previously introduced compact model equations are calculated by the four EDD embedded in the SiC Schottky diode subcircuit, where EDD:D3:I1 represents term *K t ·I d (T)·Vd (T)*, EDD:D1:I1 represents *Rd (T)*, EDD:D2:I1 represents *Id (T)* and EDD:D4:I1 represents *Is (T)*. Note the EDD currents *I2* and *I3* are ether set as *In =0.0* or *In = Vn* . In the case where *In = 0.0* the EDD branch acts as a voltage probe. Similarly, when *In = Vn* the EDD branch acts as a current to voltage converter. Although Qucs-S and QucsStudio EDD have their maximum number of branches per EDD set to 20 it is often simpler to model a device with multiple small EDD rather than a single large EDD.



An EDD subcircuit prototype of a SiC Schottky barrier diode: D1 -*Rd(T)*; D2 - *Id(T)*; D3 - part of the equation for *T*; D4 – the equation for *Is(T)* .

NOTE: *Ls* and *Cg* are not included and both *Rs* and *Rc* are considered small compared to Rd and therefore their effects have been neglected.

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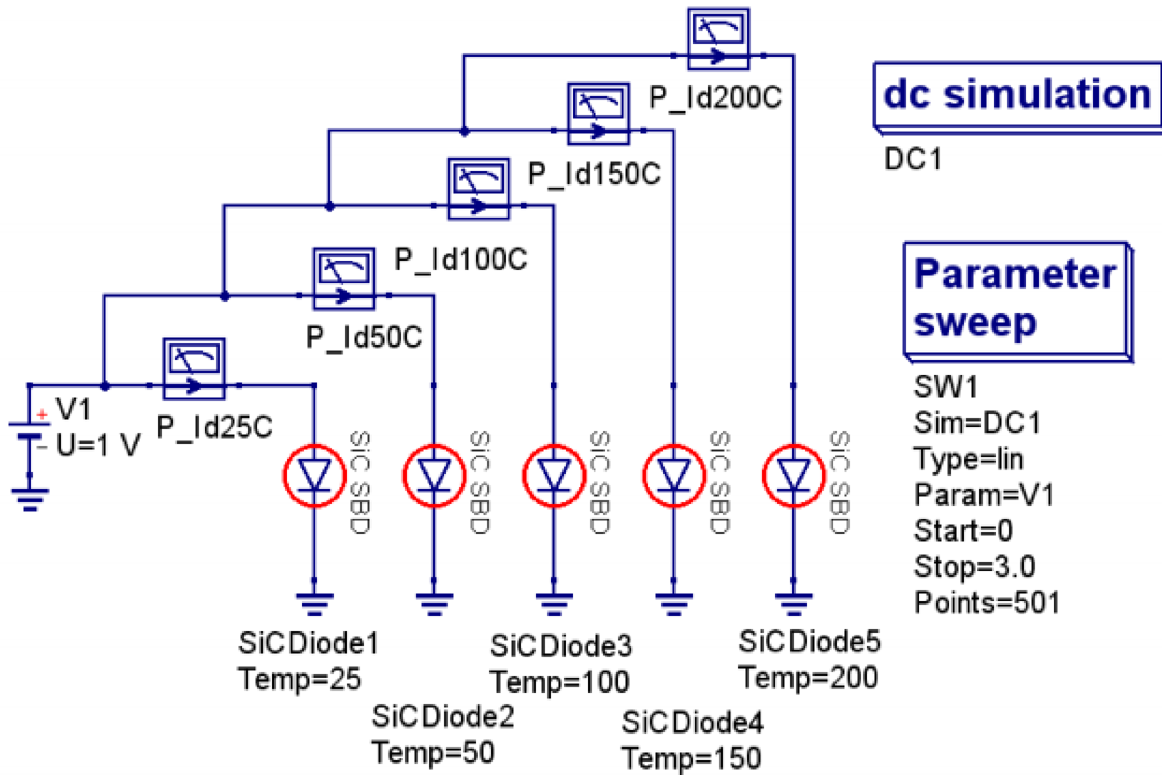
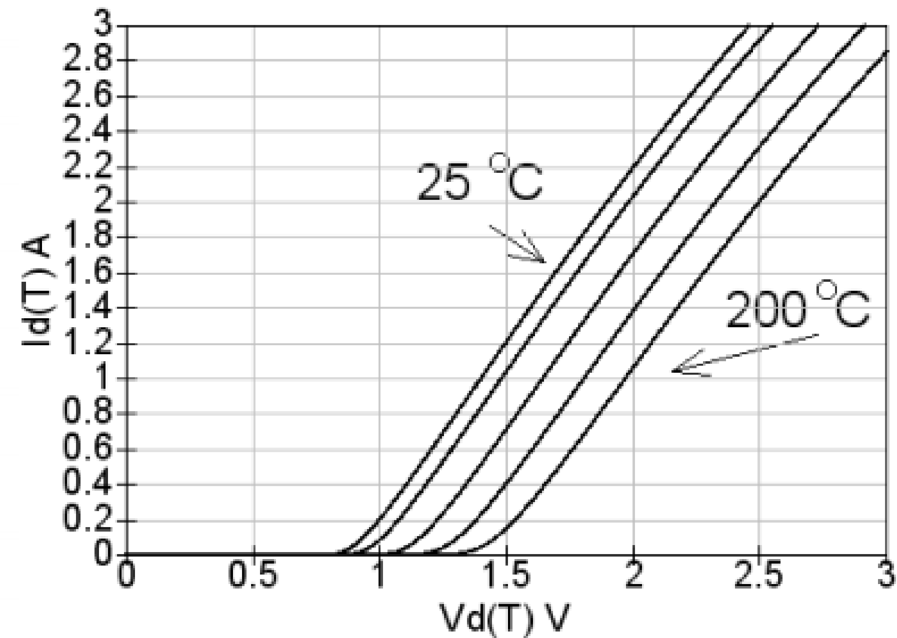


Zero recovery SiC CSD01060 forward characteristics test bench circuit: with *Kt* = 6.4 (K/W) and the device temperature Temp in the range 75 to 200 degrees Celsius respectively.



Zero recovery SiC CSD01060 forward characteristics with parameter *kt* set at 6.4 K/W.

FOSS Compact Model Pototyping with Verilog-A Equation-Defined Devices (VAEDD): Definition of VAEDD – the Extended Version of EDD

In the context of the style of compact modelling presented in this talk the new Non-linear multi-terminal modelling component named VAEDD is structually and functionally the same as an EDD.

However, It replaces an EDD with the body of a component consisting of compiled C++ code rather than a set of equations for modelling its function during simulation.

A VAEDD is computationally more efficient when compared to its equivalent EDD.

VAEDD C++ code can be generated using a Verilog-A to C++ module code compiler, for example the Automated Device Model Synthesizer (ADMS).

The following slides the outline the steps involved in developing compact models with both EDD and VAEDD contributions , concentrating on construction of VAEDD with the Qucs/Qucs-S and QucsStudio circuit simulation and modelling software.

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The process of building a VAEDD is essentially very simple. Firstly, an EDD for a given specification is constructed and tested, see slide 6.

When it is working without bugs the Verilog-A equivalent module code is written, compiled to C++ code and attached to a suitable component symbol.

The schematic on slides 9 and 10 is identical to the schematic shown in slide 6 except that EDD:D3 and EDD:D4 have been replaced by manually written Verilog-A modules VAEDD1 and VAEDD2 respectively, compiled by QucsStudio, and labelled with component type code X.

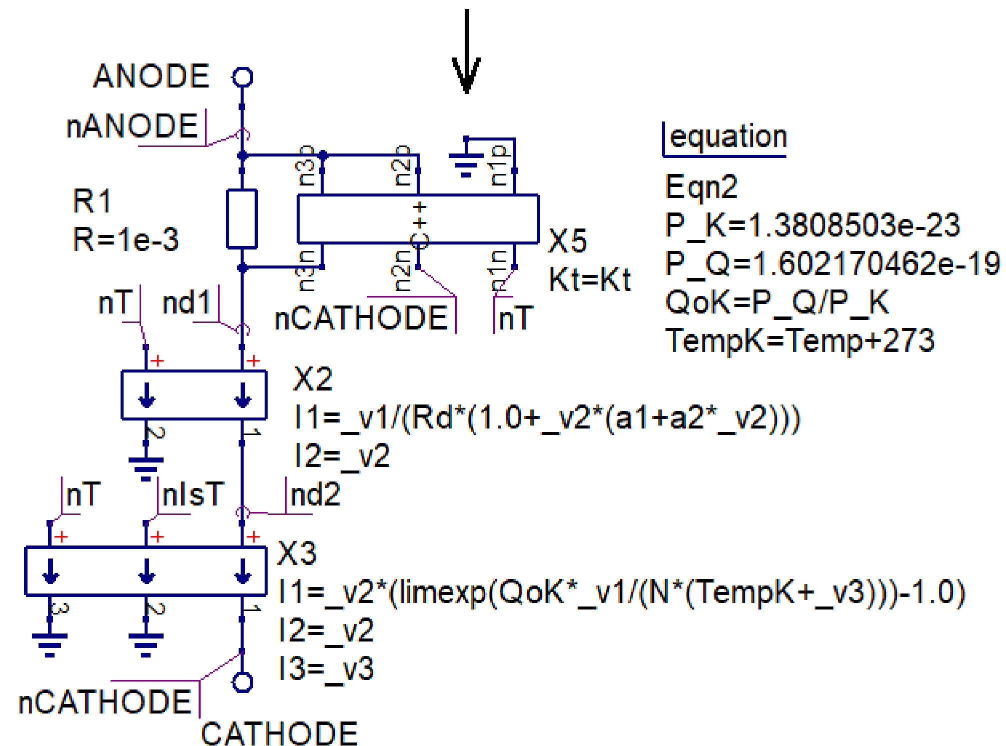
The Verilog-A module code for the two replaced EDD are given in the inserts shown in slides 9 and 10 (here EDD:D3 becomes VAEDD:X5 and EDD:D4 becomes VAEDD:X1).

These are very similar in structure varying only by the number of device pins and *In* entries.

Notice the use of the Verilog-A branch statement to simplify the module code. This is considered good practice and is recommended.

The compiled C++ VAEDD blocks can be easily generated using QucsStudio by simulating the EDD Verilog-A module code.

```
`include "disciplines.vams"
`include "constants.vams"
module VAEDD1(n3p, n3n, n2p, n2n, n1p, n1n);
inout n3p, n3n, n1p, n2p, n1n, n2n;
electrical n1p, n1n, n2p, n2n, n3p, n3n;
parameter real Kt = 6.4;
branch (n1p, n1n) B1;
branch (n2p, n2n) B2;
branch (n3p, n3n) B3;
analog begin
I(B1) <+ Kt*V(B3)*V(B2)*1e3;
end
endmodule
```



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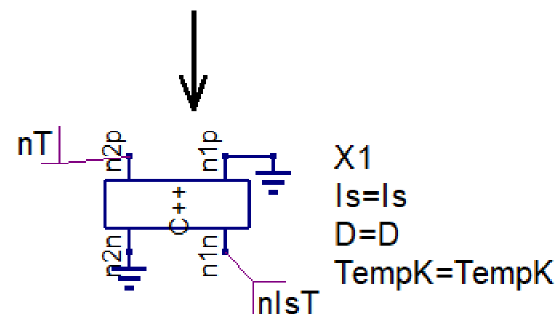
This process also links the compiled C++ module code to a software generated VAEDD symbol.

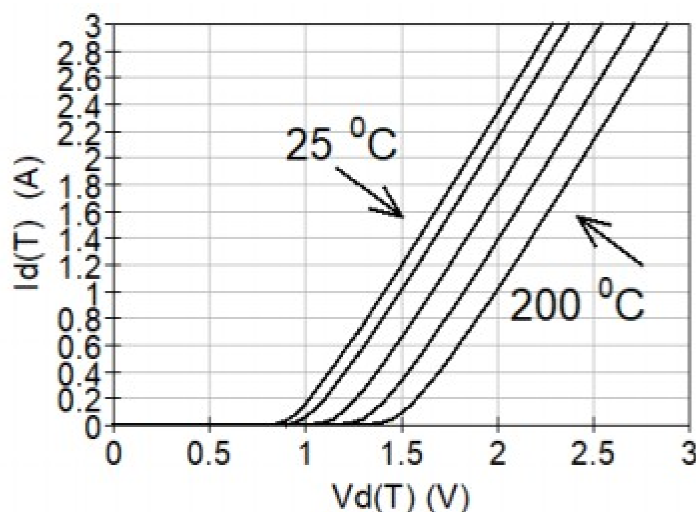
Passing higher level parameter values down the model hierarchy to VAEDD is done by equating parameter names to themselves in a VAEDD:Xn specification (for example *D=D* in VAEDD2).

The d.c. *Id/Vd* data given below is similar to the set on slide 7 Except that the have been generated with the VAEDD version of the SiC Schottky barrier diode model with parameter *Kt* set to 0.0 K/W.

The differences between the two sets of plotted data imply that there are measurable variations in the diode d.c. characteristics with and without thermal feedback.

```
`include "disciplines.vams"
`include "constants.vams"
module VAEDD2(n2p, n2n, n1p, n1n);
inout n1p, n2p, n1n, n2n;
electrical n1p, n1n, n2p, n2n;
parameter real Is = 3e-15;
parameter  real D = 2.95;
parameter real TempK = 300.0;
branch (n1p, n1n) B1;
branch (n2p, n2n) B2;
analog begin
I(B1) <+ Is*(pow(1.0+V(B2)/TempK, D));
I(B2) <+ V(B2);
end
endmodule
```





Zero recovery SiC CSD01060 forward characteristics with parameter *kt* set at 0.0 K/W

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FOSS Compact Model Pototyping with Verilog-A Equation-Defined Devices (VAEDD): Adding Dynamic Charge Properties to the SiC Schottky Barrier Diode Model with VAEDD

$$Cdep = \frac{dQ_{dep}}{dVd(T)} = Area \cdot Cj0 \cdot \left(1.0 - \frac{Vd(T)}{Vj}\right)^{-M}$$

For the operating voltage range *Vd(T) < Fc·Vj* let the diode stored charge *Qdep1* equal

$$\begin{aligned} Qdep1 &= Cd \cdot \int_0^{Vd(T)} \left(1.0 - \frac{V}{Vj}\right)^{-M} dV \\ &= \frac{Cd \cdot Vj}{1-M} \cdot \left[1.0 - \left(1.0 - \frac{Vd(T)}{Vj}\right)^{1-M}\right] \end{aligned}$$

Similarly, for the voltage operating range *Vd(T) >= Fc · Vj*
let the diode stored charge *Qdep2* equal

$$\begin{aligned} Qdep2 &= Cd \cdot \left[F1 + \frac{1}{F2} \int_{Fc \cdot Vj}^{Vd(T)} \left(F3 + \frac{M \cdot V}{Vj}\right) dV\right] \\ &= Cd \left[F1 + \frac{1}{F2} \cdot Z1\right] \end{aligned}$$

Where :

$$\begin{aligned} Cd &= Area \cdot CJ0 \\ Z1 &= (F3 \cdot (Vd(T) - Fc \cdot Vj) + F4 \cdot Z0) \\ Z0 &= (Vd(T) \cdot Vd(T) - F5 \cdot F5) \\ F1 &= \frac{Vj}{1-M} \cdot \left[1.0 - (1 - Fc)^{1-M)}\right) \\ F2 &= (1 - Fc)^{1-M} \\ F3 &= 1 - Fc \cdot (1 + M)) \\ F4 &= \frac{M}{2 \cdot Vj} \\ F5 &= Fc \cdot Vj \end{aligned}$$

M is a grading coefficient, *CJ0* is the zero d.c. bias diode depletion capacitance, *Vj* is the junction potential And *Area* is the relative device area.

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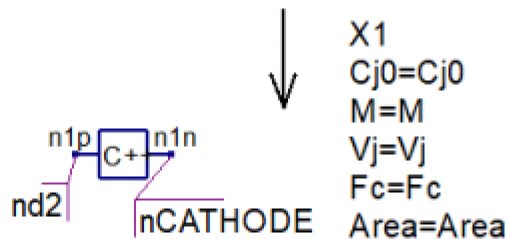
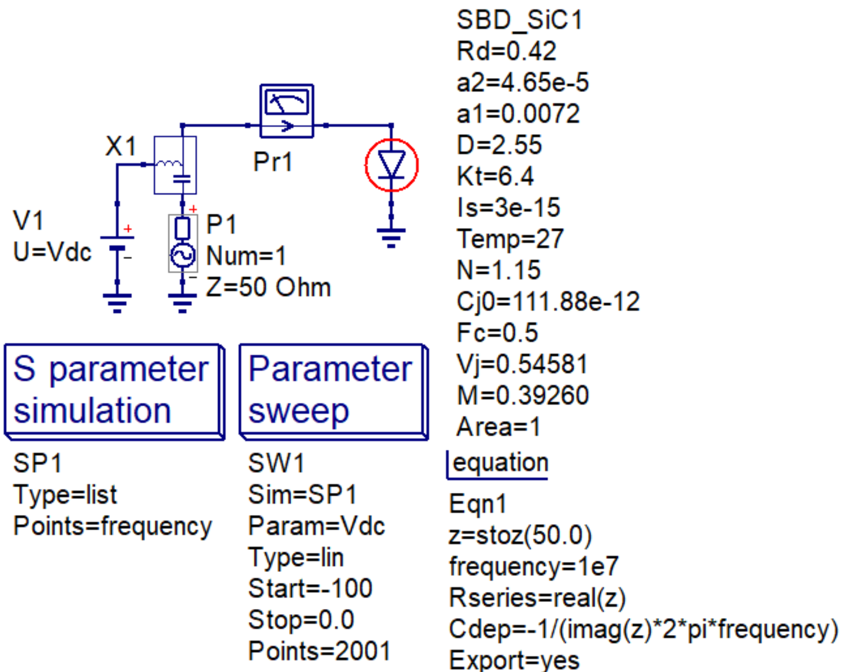
FOSS Compact Model Prototyping with Verilog-A Equation-Defined Devices (VAEDD): Adding Dynamic Charge Properties to the SiC Schottky Barrier Diode Model with VAEDD, part 2

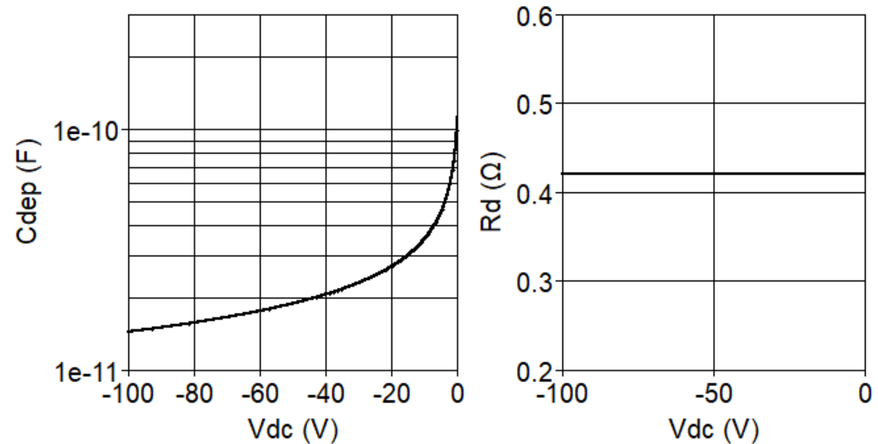
```
`include "disciplines.vams"
`include "constants.vams"
module VAEDD4(n1p, n1n);
inout n1p, n1n;
electrical n1p, n1n;
parameter real Cj0=111.88e-12;
parameter real M=0.39264;
parameter real Vj=0.54581;
parameter real Fc=0.5;
parameter real Area=1.0;
real F1, F2, F3;
branch (n1p, n1n) B1;
analog begin
@(initial_model)
begin
F1=(Vj/(1-M))*(1-pow(1-Fc,(1-M)));
F2=pow(1-Fc,(1+M));
F3=1-Fc*(1+M);
end
if (V(B1)<Fc*Vj)
 begin
  I(B1)<+ddt((Area*Cj0*Vj/(1-M))*(1-pow(1-V(B1)/Vj,
       (1-M))));
 end
else
 begin
  I(B1)<+ddt(Area*Cj0*F1+(Area*Cj0/F2)*(F3*(V(B1)-Fc*Vj)+
           (M/(2*Vj))*(V(B1)*V(B1)-Fc*Fc*Vj*Vj)));
 end
end
endmodule
```



SiC Schottky diode depletion capacitance modelled
by a two terminalVAEDD: pins labelled *nd2 (n1p)* and *nCATHODE (n1n)* connect to the same named pins in slides 9 and 10. The Cdep(T) VAEDD evaluates diode depletion capacitance at different d.c. voltage bias values and temperature
T = TempK.

FOSS Compact Model Prototyping with Verilog-A Equation-Defined Devices (VAEDD): Adding Dynamic Charge Properties to the SiC Schottky Barrier Diode Model with VAEDD, part 3





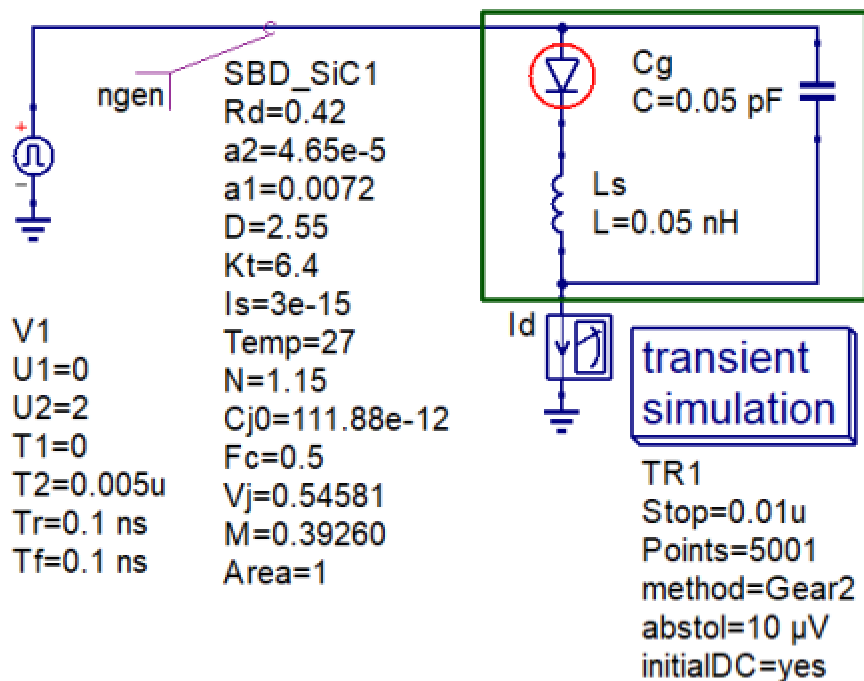
S parameter test bench for extracting SiC Schottky barrier diode parameters from small signal a.c. simulation.

The S parameter test bench shown above is capable of determining *S[1, 1]* from simulation and zero recovery SiC CSD01060 diode forward characteristics with parameter *kt* set at 0.0 K/W; extracting diode equivalent circuit parameters *Rd* and *Cj0* at temperature *TempK* K.

The d.c. bias voltage V d.c. is swept over the range -100 V to 0 V in order to check the variation of Cdep and Rd. The -100V to 0V bias voltage range ensures that the SiC Schottky barrier diode is reverse biased and that its small signal a.c. equivalent circuit simplifies to an impedance, where $z = Rd - j/(2 \cdot pi \cdot frequency \cdot Cdep)$.

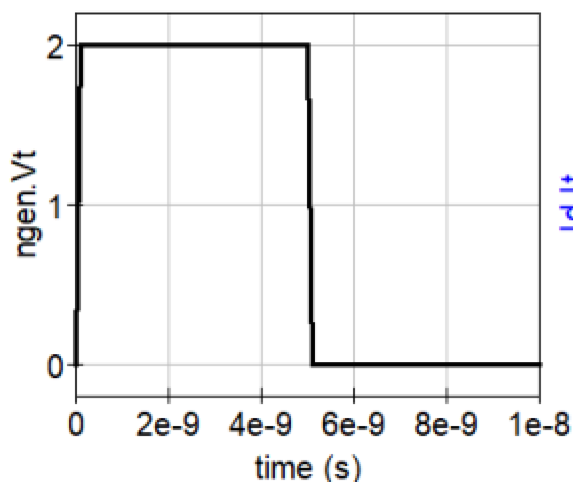
Hence, after converting *S[1, 1]* to impedance *z*, *Rd* can be found from *real(z)* and *Cdep* from expression $-1/(imag(z) \cdot 2 \cdot pi \cdot frequency)$.

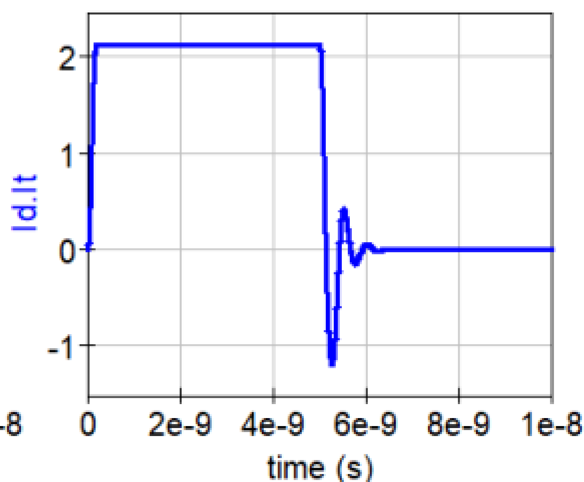
FOSS Compact Model Prototyping with Verilog-A Equation-Defined Devices (VAEDD): Simulation of a SiC Schottky Barrier Diode Forward Recovery Time



In this test bench the SiC Schottky barrier diode, plus parasitic components *Ls* and *Cg* is turned from an ON state (2 A d.c forward bias) to an OFF state (0 V d.c bias) in a fraction of a nano second.

With the device transit time set at zero Seconds the observed diode recovery time should also approach zero seconds, being determined by the residual charge stored by *Cdep*. With *Cdep* ≈ 100pF and *Rd* ≈ 0.4 Ω the turn-off time constant is roughly 40 ps, confirming the order of magnitude suggested by th *Id.It* versus *time*(s) curve.





SiC Schottky barrier diode test bench for estimating zero forward recovery time from simulation data: the Schottky barrier diode is modelled with the compact model introduced in previous slides.

FOSS Compact Model Prototyping with Verilog-A Equation-Defined Devices (VAEDD): Summary

- It is slightly over ten years since the EDD was introduce into the compact modelling repertoire. Although the EDD has been a very successful new modelling component, being widely used as a straightforward non-linear interactive prototyping element, it is characterised by slow simulation speed when compared to compiled C++ compact device models.

- This paper introduces a new extension to the EDD called a VAEDD that largely overcomes the EDD speed limitations.

- The VAEDD extension has an identical structure to the EDD but replaces its internal interpreted code with a Verilog-A module synthesized to C++, compiled and dynamically linked to the main body of circuit simulation code.

- In most respects a VAEDD can be considered to be a very small Verilog-A compact model that is built around the EDD pin layout and a prescribed internal code template.

- By adopting this arrangement for the VAEDD extension to the EDD it becomes possible to develop a new compact device model using EDD, and indeed other simulation components, then to replace one or more EDD with an equivalent number of VAEDD if Better overall model performance is required.

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