

# An outline of Qucs-S compact device modelling: History and capabilities: Part 2 XSPICE Code Models; basic properties to model synthesis, and beyond

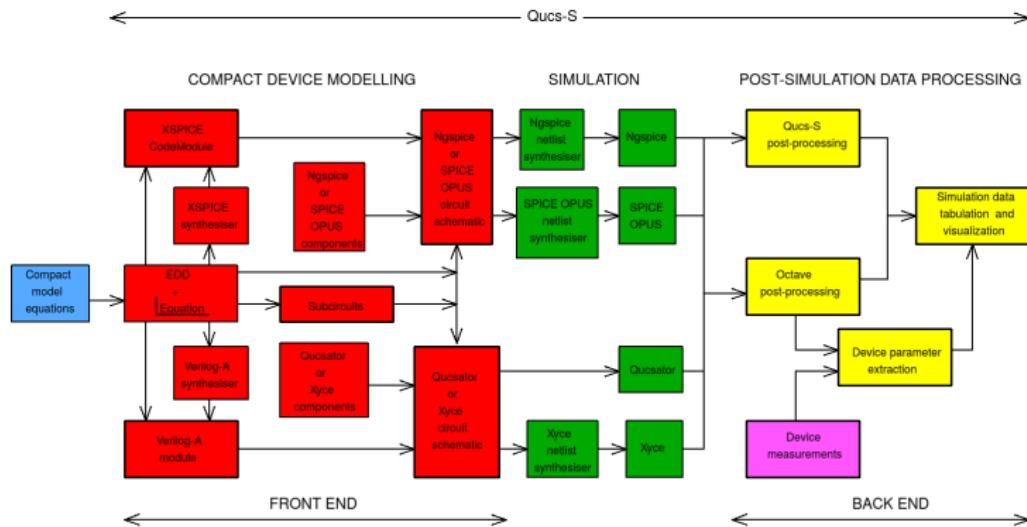
Mike Brinson<sup>1</sup>, [mbrin72043@yahoo.co.uk](mailto:mbrin72043@yahoo.co.uk).  
Vadim Kuznetsov<sup>2</sup>, [ra3xdh@gmail.com](mailto:ra3xdh@gmail.com)

<sup>1</sup>Centre for Communications Technology, London Metropolitan University,  
UK

<sup>2</sup>Bauman Moscow Technical University, Russia



# A flow chart showing Qucs-S compact modelling facilities and data movement

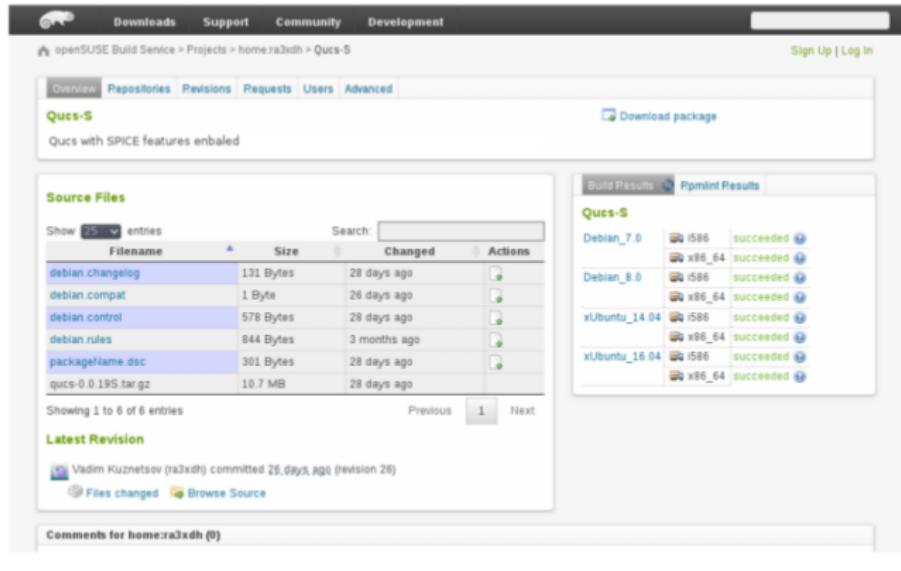


## NOTES:

1. Qucs-S allows the selection of the simulation engine to use.
2. Available simulation components depends on the simulation engine chosen.
3. Users may select either Qucs-S or Octave post-processing of simulator data.

# Qucs-S binary packages

- Debian packages are available here:  
<http://download.opensuse.org/repositories/home:/ra3xdh/>
- Windows Installer: <https://github.com/ra3xdh/qucs/releases/download/0.0.19S/qucs-0.0.19S-setup.zip>



The screenshot shows the openSUSE Build Service project page for the Qucs-S package. The top navigation bar includes links for Downloads, Support, Community, and Development. The main content area shows the project's status and build results.

**Project Status:** Qucs-S (Qucs with SPICE features enabled)

**Source Files:**

Filename	Size	Changed	Actions
debian.changelog	131 Bytes	28 days ago	<a href="#">View</a>
debian.compat	1 Byte	26 days ago	<a href="#">View</a>
debian.control	578 Bytes	28 days ago	<a href="#">View</a>
debian.rules	844 Bytes	3 months ago	<a href="#">View</a>
packageName.dsc	301 Bytes	28 days ago	<a href="#">View</a>
qucs-0.0.19S.tar.gz	10.7 MB	28 days ago	<a href="#">View</a>

Show 20 entries | Search:

**Build Results:**

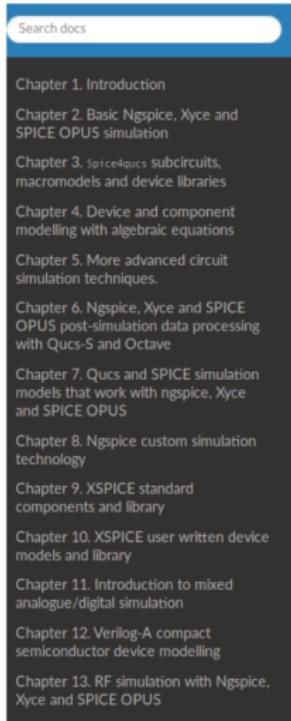
Variant	Architecture	Status
Debian_7.0	i586	succeeded
	x86_64	succeeded
Debian_8.0	i586	succeeded
	x86_64	succeeded
xUbuntu_14.04	i586	succeeded
	x86_64	succeeded
xUbuntu_16.04	i586	succeeded
	x86_64	succeeded

**Latest Revision:** Vadim Kuznetsov (ra3xdh) committed 26 days ago (revision 26)

[Files changed](#) [Browse Source](#)

**Comments for home:ra3xdh (0)**

# Qucs-S a maturing GPL software package: Qucs-S Help documentation



## Qucs-S Help documentation

### User Manual and Reference Material

Authors Mike Brinson ([mbrin72043@yahoo.co.uk](mailto:mbrin72043@yahoo.co.uk)) and Vadim Kusnetsov ([ra3xdh@gmail.com](mailto:ra3xdh@gmail.com))

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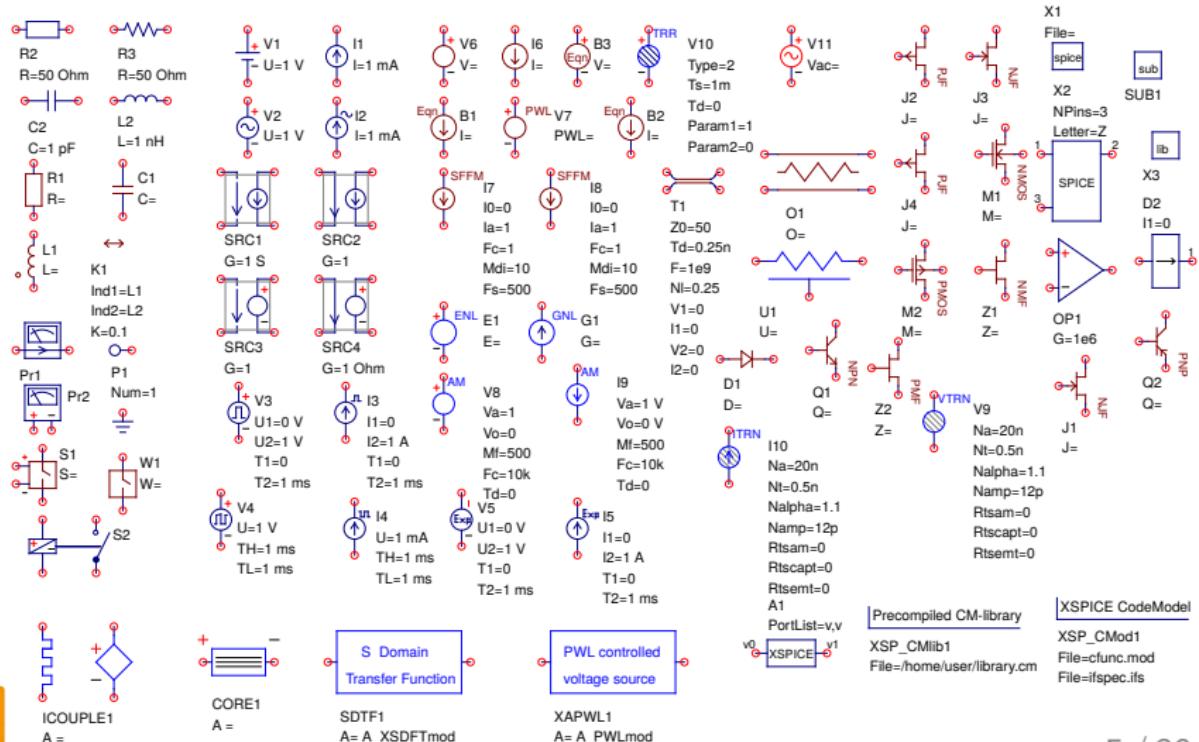
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#### Contents:

- [Chapter 1. Introduction](#)
- [Chapter 2. Basic Ngspice, Xyce and SPICE OPUS simulation](#)
- [Chapter 3. Spice4qucs subcircuits, macromodels and device libraries](#)
- [Chapter 4. Device and component modelling with algebraic equations](#)
- [Chapter 5. More advanced circuit simulation techniques](#).
- [Chapter 6. Ngspice, Xyce and SPICE OPUS post-simulation data processing with Qucs-S and Octave](#)



# Qucs-S a maturing GPL software package: Ngspice, Xyce and SPICEOPUS built in components



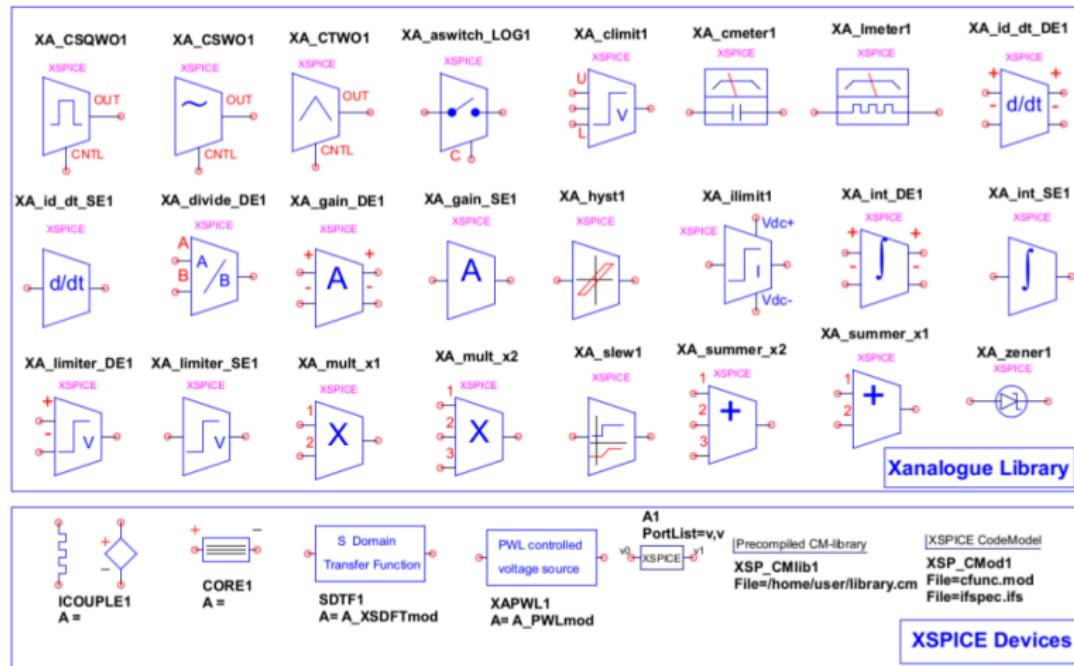
# Qucs-S a maturing GPL software package: Available semiconductor device models

Type	Description	Level	Ngspice	Xycce	SPICEOPUS
D	Legacy	1	X	X	X
		2		X	
		3			X
BJT	Legacy VBIC FBH HBI_X MEXTRAM	1	X	X	X
		10,11,12		X	
		23		X	
		504,505			X
JFET		1	X	X	X
		2	X	X	X
MESFET	1 (Statz) 2 (Ytterdel)	X		X	X
		X			
MOSFET Legacy	1 2 3 4(BSIM1) 5(BSIM2) 6 47 8 9	X		X	X
		X		X	X
		X		X	X
		X		X	X
		X		X	X
		X		X	X
		X		X	X
		X		X	X
		X		X	X
		X		X	X
BSIM3v2	53				
		X			
BSIM3v3	49				
		X			
BSIM4	60 14 54				
		X		X	X
BSIM3SOIv1	55				
		X			X
BSIMOIV2	56 58,55,57				
		X		X	X
STAGSOI3	10 57				
		X		X	X
UFSOI	58				X
SOI3	60	X			
UFET	7				X
EKVv2p6	44	X			
HISIM2	61,68	X			
HISIM_HV	62,63	X			
VDMOS	18				
BSIM 6p1	77			X	
PSP 103p1	103			X	

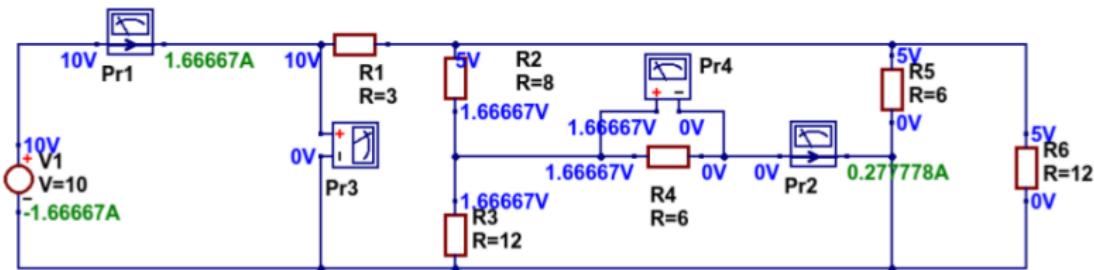
# Qucs-S a maturing GPL software package: Simulation control icons

<b>dc simulation</b>	<b>Fourier simulation</b>	<b>XYCE script</b>	<b>.NODESET</b>	<b>.GLOBAL PARAM</b>	<b>.OPTIONS</b>	<b>.IC</b>
DC1	FOUR1 Sim=TR1 numfreq=10 F0=1kHz Vars=V(1)	XYCESCR1 SpiceCode= .AC LIN 2000 100 10MEG .PRINT AC format=raw file=ac.txt V(1)	Nodeset1 v(node1)=1	SpGlobPar1 y=1	SpiceOptions1 GMIN=1e-12	SpiceC1 v(node1)=1
<b>transient simulation</b>	<b>Distortion simulation</b>	<b>Nutmeg script</b>	<b>Equation</b>	<b>.PARAM</b>	<b>Parameter sweep</b>	<b>Noise simulation</b>
TR1 Type=lin Start=0 Stop=1 ms	DISTO1 Type=lin Start=1 Hz Stop=10 kHz Points=100	Nutmeg NutmegEq1 Simulation=ac y=1	Eqn1 y=1	SpicePar1 y=1	SW1 Sim= Type=lin Param=R1 Start=5 Ohm Stop=50 Ohm Points=20	NOISE1 Type=lin Start=1 Hz Stop=10 kHz Points=100 Output=v(node1) Source=V1
<b>ac simulation</b>	<b>Pole-Zero simulation</b>	<b>INCLUDE</b>		<b>.MODEL</b>		
AC1 Type=lin Start=1 GHz Stop=10 GHz Points=19	PZ1 Input=in 0 Output=out 0 TF_type=vol PZ_mode=pz	SpiceInclude1 File=~/home/user/library.inc		SpiceModel1 Line_1 =.MODEL DIODE1 D(BF=50 Is=1e-13 Vbf = 50)		
<b>Harmonic balance simulation</b>						
HB1 n=4	CUSTOM1 SpiceCode= .AC LIN 2000 100 10MEG let K=V(1)/V(2)					

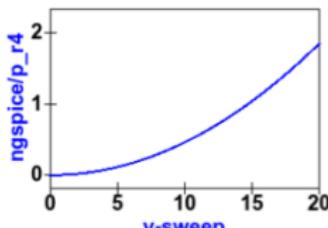
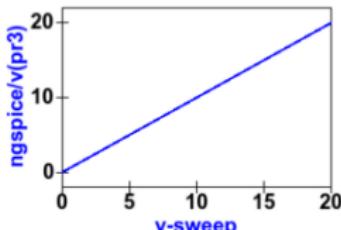
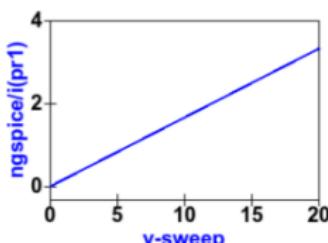
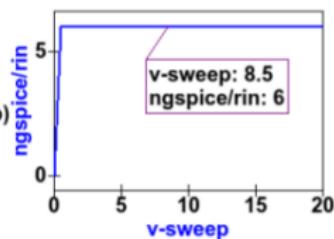
# Qucs-S a maturing GPL software package: XSPICE analogue component models



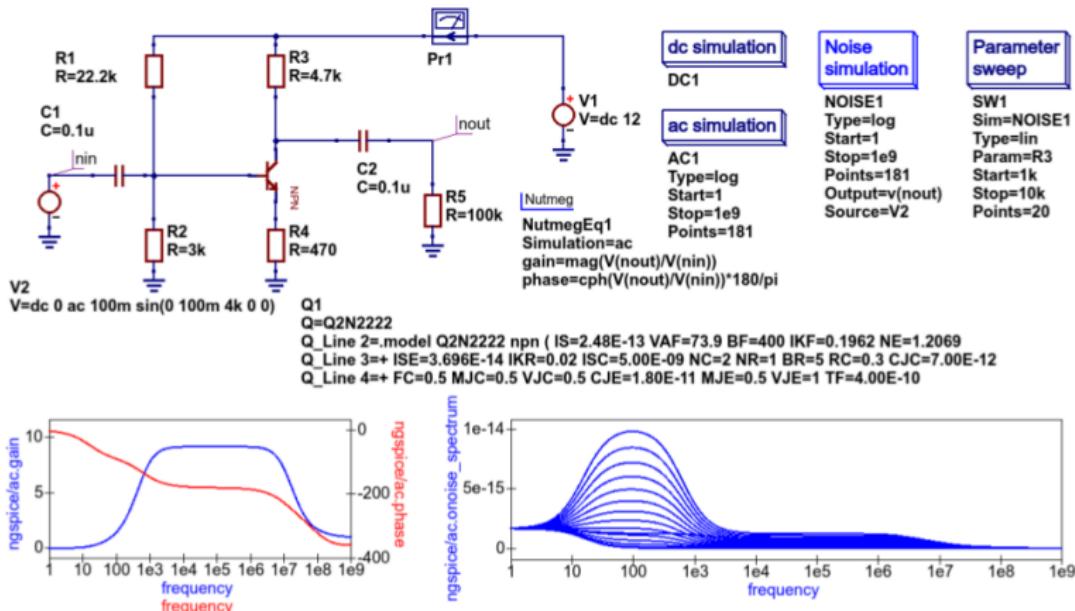
# Qucs-S a maturing GPL software package: Qucs-S extended circuit simulation Part 1. SPICE .OP to visual DC by pressing key F8



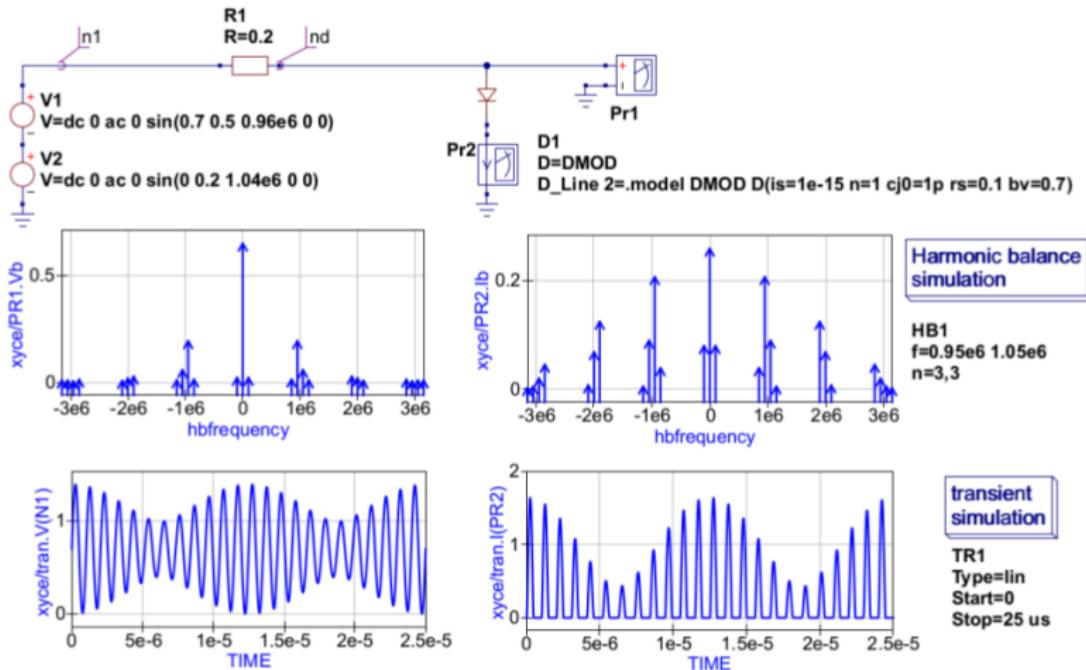
Nutmeg  
NutmegEq1  
Simulation=dc  
Rin=V(pr3) / ( vpr1#branch +1p)  
P\_R4=V(pr4) \* vpr2#branch



# Qucs-S a maturing GPL software package: Qucs-S extended circuit simulation Part 2. Noise spectral response



# Qucs-S a maturing GPL software package: Qucs-S extended circuit simulation Part 3. Multi-tone Harmonic balance analysis



# Qucs-S a maturing GPL software package: Qucs-S extended circuit simulation Part 4. Direct support for SPICE libraries

The screenshot shows the Qucs-S software interface. On the left, a 'Manage Libraries' window is open, displaying a list of available libraries under the 'Libraries' tab. The 'ad822' library is selected and highlighted in grey. The list includes categories like System Libraries, AnalogueCM, Bridges, Cores, Diodes, Ideal, JFETs, LEDs, MOSFETs, NMOSFETs, OpAmps, PMOSFETs, Regulators, Transformers, Transistors, Varistors, Xanalogue, Z-Diodes, User Libraries, and the selected ad822 library. The main workspace on the right shows a schematic diagram of a circuit. A callout arrow points from the 'ad822' library entry in the library manager to the device symbol in the schematic. The schematic includes various components like resistors (R1=10k, R2=10k), capacitors (C1=0.001uF, C2=0.001uF), voltage sources (V1=1V, V2=1V, V3=1V, V4=1V), and a dependent current source (ib). The circuit is labeled X1, File=ad822.cir, Device=AD822, SymPattern=opampSt. Below it is another part labeled X2, File=ad822.cir, Device=AD822, SymPattern=opampSt. A red text box in the center states: "Qucs-S now includes direct support for SPICE libraries".

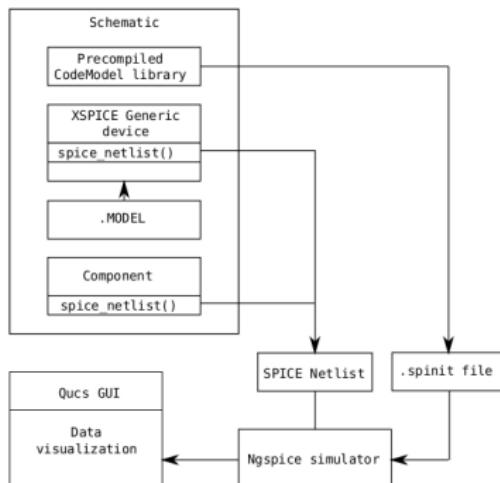
## Qucs-S a maturing GPL software package: Modelling tool additions and new features

- Qucs-S includes for the first time a turn-key XSPICE "code level modelling" package for use with the Ngspice and SPICE OPUS circuit simulators,
- Qucs-S has also been extended to include a new Qucs/Octave integrated tool set for compact device model and circuit macromodel parameter extraction. The technique employed is based on data fitting and optimization using measured, or manufacturers published device data, compared against simulated circuit data.



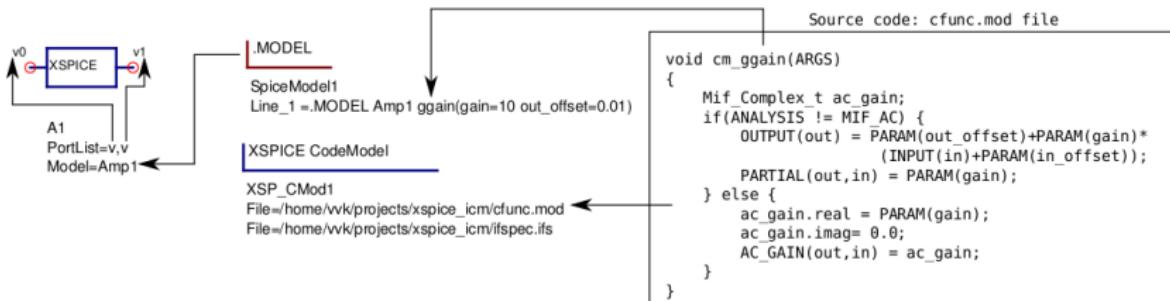
# Qucs-S a maturing GPL software package: XSPICE Code Model support subsystem

- The XSPICE generic device component is the foundation for
  - Precompiled XSPICE device (\*.cm) library support, and
  - Dynamic XSPICE "Code Model" compilation system which allows Code Model sources to be attached to a schematic and compiled automatically at simulation time.

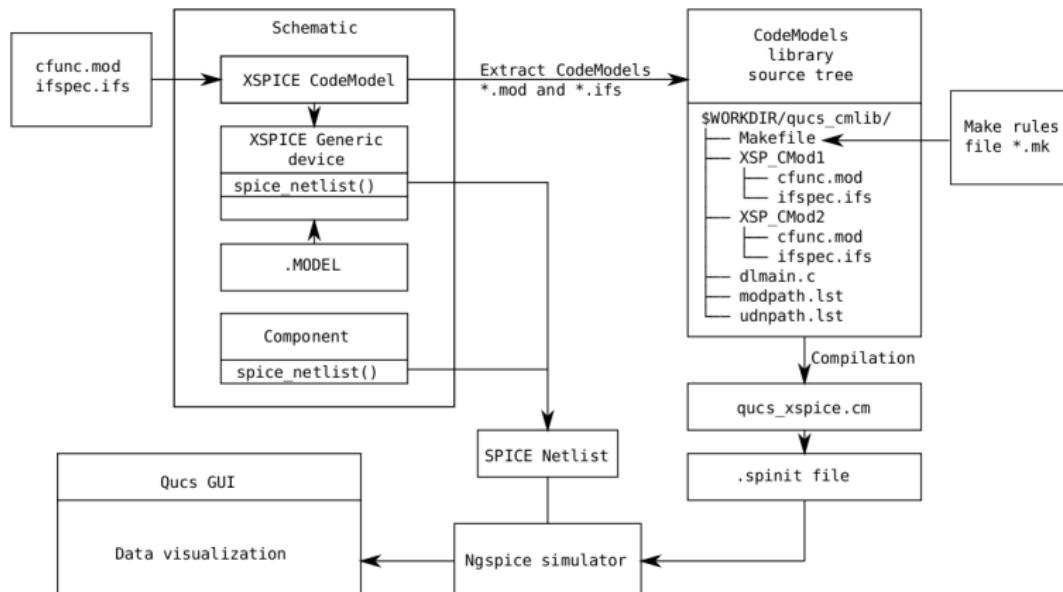


# Qucs-S a maturing GPL software package: XSPICE Turn-Key Model Generation; compiler system building blocks

- The XSPICE generic device component is a building block for the construction of user-defined A-devices. It is defined by a comma separated port list, plus XSPICE port designators. These are attached to a SPICE .MODEL statement



# Qucs-S a maturing GPL software package: XSPICE Turn-Key Model Generation; compiler system dataflow diagram

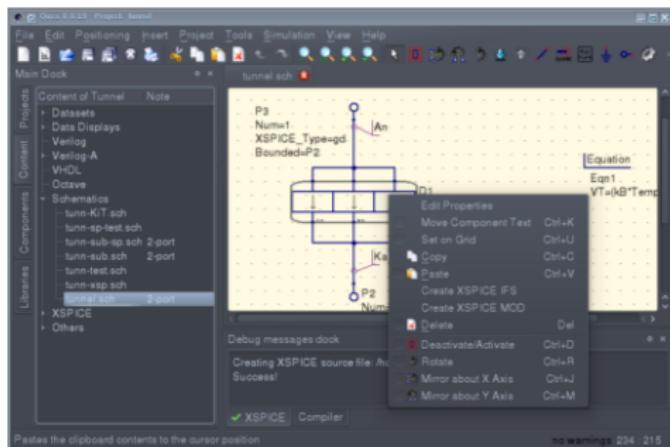


# Main features of the XSPICE CodeModel synthesizer

## Main features:

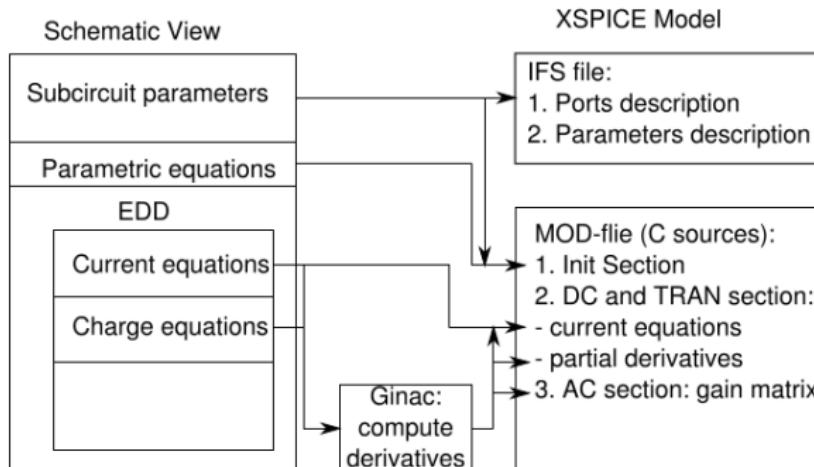
- Synthesize XSPICE C-code and interface description from EDD schematic view;
- Access to code synthesizer from right-click on the EDD component;
- Synthesizer generates a pair of MOD and IFS files from a single EDD;
- Automatic recognition of model parameters and dependent variables;
- Automatic symbolic computation of partial derivatives and AC gain matrix using Ginac embedded CAS library;

## • XSPICE synthesizer context menu



# The structure of the XSPICE model synthesizer

- Giac <http://www.ginac.de/> library is used for symbolic computation of partial derivatives and AC gain matrix;
- Interface description file (\*.IFS) is generated from subcircuit symbol or from the EDD and attached equations;
- Model description (C-code \*.MOD) is generated from individual EDDs;



# Tunnel diode XSPICE model

**Schematic view**

**XSPICE sources**

```

/* XSPICE codemodel tunnel auto-generated template */

#include <math.h>
#include "xspice_mathfunc.h"

void cm_tunnel(ARGs)
{
    Complex_t ac_gain00;
    static double Is,Iv,Ip,Vp,C,Temp0;
    static double VT;
    static double V1,V1_old;
    double Q0, cQ0, double delta_t;

    if(INIT) {
        Is = PARAM(is); Iv = PARAM(iv);
        K1 = PARAM(k1); Vv = PARAM(vv);
        Ip = PARAM(ip); Vp = PARAM(vp); C = PARAM(c);
        Temp0 = PARAM(temp0);
        VT=8.6173402243760290e-05*Temp0;
    }
    if (ANALYSIS != AC) {
        if (TIME == 0) {
            V1_old = V1 = INPUT(An_Ka);
            Q0=0.0; cQ0=0.0;
        } else {
            V1 = INPUT(An_Ka);
            delta_t=TIME-T(i);
            Q0 = (C)*(V1-V1_old)/(delta_t+1e-20);
            cQ0 = (C)/(delta_t+1e-20);
            V1_old = V1;
        }
        OUTPUT(An_Ka) = Is*( exp(1.0/VT*V1)-1.0+
            exp(-Iv*V1*K1)*Iv*exp((Vp-V1)/Vp)*Ip/Vp*V1 + Q0;
        PARTIAL(An_Ka,An_Ka) = Ip*exp(1.0/Vp*(Vp-V1))/Vp+
            1.0/VT*exp(V1/VT)*Is-Ip*exp(1.0/Vp*(Vp-V1))/(Vp*Vp)*V1+
            Iv*K1*exp((V1-Vv)*K1) + cQ0;
    } else {
        ac_gain00.real = Ip*exp(1.0/Vp*(Vp-V1))/Vp+
            1.0/VT*exp(V1/VT)*Is-Ip*exp(1.0/Vp*(Vp-V1))/(Vp*Vp)*V1+
            Iv*K1*exp((V1-Vv)*K1);
        ac_gain00.imag = (C)*RAD_FREQ;
        AC_GAIN(An_Ka,An_Ka) = ac_gain00;
    }
}

```

## Two-port testbench model: vacuum triode

- Triode is one of the simplest possible compact models. Triode equations:

$$I_{grid} = 0 \quad (11)$$

$$I_{plate} = \frac{1}{K_g} \left( V_{grid} + \frac{V_{plate}}{\mu} \right)^{1.5} \quad (12)$$

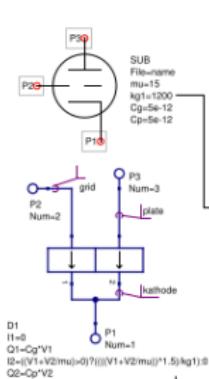
- Model parameters are:  $\mu$ ,  $K_g$ ,  $C_{grid}$ , and  $C_{plate}$ ;
- Additional equations are required to implement XSPICE model (two partial derivatives and AC gain matrix):

$$g_{plate} = \frac{\partial I_{plate}}{\partial V_{plate}} = \frac{1.5}{\mu K_g} \sqrt{\frac{V_{plate}}{\mu} + V_{grid}} \quad (13)$$

$$g_{p.k.} = \frac{\partial I_{plate}}{\partial V_{grid}} = \frac{1.5}{K_g} \sqrt{\frac{V_{plate}}{\mu} + V_{grid}} \quad (14)$$

$$(G_{AC}) = \begin{pmatrix} j\omega C_g & g_{p.k.} \\ 0 & g_{plate} + j\omega C_{plate} \end{pmatrix} \quad (15)$$

# Triode EDD implementation and auto-generated XSPICE Code



```

/* XSPICE codemodel triodi auto-generated template */

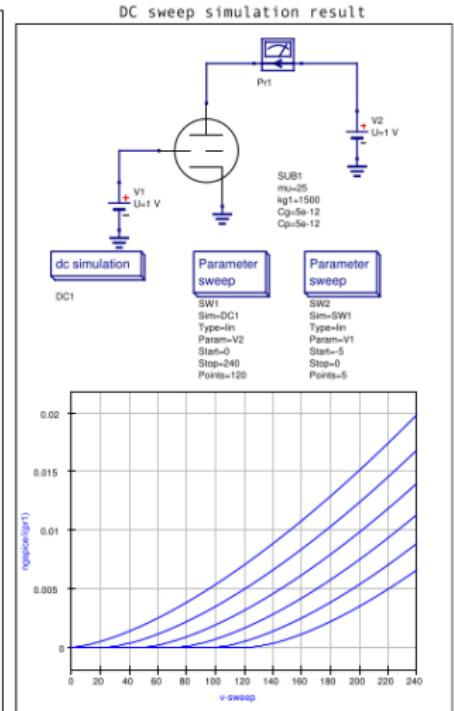
#include <math.h>
#include "xspice_mathfunc.h"

void cm_triodi(ARGS)
{
    Complex_t ac_gain00, ac_gain01, ac_gain10, ac_gain11;
    static double Cg, mu, kg1, Cp, V1, V2, V1_old, V2_old;
    double Q0, cQ0, Q1, cQ1; double delta_t;

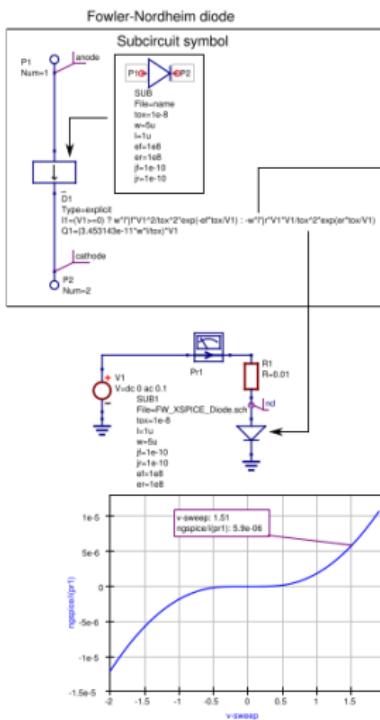
    if (INIT) {
        Cg = PARAM(cg); mu = PARAM(mu); kg1 = PARAM(kg1); Cp = PARAM(cp);
    }

    if (ANALYSIS != AC) {
        if (TIME == 0) {
            V1_old = V1 = INPUT(grid_kathode); V2_old = V2 = INPUT(plate_kathode);
            Q0 = 0.0; cQ0 = 0.0; Q1 = 0.0; cQ1 = 0.0;
        } else {
            V1 = INPUT(grid_kathode); V2 = INPUT(plate_kathode);
            delta_t = TIME - T1;
            Q0 = (Cg * (V1 - V1_old)) / (delta_t + 1e-20);
            cQ0 = (Cg) / (delta_t + 1e-20);
            Q1 = ((Cp * (V2 - V2_old)) / (delta_t + 1e-20));
            cQ1 = (Cp) / (delta_t + 1e-20);
            V1_old = V1; V2_old = V2;
        }
        OUTPUT(grid_kathode) = 0.0 + Q0;
        OUTPUT(plate_kathode) = ((V1 + V2 / mu) ? pow(V1 + V2 / mu, 1.5) : kg1 * 0.0 + Q1);
        PARTIAL(grid_kathode.grid_kathode) = 0.0 + cQ0;
        PARTIAL(grid_kathode.plate_kathode) = 0.0;
        PARTIAL(plate_kathode.grid_kathode) =
            ((V1 + V2 / mu) ? 71.59 * xpow(V1 + V2 / mu, 0.5) : kg1 * 0.0);
        PARTIAL(plate_kathode.plate_kathode) =
            ((V1 + V2 / mu) ? 71.59 * xpow(V2 / mu * V1, 0.5) : mu / kg1 * 0.0 + cQ1);
    } else {
        ac_gain00.real = 0.0;
        ac_gain00.imag = (Cg) * RAD_FREQ;
        AC_GAIN(grid_kathode.grid_kathode) = ac_gain00;
        ac_gain01.real = 0.0; ac_gain01.imag = 0.0;
        AC_GAIN(grid_kathode.plate_kathode) = ac_gain01;
        ac_gain10.real = ((V1 + V2 / mu) ? 71.59 * xpow(V1 + V2 / mu, 0.5) : kg1 * 0.0);
        ac_gain10.imag = 0.0;
        AC_GAIN(plate_kathode.grid_kathode) = ac_gain10;
        ac_gain11.real = ((V1 + V2 / mu) ? 71.59 * xpow(V2 / mu * V1, 0.5) : mu / kg1 * 0.0);
        ac_gain11.imag = (Cp) * RAD_FREQ;
        AC_GAIN(plate_kathode.plate_kathode) = ac_gain11;
    }
}

```



# Fowler-Nordheim diode model



**Auto-synthesized XSPICE code**

```

/* XSPICE codemodel fw_diode auto-generated template */

#include <math.h>

#define D_0_step(x)
#define step(x) ((x)>0.0?1.0:((x)==0)?0.5:0.0)

#define Xpow(x,p) pow(fabs(x),(p))

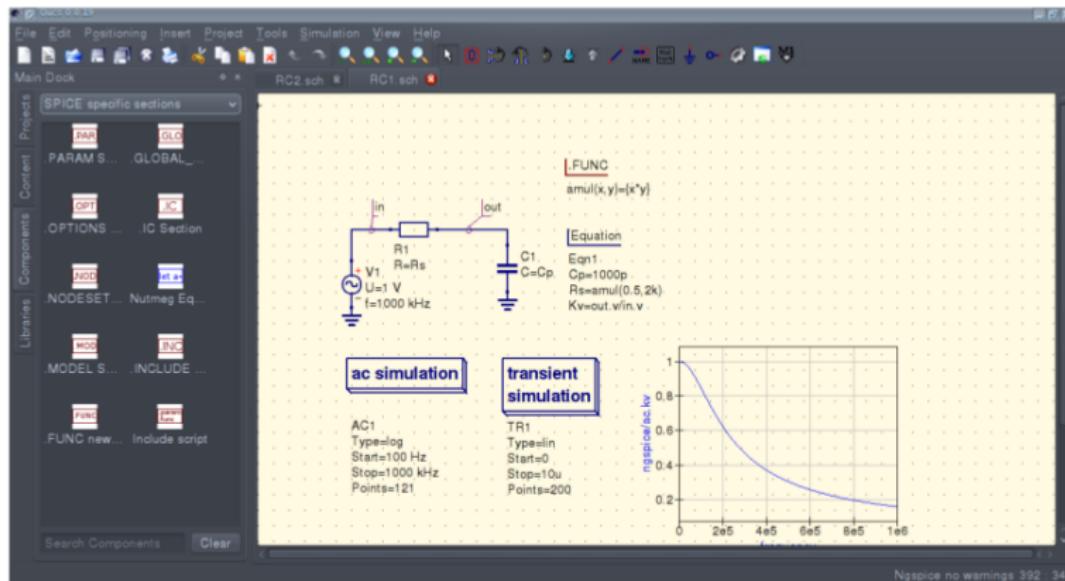
void cm_fw_diode(ARG5)
{
    Complex_t ac_gain0;
    static double w1,l,f,tox,ef,jr,er;
    static double V1,V1_old;
    double Q0, cQ0;
    double delta_t;

    if(INIT) {
        w = PARAM(w);
        l = PARAM(l);
        jf = PARAM(jf);
        tox = PARAM(tox);
        ef = PARAM(ef);
        jr = PARAM(jr);
        er = PARAM(er);
    }
    if (ANALYSIS != AC) {
        if (TIME == 0) {
            V1 = V1 = INPUT(anode_cathode);
            Q0=0.0;
            cQ0=0.0;
        } else {
            V1 = INPUT(anode_cathode);
            delta_t=TIME-T1;
            Q0 = (3.4531430000000001e-11/l/tox*w)*(V1-V1_old)/(delta_t+1e-20);
            cQ0 = (3.4531430000000001e-11/l/tox*w)/(delta_t+1e-20);
            V1_old = V1;
        }
        OUTPUT(anode_cathode) = (V1>0)?
            jf*(V1*V1)*exp(-ef*V1*tox)/(tox*tox)*:
            -jf*(exp(-V1*tox)*(V1*V1)*w/(tox*tox)*)+Q0;
        PARTIAL(anode_cathode,anode_cathode) = (V1>0)?
            2.*0.1.*theta(tox*tox)*l*exp(-tox*ef/V1)*jf*ef*w:
            -2.*0.1.*theta(tox*tox)*l*jf*V1*w*exp(tox*er/V1)+1.0/tox*l*jr*er*w*exp(tox*er/V1)+cQ0;
    } else {
        ac_gainm0.real = (V1>0)?
            2.*0.1.*theta(tox*tox)*l*exp(-tox*ef/V1)*jf*V1*w+1.0/tox*l*exp(-tox*ef/V1)*jf*ef*w:
            -2.*0.1.*theta(tox*tox)*l*jf*V1*w*exp(tox*er/V1)+1.0/tox*l*jr*er*w*exp(tox*er/V1);
        ac_gainm0.img = (3.4531430000000001e-11/l/tox*w)*RAD_FREQ;
        AC_GAIN(anode_cathode,anode_cathode) = ac_gain0;
    }
}

```

# Qucs-S : .FUNC entry: user-defined SPICE functions 1

- .FUNC pseudo-component is placed at the "SPICE specific section group"
- .FUNC entries prepend components description in the auto-generated netlist

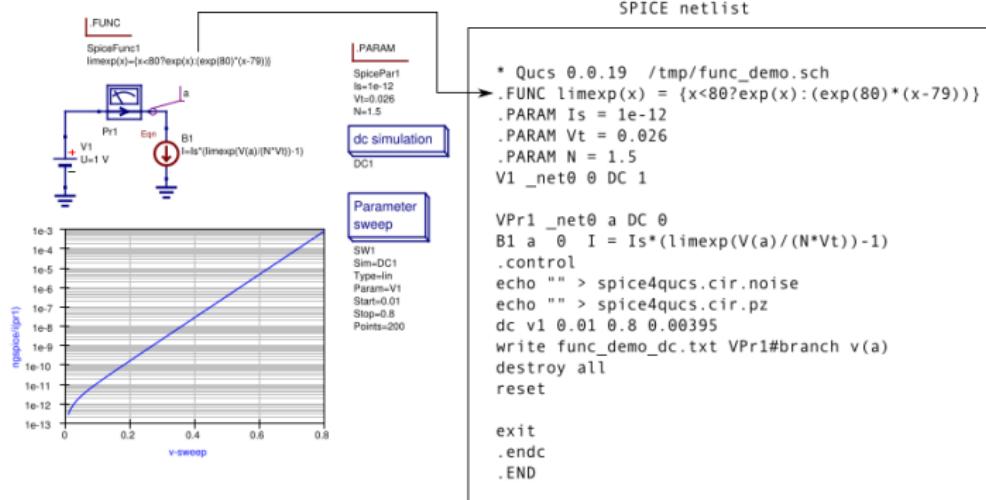


## Qucs-S : .FUNC entry: user-defined SPICE functions 2

- Diode model implementation with Ngspice and limexp() function:

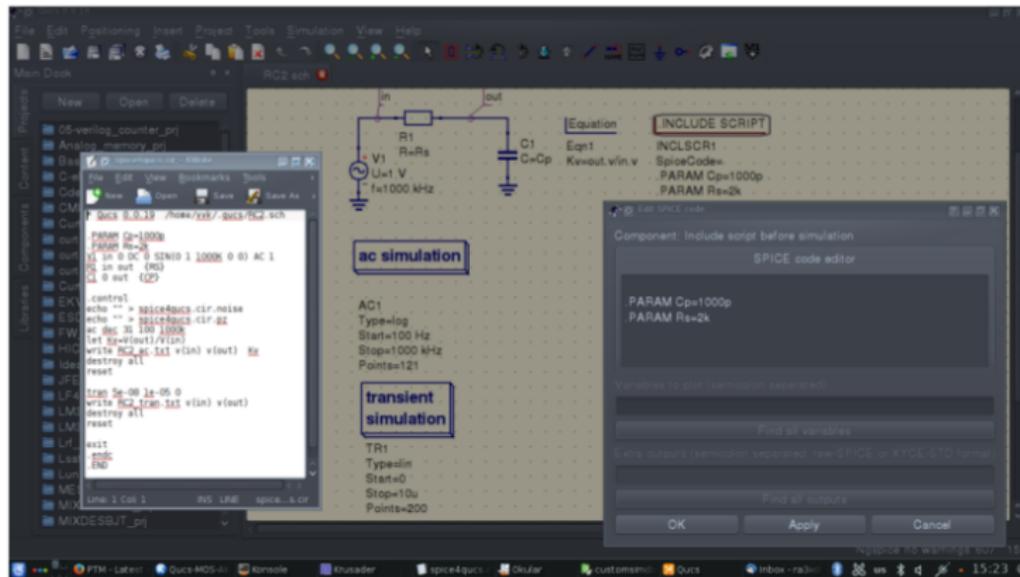
$$I = I_s \left( \exp \left( \frac{V}{N V_t} \right) - 1 \right)$$

- Schematic and auto-generated SPICE netlist:



# Include scripts: run some SPICE code before components initialized

- Include scripts allow to place some custom SPICE code (parameters, options, function definitions) before components initialization and edit this code manually.



# Post-simulation data processing : 1. using Qucs

Equation blocks + simulation data sets → Data processing → Tables and plots

**Constants:** i, j, pi, e, kB, q

**Immediate:** 2.5, 1.4+j5.1, [1, 3, 4, 5, 7], [11, 12; 21, 22]

**Ranges:** Lo:Hi, :Hi, Lo:, :

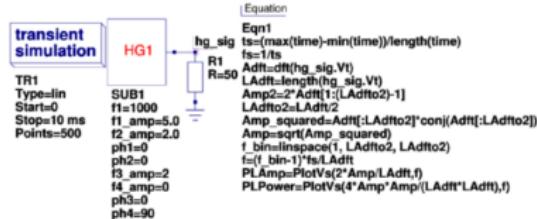
**Logical operators:** lx, x&&y, x||y, x^&y, x?y:z, x==y, x!=y, x<y, x<=y, x>y, x>=y

**Number suffixes:** E, P, T, G, M, k, m, u, n, p, f, a

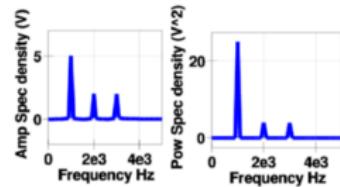
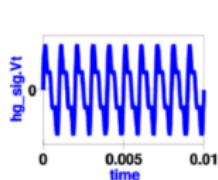
**Matrices:** M, M[2,3], M[:,3]

**Arithmetic operators:** +x, -x, x+y, x-y, x^y, x/y, x%y, x^y

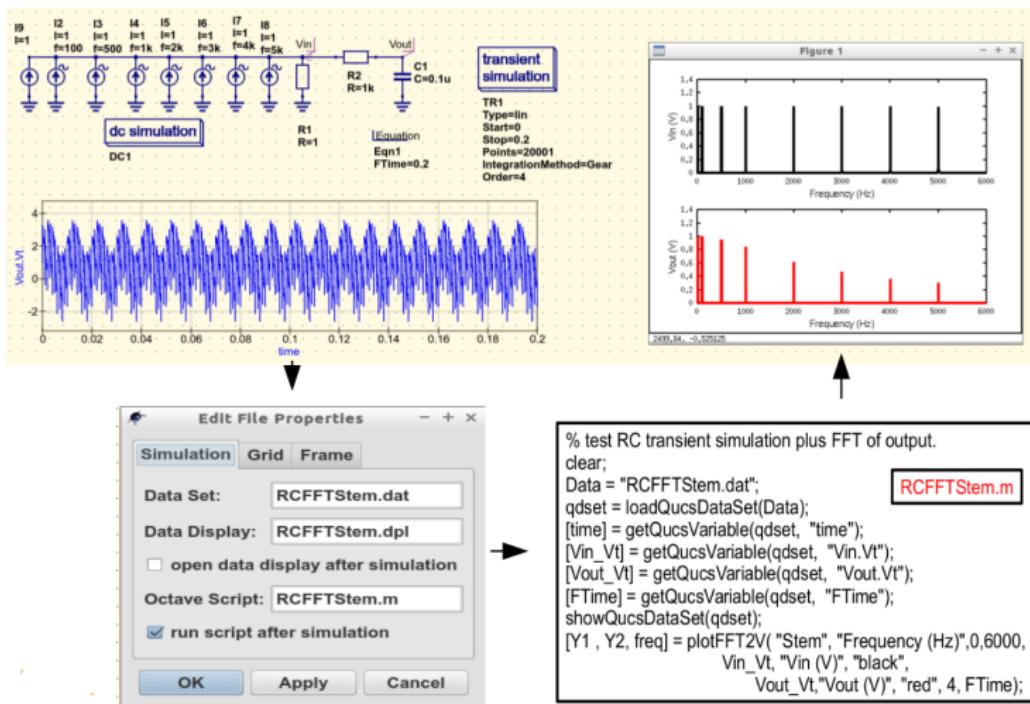
abs adjoint angle arccos arccosec arccot arcosh arcoth arcsin arsech arsinh artanh avg bessel0 besselj bessely conj cos cosec cosech cosh cot cumavg cumprod cumsum dB dbm dbm2w deg2rad det dft diff erf erfc erfcinv erfinv exp eye fft fix floor Freq2Time GaCircle GpCircle hypot idft ifft imag integrate interpolate inverse kbd limexp linspace ln log10 log2 logspace mag max min Mu Mu2 NoiseCircle norm phase PlotVs polar prod rad2deg random real rms Rollet round rtoiwr rtoiy rtoz runavg sec sech sign sin sinc sinh sqr sqrt srandom StabCircleL StabCircleS StabFactor StabMeasure stddev step stos stoy stoz sum tan tanh Time2Freq transpose twoport unwrap variance vt w2dbm xvalue ytor ytos ytoz yvalue ztor ztos ztoy



Limitations: NO user defined functions or control loops



## Post-simulation data processing : 2. using Octave



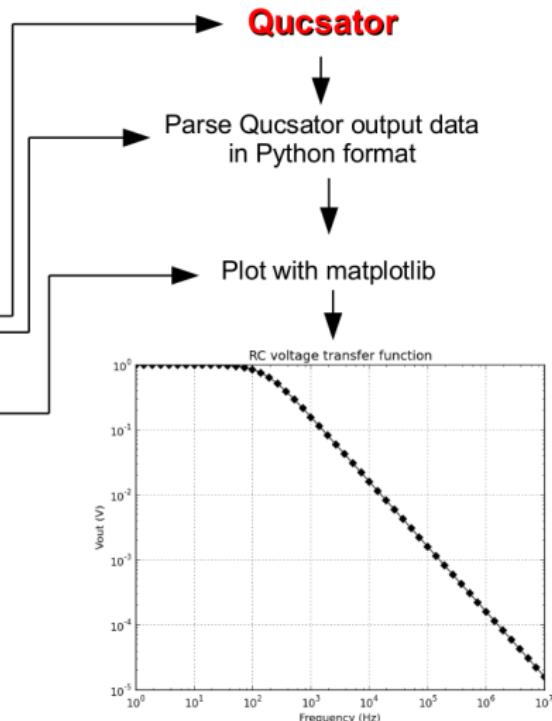
## Post-simulation data processing : 3. using Python

```
# Basic Python script to demonstrate Qucs simulation with Qucsator
#
import subprocess
import parse_result as pr
import numpy as np
import matplotlib.pyplot as plt
#
from string import Template
#
def runSim():
    netfile = open('RC.net', 'r')
    outfile = open('sim_result.dat', 'w')
    process = subprocess.Popen(['qucsator', stdin = netfile, stdout = outfile])
    process.wait()
    netfile.close()
    outfile.close()
#
# Undertake simulation and plot output results
#
runSim()
data = pr.parse_file('sim_result.dat')
x = data['acfreq']
y = np.abs(data['out.v'])
plt.loglog(x, y, 'kD')
plt.grid()
plt.title('RC voltage transfer function')
plt.xlabel('Frequency (Hz)')
plt.ylabel('Vout (V)')
plt.show()
```

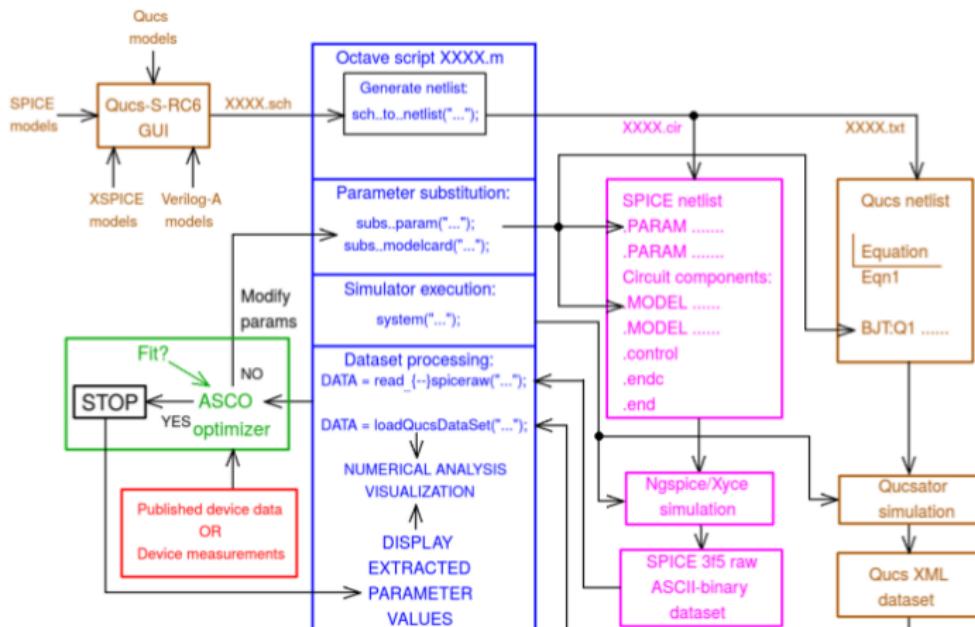
### Python script

```
# File RC.net
#
Vac:V1 in gnd U = "1V" f = "1 kHz"
R:R1 out in R = "1 k"
C:C1 out gnd C = "1 u"
.AC:AC1 Start = "1 Hz" Stop = "10 MHz" Points = "50" Type = "log"
```

### Qucs netlist



# Qucs-S/Ngspice/Xyce Circuit Analysis and Compact Device Parameter Extraction from Manufacturers Data or Measurements Controlled by Octave Script Files: Part I Structure Diagram



# Qucs-S/Ngspice/Xyce Circuit Analysis and Compact Device Parameter Extraction from Manufacturers Data or Measurements Controlled by Octave Script Files: Part II Octave Package

- The main purposes of Octave integration are:
  - Parameter substitution in Qucs and SPICE netlists,
  - Simulation process control from Octave,
  - Simulator output dataset (SPICE3f5-raw and Qucs XML) loading into Octave matrix structures,
  - Compact model parameter extraction from simulation and manufacturer's, or measured, data using curve fitting and optimization with the ASCO package.
- Example Octave package functions:
  - *subs\_spice\_netlist(FILE, PARAM, VALUE),*
  - *subs\_qucs\_netlist(FILE, PARAM, VALUE),*
  - *subs\_spice\_model\_netlist(FILE, MODEL, PARAM, VALUE),*
  - *DATA = read\_spiceraw(FILE).*

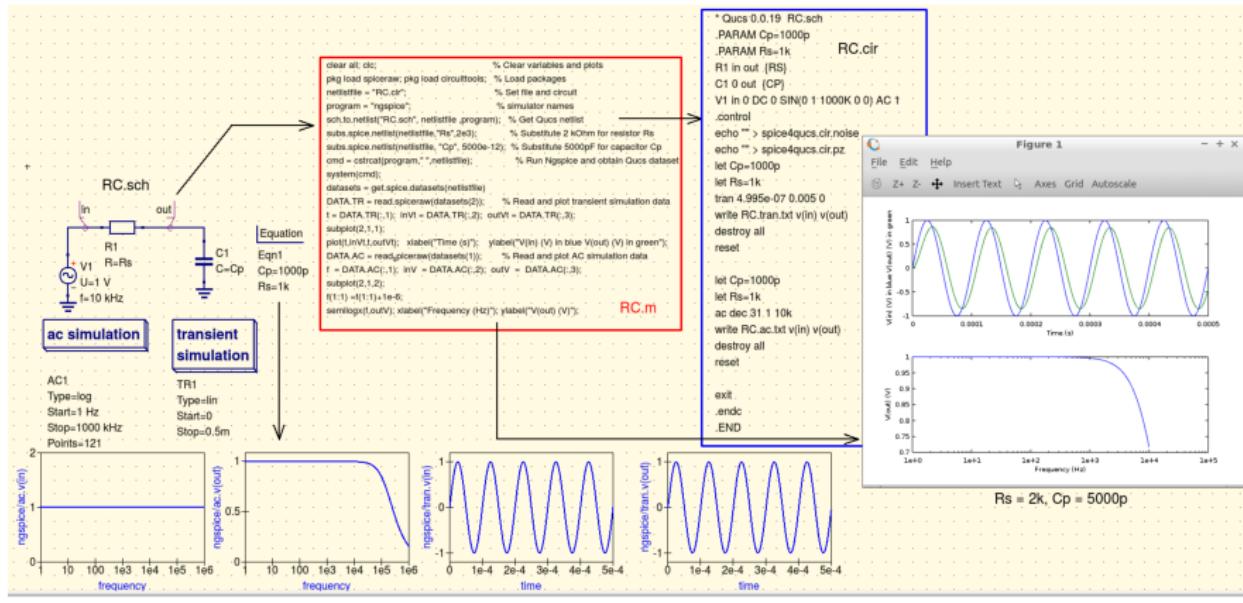
Where FILE – represents SPICE or Qucs netlist files

PARAM – represents a SPICE or Qucs variable or .MODEL parameter name

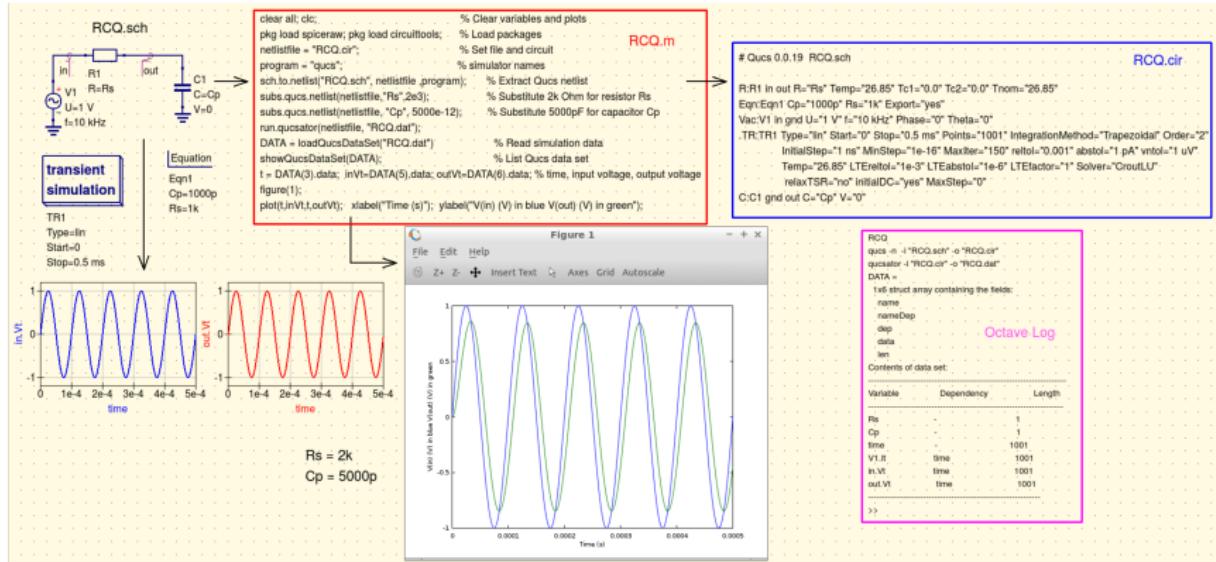
VALUE – represents a parameter value to replace its original quantity



# Qucs-S/Ngspice/Xyce Circuit Analysis and Compact Device Parameter Extraction from Manufacturers Data or Measurements Controlled by Octave Script Files: Part III Simple Ngspice example



# Qucs-S/Ngspice/Xyce Circuit Analysis and Compact Device Parameter Extraction from Manufacturers Data or Measurements Controlled by Octave Script Files: Part IV Simple Qucs example



# Qucs-0.0.19S : Qucs with SPICE 1

## Download links

The latest stable release is Qucs-0.0.19S. It is based on stable Qucs-0.0.19.

- Documentation at [readthedocs.io](#)
- Source tarball: [qucs-0.0.19S.tar.gz](#)
- Debian repository (32 and 64 bit), but with openSUSE OBS:
  - Debian 8 "Jessie" at: [download.opensuse.org](#)
  - Debian 7 "Wheezy" at: [download.opensuse.org](#)
- Windows installer (Zipped EXE): [qucs-0.0.19S-setup.zip](#)

[Installation instructions...](#)

## Contribution guide

Qucs-S is open for everyone's contribution. See [here](#) for contribution guide.

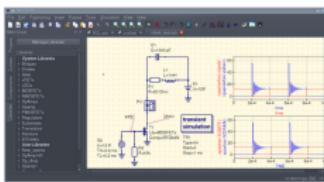
## What is Qucs-S?

Qucs-S is a spin-off of the [Qucs](#) cross-platform circuit simulator. "S" letter indicates SPICE. The purpose of the Qucs-S subproject is to use free SPICE circuit simulation kernels with the Qucs GUI. It merges the power of SPICE and the simplicity of the Qucs GUI. Qucs intentionally uses its own SPICE incompatible simulation kernel Qucsator. It has advanced RF and AC domain simulation features, but the most of existing industrial SPICE models are incompatible with it. Qucs-S is not a simulator by itself, but it requires to use a simulation backend with it. The schematic document format of Qucs and Qucs-S are fully compatible. Qucs-S allows to use the following simulation kernels with it:

- [Ngspice](#) is recommended to use. Ngspice is powerful mixed-level/mixed-signal circuit simulator. The most of industrial SPICE models are compatible with Ngspice. It has an excellent performance for time-domain simulation of switching circuits and powerful postprocessor.
- [XYCE](#) is a new SPICE-compatible circuit simulator written by Sandia from the scratch. It supports basic SPICE simulation types and has an advances RF simulation features such as Harmonic balance simulation.
- [SpiceOpus](#) is developed by the Faculty of Electrical Engineering of the Ljubljana University. It based on the SPICE-3S code
- Qucsator as backward compatible

## Qucs-S: Qucs with SPICE

## Simulation example with Qucs-S and Ngspice

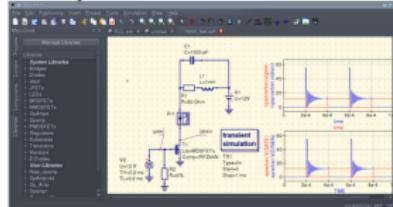


[\(More screenshots...\)](#)

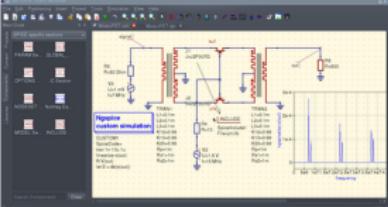


# Qucs-0.0.19S : Qucs with SPICE 2

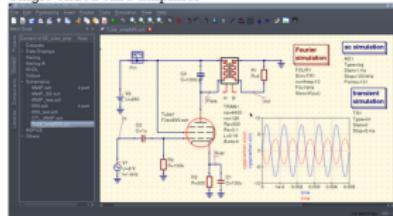
- MOSFET power switch



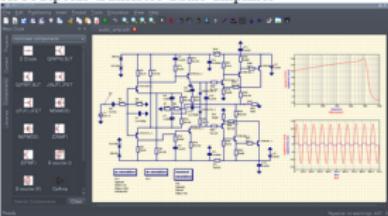
- JFET mixer



- Single-ended tube amplifier



- Hi-Fi bipolar transistor audio amplifier



[\(to top...\)](#)

## Main features

- Backward compatible with Qucs by the component types and simulations
- Direct support of SPICE models from components datasheets. SPICE model could be added to schematic without any adaptation.
- Basic SPICE components: RCL, BJT, MOSFET, JFET, MESFET, switches;
- Advanced SPICE components: Equation-defined sources and RCLs, transmission lines;
- Direct support of SPICE Modelcards, SPICE sections (.IC, .NODESET);
- Parametric circuits (.PARAM) and SPICE postprocessor (Nutmeg)
- Basic SPICE simulations: DC, AC, TRAN;
- Advanced SPICE simulation: DISTO, NOISE, Spectrum analysis;
- Single-tone and Multitone Harmonic balance analysis with XYCE backend;
- Nutmeg script simulation: direct access to the SPICE code and construct your own simulation;
- XYCE script simulation type;



## Qucs-S : Plans for the future 1; the next release

Plans for the next Qucs-S 0.0.20 release:

- Include an XSPICE code synthesizer;
- The support for .FUNC and Include scripts;
- Improvements in XYCE support: new components and .SENS analysis;
- Ngspice digital library;
- Synchronize code base with mainline Qucs and bugfixing;
- Release date scheduled: Summer 2017;

Source code available at:

- Stable and release candidates:

<https://github.com/ra3xdh/qucs/tree/qucs-s-stable>

- Development branch:

[https://github.com/ra3xdh/qucs/tree/spice4qucs\\_current](https://github.com/ra3xdh/qucs/tree/spice4qucs_current)



## Qucs-S : Plans for the future 2; more software features – Possible new directions for XSPICE synthesizer development

- Synthesize more complex XSPICE models: for example GaN HEMT, photodiodes and photoBJTs;
- Introduce a new generation of source based components, where their C code can be dynamically synthesized and compiled before simulation;
- Allow the linking of symbolic computation libraries to the XSPICE kernel to introduce symbolic computations at simulation time;
- Extend the number of devices in the pre-synthesized XSPICE libraries which are shipped with Qucs-S (currently very limited);

## Qucs-S : Plans for the future 3; Adding Open Source Hardware to Qucs-S – current low cost open source measurement hardware choices

Labrador (Espotek)  
\$29



Oscilloscope (2 channel, 750ksps)  
Arbitrary Waveform Generator (2 channel, 1MSPS)  
Power Supply (4.5 to 15V, 1.5W max, closed-loop)  
Logic Analyzer (2 channel, 3MSPS per channel, with serial decoding)  
Multimeter (V/I/R/C)  
Software compatible with Windows, OSX, and Linux

ADALM1000 (Analog Devices)  
£38



USB powered learning tool  
Measuring and sourcing current (- 200 to +200mA) and voltage  
(0 to 5V) simultaneously on same pin  
Oscilloscope (100 kSPS), function generator (100 kSPS)  
PixelPulse 2 (open source) supports Windows, Linux, OS X  
16-bit (0.05%) basic measure accuracy with 4 digit resolution  
Source and sink (2-quadrant) operation  
C, C++ and Python bindings  
MATLAB Data Acquisition Toolbox Support  
Open source hardware  
ADALP2000 Analog Parts Kit offers wide selection of analog  
components and allows solderless breadboarding



## Qucs-S : Plans for the future 4; Adding Open Source Hardware to Qucs-S – current low cost open source measurement hardware choices 2

adalm2000 (Analog Devices)  
\$99



Two-channel USB digital oscilloscope  
Two-channel arbitrary function generator  
16-channel digital logic analyzer (3.3V CMOS and 1.8V or 5V tolerant, 100MS/s)  
16-channel pattern generator (3.3V CMOS, 100MS/s)  
16-channel virtual digital I/O  
Two input/output digital trigger signals for linking multiple instruments (3.3V CMOS)  
Single channel voltmeter (AC, DC, ±20V)  
Network analyzer – Bode, Nyquist, Nichols transfer diagrams of a circuit. Range: 1Hz to 10MHz  
Spectrum Analyzer – power spectrum and spectral measurements (noise floor, SFDR, SNR, THD, etc.)  
Digital Bus Analyzers (SPI, I<sup>2</sup>C, UART, Parallel)  
Two programmable power supplies (0...+5V , 0...-5V)



## Qucs-S : Plans for the future 5; Adding Open Source Hardware to Qucs-S – current low cost open source measurement hardware choices 3

Analog Discovery 2 (Digilent)  
\$279



Two-channel USB digital oscilloscope (1 MΩ, ±25 V, differential, 14-bit, 100 MSPS, 30 MHz+ bandwidth - with the Analog Discovery BNC adapter board, 1286-1073-ND sold separately)

Two-channel arbitrary function generator (±5 V, 14-bit, 100 MSPS, 20 MHz+ bandwidth - with the Analog Discovery BNC adapter board, 1286-1073-ND sold separately )

Stereo audio amplifier to drive external headphones or speakers with replicated AWG signals

16-channel digital logic analyzer (3.3 V CMOS, 100 MSPS)

16-channel pattern generator (3.3 V CMOS, 100 MSPS)

16-channel virtual digital I/O including buttons, switches, and LEDs which are perfect for logic training applications

Two input/output digital trigger signals for linking multiple instruments (3.3 V CMOS)

